

54F/74F707

400 MHz 8-Bit TTL-ECL Register

General Description

The 'F707 TTL-ECL Shift Register is comprised of an 8-bit transparent holding register with TTL inputs for data and load enable which is translated internally to ECL levels. The holding register is the loading stage for the 8-bit shift register. The shift register is a single direction, two output shift register with a cascade input that is functional during serial shift operations.

The shift register also features a mode input (MODE) and differential ECL clock inputs (SC and \overline{SC}) for synchronous shifting and loading of data, both of which are done on the rising edge of the clock. The mode input is provided for selection of shifting or loading of data. Two outputs are available, one for every fourth bit of the shift register. Parallel loading will take place at speeds up to 100 MHz. Shifting will take place at speeds up to 400 MHz. The 'F707 was designed for high speed TTL-ECL translation applications in high resolution color graphics, instrumentation, and communication systems.

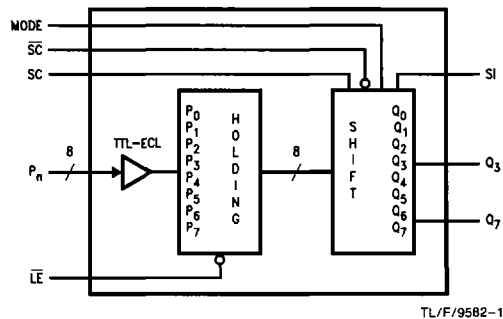
Features

- 400 MHz shift speed
- 100 MHz parallel load speed
- TTL parallel inputs
- ECL serial input
- 10K and 10KH ECL compatible
- Transparent data holding register
- Available in 20-lead DIP

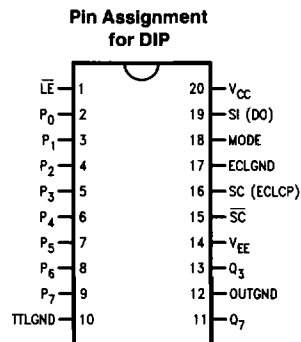
Applications

- High resolution color graphics
- CAE/CAD/CAM applications
- Radar Processing
- Instrumentation

Functional Block Diagram

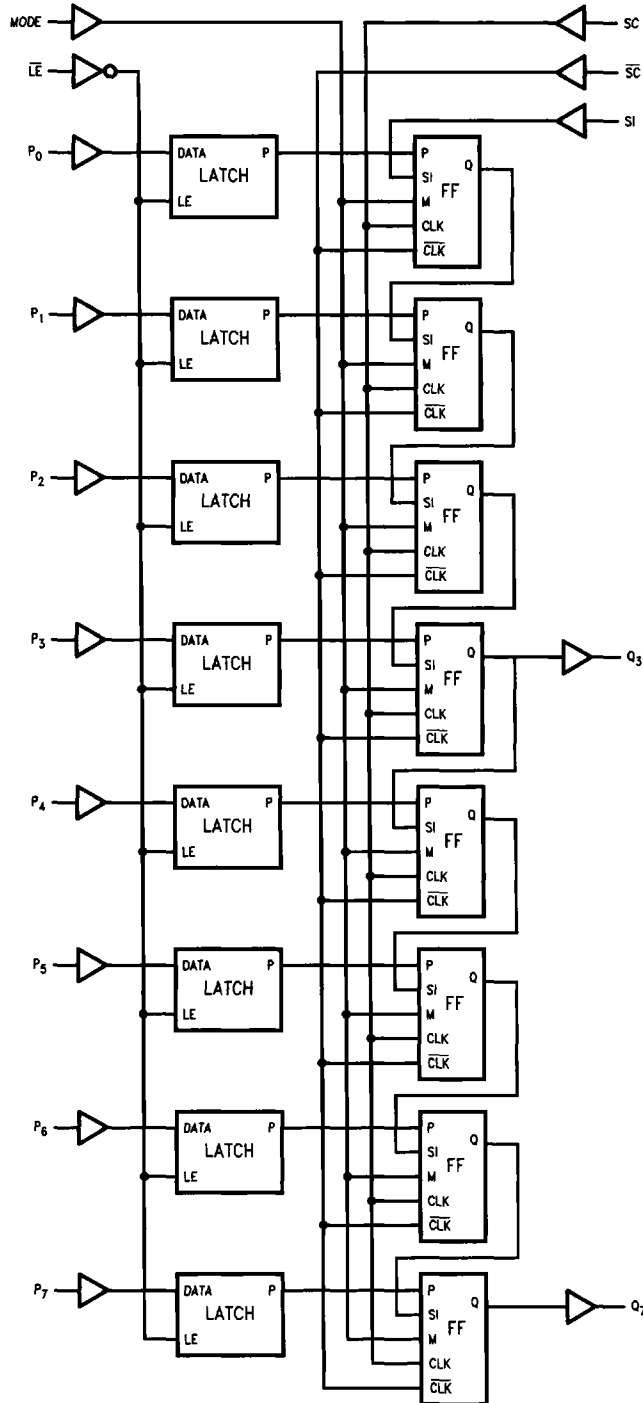


Connection Diagram



TL/F/9582-2

'F707 Logic Diagram



TL/F/9582-3