HD74HC881 ● Arithmetic Logic Unit/Function Generator **Preliminary**

The HD74HC881 has the same pinout and same functionality as the HD74HC181 except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M=H).
In the logic mode the HD74HC881 provides the user with a status check on the input words, A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P}=F_0+F_1+F_2+F_3$
$\overline{G}$="High"
$C_{n+4}=P \bullet C_n$

Table 1
$S_0=S_3=H$, $S_1=S_2=L$, $M=H$

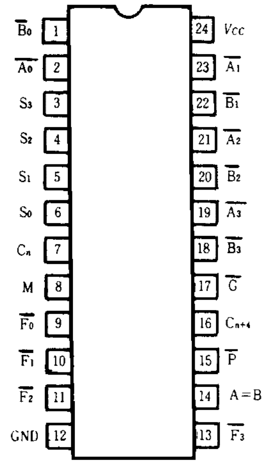
C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$A_0=B_0$	$A_1=B_1$	$A_2=B_2$	$A_3=B_3$	H	L	H
L	$A_0=B_0$	$A_1=B_1$	$A_2=B_2$	$A_3=B_3$	H	L	L
×	$A_0 \neq B_0$	×	×	×	H	H	L
×	×	$A_1 \neq B_1$	×	×	H	H	L
×	×	×	$A_2 \neq B_2$	×	H	H	L
×	×	×	×	$A_3 \neq B_3$	H	H	L

Table 2
$S_0=S_1=S_3=L$, $S_2=H$, $M=H$

C_n	Data Inputs				Outputs		
H	$\overline{A}_0$ or $\overline{B}_0=L$	$\overline{A}_1$ or $\overline{B}_1=L$	$\overline{A}_2$ or $\overline{B}_2=L$	$\overline{A}_3$ or $\overline{B}_3=L$	$\overline{G}$	$\overline{P}$	C_{n+4}
L	$\overline{A}_0$ or $\overline{B}_0=L$	$\overline{A}_1$ or $\overline{B}_1=L$	$\overline{A}_2$ or $\overline{B}_2=L$	$\overline{A}_3$ or $\overline{B}_3=L$	H	L	H
×	$\overline{A}_0$ or $\overline{B}_0=H$	×	×	×	H	L	L
×	×	$\overline{A}_1$ or $\overline{B}_1=H$	×	×	H	H	L
×	×	×	$\overline{A}_2$ or $\overline{B}_2=H$	×	H	H	L
×	×	×	×	$\overline{A}_3$ or $\overline{B}_3=H$	H	H	L

The combination of signals on the S_3 through S_0 control lines determine the operation performed on the data words to generate the output bits Fi. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The HD74HC881 has the unique feature of providing an A=B status while the exclusive OR ($\oplus$) function is being utilized. When the control inputs (S_3, S_2, S_1, S_0) equal H, L, L, H; a status check is generated to determine whether all pairs (Ai, Bi) are equal in the following manner: $P=(A_0 \oplus B_0)+(A_1 \oplus B_1)+(A_2 \oplus B_2)+(A_3 \oplus B_3)$. This unique bit-by-bit comparison of the data words which is available on the CMOS output is particularly useful when cascading HD74HC881's. As the A=B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A=B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A=B open drain output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity
If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being high it is necessary to place the control lines in the stage L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $P=\overline{A}_0\overline{B}_0+\overline{A}_1\overline{B}_1+\overline{A}_2B_2+\overline{A}_3\overline{B}_3$.

■ PIN ARRANGEMENT



(Top View)

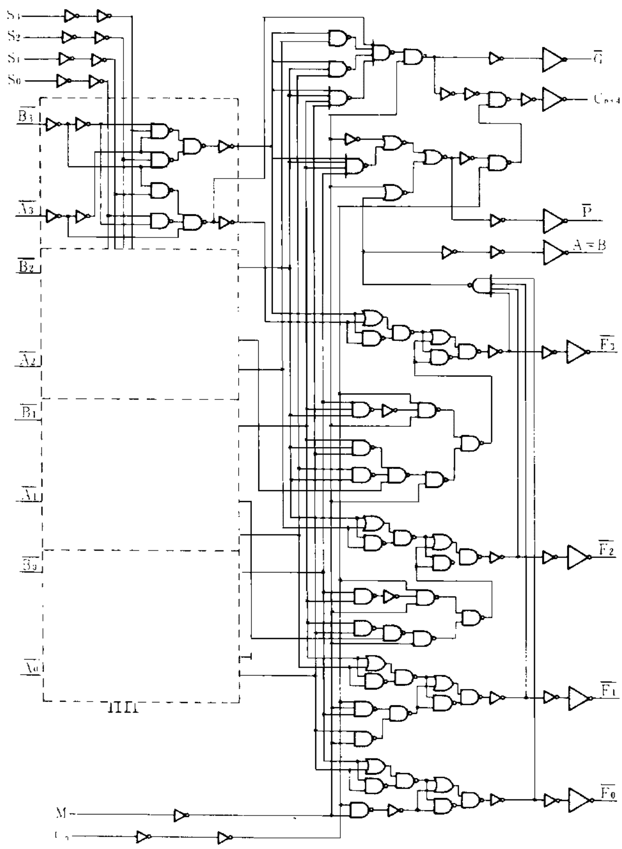
S_3	S_2	S_1	S_0	M	$\overline{P}=F_0+F_1+F_2+F_3$
L	H	L	L	H	$\overline{A}_0 \cdot \overline{B}_0+\overline{A}_1 \cdot \overline{B}_1+\overline{A}_2 \cdot \overline{B}_2+\overline{A}_3 \cdot \overline{B}_3$
H	L	L	H	H	$(A_0 \oplus B_0)+(A_1 \oplus B_1)+(A_2 \oplus B_2)+(A_3 \oplus B_3)$

■FEATURES

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

NOTE
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		$Ta=25°C$ min	$Ta=25°C$ typ	$Ta=25°C$ max	$Ta=-40\sim+85°C$ min	$Ta=-40\sim+85°C$ max	Unit
Input Voltage	V_{IH}	2.0			1.5	–	–	1.5	–	V
		4.5			3.15	–	–	3.15	–	
		6.0			4.2	–	–	4.2	–	
	V_{IL}	2.0			–	–	0.5	–	0.5	V
		4.5			–	–	1.35	–	1.35	
		6.0			–	–	1.8	–	1.8	
Output Voltage	V_{OH}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	–	1.9	–	V
		4.5			4.4	4.5	–	4.4	–	
		6.0			5.9	6.0	–	5.9	–	
		4.5		$I_{OH}=-4mA$	4.18	–	–	4.13	–	
		6.0		$I_{OH}=-5.2mA$	5.68	–	–	5.63	–	
	V_{OL}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	–	0.0	0.1	–	0.1	V
		4.5			–	0.0	0.1	–	0.1	
		6.0			–	0.0	0.1	–	0.1	
		4.5		$I_{OL}=4mA$	–	–	0.26	–	0.33	
		6.0		$I_{OL}=5.2mA$	–	–	0.26	–	0.33	
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		–	–	4.0	–	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C			Ta=−40～+85°C		Unit
				min.	typ.	max.	min.	max.	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	C_n to C_{n+4}	–	–	200	–	250	ns
		4.5		–	–	40	–	50	
		6.0		–	–	34	–	43	
	t_{PLH} t_{PHL}	2.0	C_n to any F	–	–	150	–	190	ns
		4.5		–	–	30	–	38	
		6.0		–	–	26	–	33	
	t_{PLH} t_{PHL}	2.0	A or B to G S_0=S_3=V_{CC}, S_1=S_2=GND	–	–	150	–	190	ns
		4.5		–	–	30	–	38	
		6.0		–	–	26	–	33	
	t_{PLH} t_{PHL}	2.0	A or B to G S_0=S_3=GND, S_1=S_2=V_{CC}	–	–	150	–	190	ns
		4.5		–	–	30	–	38	
		6.0		–	–	26	–	33	
	t_{PLH} t_{PHL}	2.0	A or B to P	–	–	150	–	190	ns
		4.5		–	–	30	–	38	
		6.0		–	–	26	–	33	
	t_{PLH} t_{PHL}	2.0	A_1 or B_1 to F_1 S_0=S_3=V_{CC}, S_1=S_2=GND	–	–	240	–	300	ns
		4.5		–	–	48	–	60	
		6.0		–	–	41	–	51	
	t_{PLH} t_{PHL}	2.0	A or B to C_{n+4} S_0=S_3=V_{CC}, S_1=S_2=GND	–	–	250	–	315	ns
		4.5		–	–	50	–	63	
		6.0		–	–	43	–	54	
	t_{PLH} t_{PHL}	2.0	A_1 or B_1 to F_1 S_1=S_2=V_{CC} or M=V_{CC}	–	–	275	–	345	ns
		4.5		–	–	55	–	69	
		6.0		–	–	47	–	59	
	t_{PLH} t_{PHL}	2.0	A or B to A=B	–	–	280	–	350	ns
		4.5		–	–	56	–	70	
		6.0		–	–	48	–	60	
	t_{PLH} t_{PHL}	2.0	A or B to C_{n+4} S_0=S_3=GND, S_1=S_2=V_{CC}	–	–	280	–	350	ns
		4.5		–	–	56	–	70	
		6.0		–	–	48	–	60	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		–	–	75	–	95	ns
		4.5		–	–	15	–	19	
		6.0		–	–	13	–	16	
Input Capacitance	C_{in}	–		–	5	10	–	10	pF