



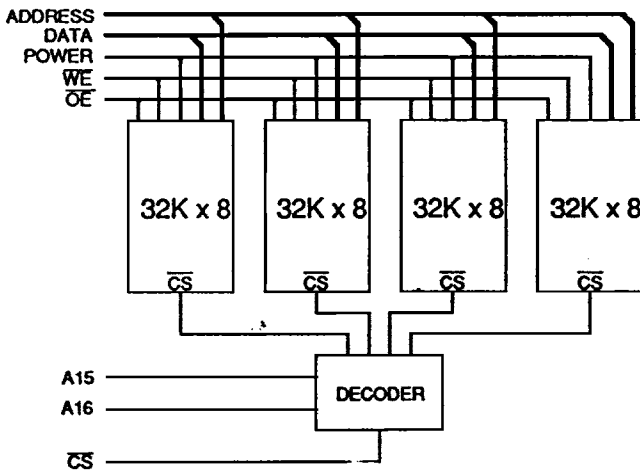
Mosaic
Semiconductor
Inc.

131,072 x 8 CMOS EEPROM

Features

- Fast Access Times of 200/250/300/350 ns
- JEDEC 1Mb EEPROM Standard 32 pin DIL footprint
- Operating Power 495 mW (max)
- Standby Power 72 mW (max)
- Hardware and Software Data Protection
- Byte and Page Write up to 64 bytes in 12ms
- DATA Polling for End of Write Detection
- 10⁴ Erase/Write cycles & 10 year Data Retention
- Completely Static Operation
- May be Screened in accordance with MIL-STD-883C (suffix MB)

Block Diagram



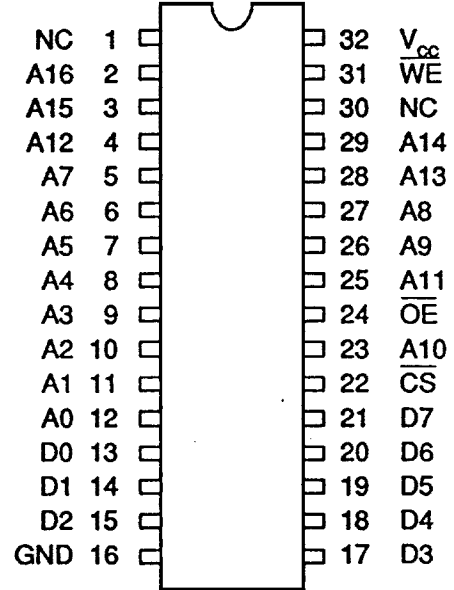
128K X 8 EEPROM

ME8128SC-20/25/30/35

Issue 1.6: November 1991

ADVANCE PRODUCT INFORMATION

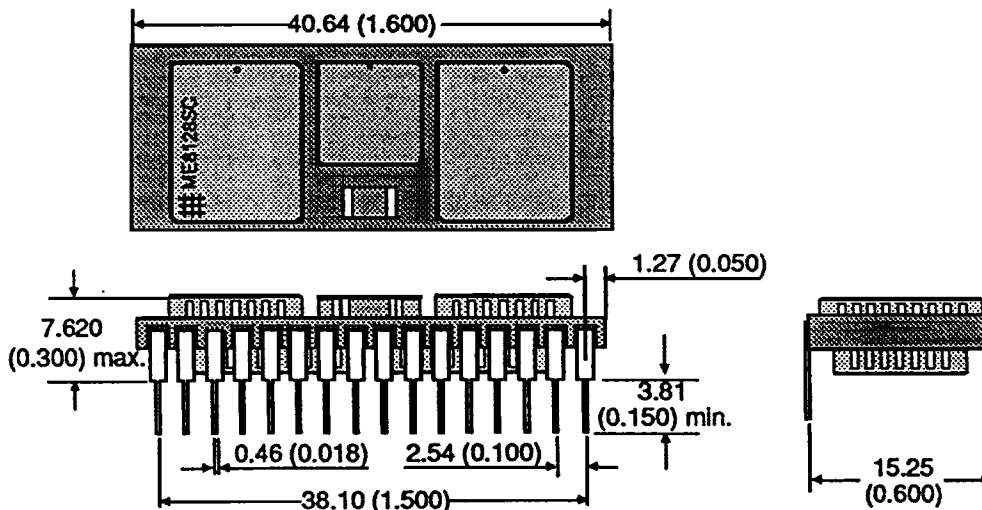
Pin Definition



Pin Functions

- A0-A16 Address Inputs
- D0-7 Data Input/Output
- CS Chip Select
- OE Output Enable
- WE Write Enable
- NC No Connect
- V_{cc} Power (+5V)
- GND Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings

Voltage on any pin relative to GND	V_T	-0.6V to +6.25	V
Voltage on OE and A9 relative to GND	V_{OEA}	-0.6V to +13.5	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature Under Bias	T_{BAS}	-55 to +125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
 (2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		<i>min</i>	<i>typ</i>	<i>max</i>	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (ME8128SCI)
	T_{AM}	-55	-	125	°C (ME8128SCM,MB)

DC Electrical Characteristics ($V_{CC}=5V\pm 10\%$, $T_A=-55$ to $+125^\circ C$)

Parameter	Symbol	Test Condition	<i>min</i>	<i>max</i>	Unit
Input Leakage Current (A15, A16, \overline{CS})	I_{L1}	$0V \leq V_{IN} \leq V_{CC}$	-	40	μA
	I_{L2}	$0.5V \leq V_{IN} \leq 2.7V$	-	8	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$, $V_{IO}=\text{Gnd to } V_{CC}$	-	40	μA
Operating Supply Current	I_{CC}	$f = 5 \text{ MHz}$, $I_{IO}=0\text{mA}$	-	90	mA
Standby Current	I_{SB}	TTL Levels	-	13	mA
Standby Current	I_{SB1}	CMOS Levels (1)	-	1.36	mA
Output Voltage	V_{OL}	$I_{OL}=2.1\text{mA}$	-	0.45	V
	V_{OH}	$I_{OH}=-400\mu A$	2.4	-	V

Capacitance ($V_{CC}=5V\pm 10\%$, $T_A=25^\circ C$, $f=1\text{MHz}$)

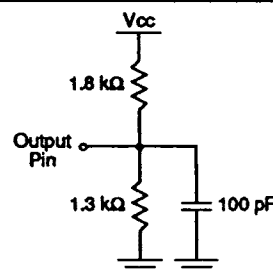
Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance (\overline{CS} , A15, A16)	C_{IN1}	$V_{IN} = 0V$	-	6	pF
I/P Capacitance (other)	C_{IN2}	$V_{IN} = 0V$	16	24	pF
I/O Capacitance	C_{IO}	$V_{IO} = 0V$	32	48	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

- * Input pulse levels: 0.8V to 2.4V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: 1 TTL gate + 100pF
- * $V_{CC}=5V\pm 10\%$

Output Test Load



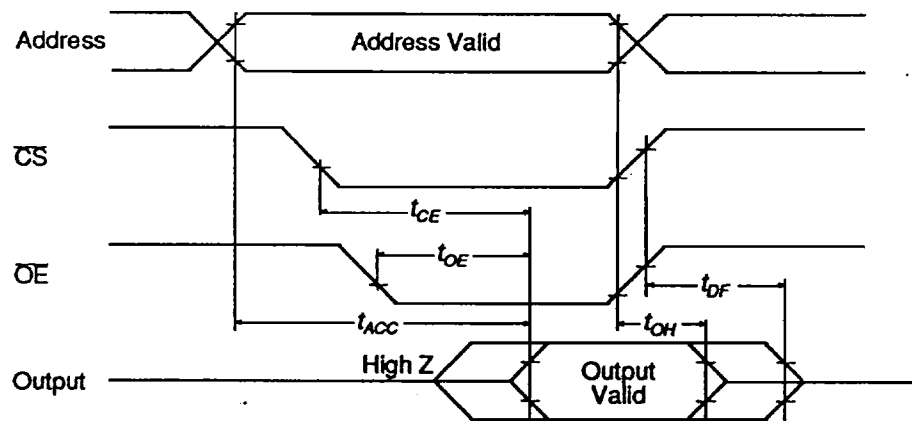
AC READ CHARACTERISTICS

Read Cycle

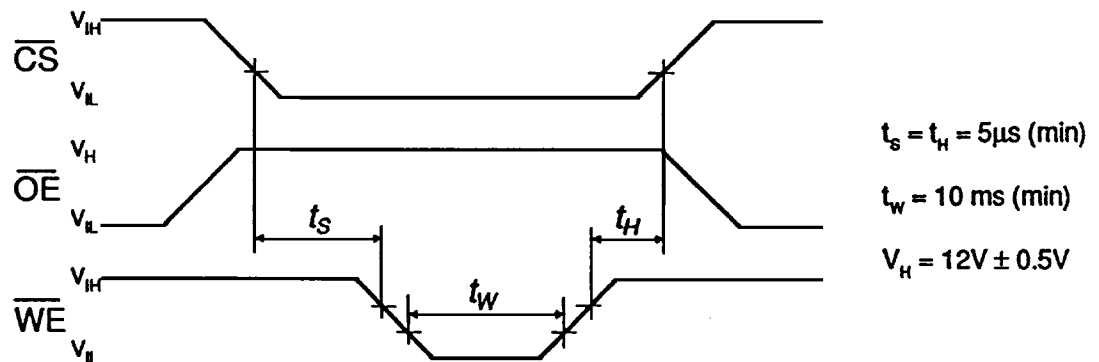
Parameter	Symbol	-200		-250		-300		-350		Unit
		min	max	min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	-	200	-	250	-	300	-	350	ns
\overline{CS} to Output Delay	t_{CS1}	-	200	-	250	-	300	-	350	ns
\overline{OE} to Output Delay	t_{OE2}	0	80	0	90	0	90	0	90	ns
\overline{CS} or \overline{OE} to Output Float	$t_{DF3,4}$	0	60	0	60	0	80	0	80	ns
Output Hold from \overline{OE} , \overline{CS} or Address, (whichever occurred first)	t_{OH}	0	-	0	-	0	-	0	-	ns

- Notes: (1) \overline{CS} may be delayed up to $t_{ACC} - t_{CS}$ after the address transition without impact on t_{ACC} .
 (2) \overline{OE} may be delayed up to $t_{CS} - t_{OE}$ after the falling edge of \overline{CS} without impact on t_{CS} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 (3) t_{DF} is specified from \overline{OE} or \overline{CS} whichever occurs first ($C_L = 5pF$).
 (4) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform



Chip Erase Waveform



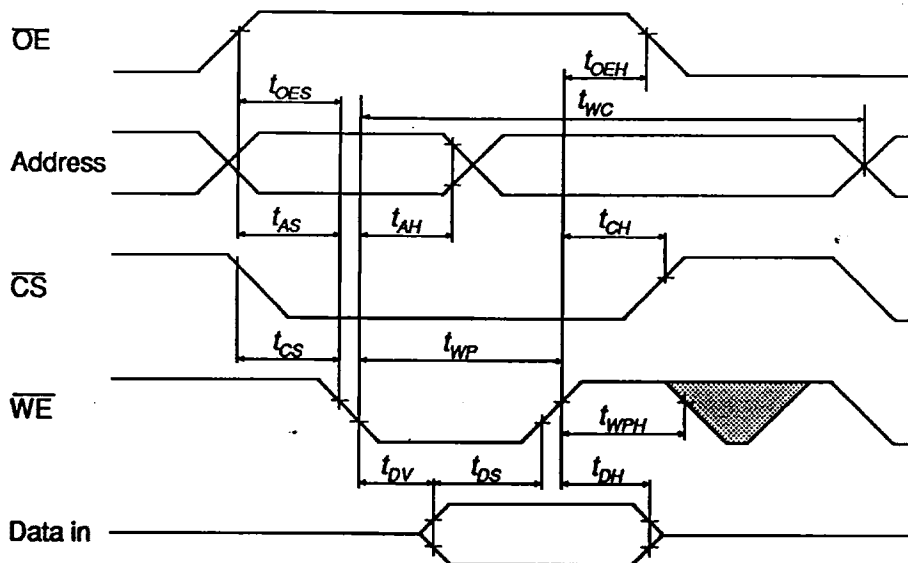
AC WRITE CHARACTERISTICS

Write Cycle

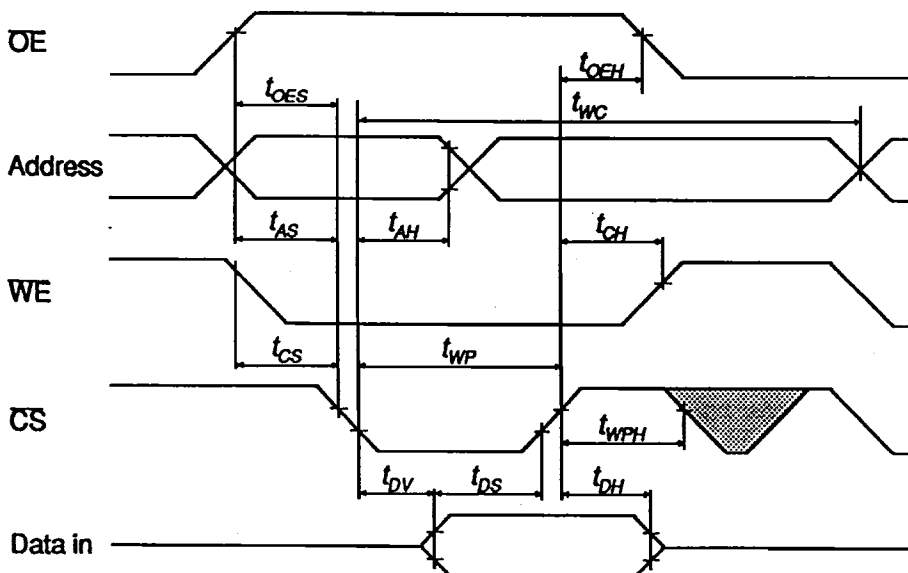
Parameter	Symbol	min	typ	max	Unit
Address, \overline{OE} Set-up Time	t_{AS}, t_{OES}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width (\overline{WE} or \overline{CS})	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, OE Hold Time	t_{DH}, t_{OEH}	0	-	-	ns
Time to Data Valid	t_{DV}	NR ⁽¹⁾	-	-	-
Write Cycle Time	t_{WC}	0.4	-	12	ms

Note: (1) NR = No Restriction

AC Write Waveform - \overline{WE} Controlled



AC Write Waveform - \overline{CS} Controlled

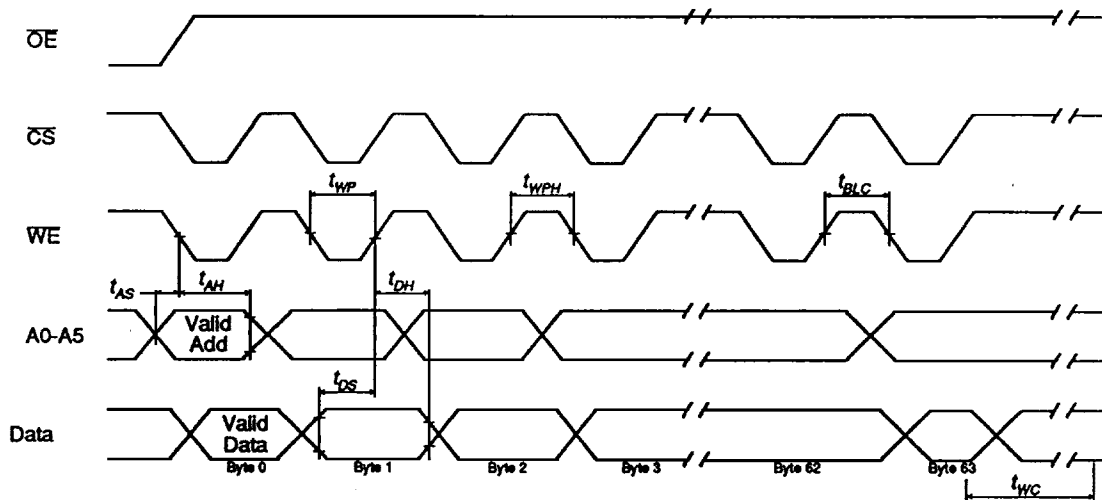


PAGE MODE WRITE CHARACTERISTICS

Write Cycle

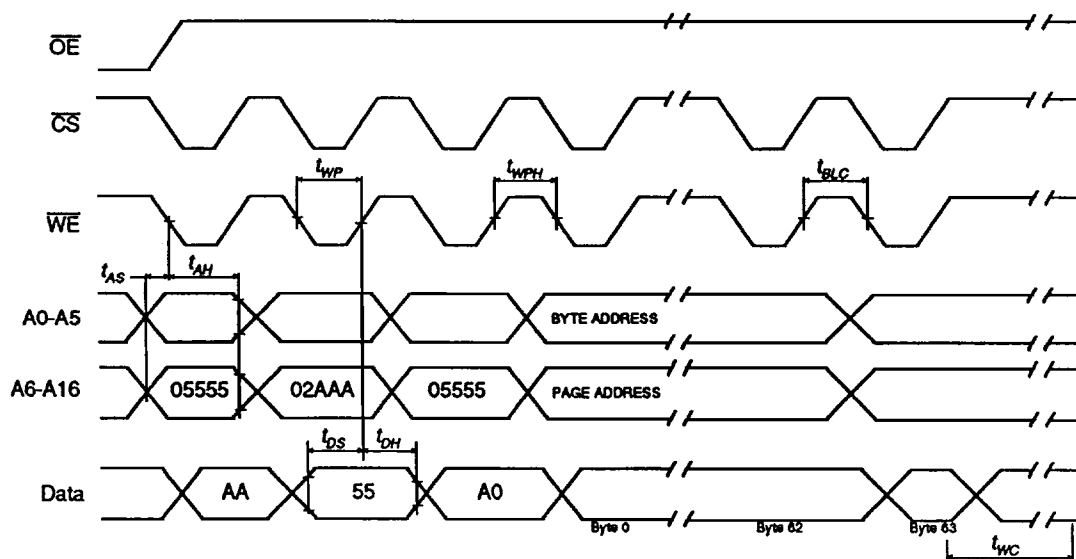
Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	0.4	-	12	mS
Address Set-up Time	t_{AS}	0	-	-	nS
Address Hold Time	t_{AH}	50	-	-	nS
Data Set-up Time	t_{DS}	50	-	-	nS
Data Hold Time	t_{DH}	0	-	-	nS
Write Pulse Width	t_{WP}	100	-	-	nS
Byte Load Cycle Time	t_{BLC}	-	-	300	μ S
Write Pulse Width High	t_{WPH}	50	-	-	nS

Page Mode Write Waveform



Note: A6 through A16 must specify the page address during each high to low transition of \overline{WE} (or \overline{CE}).
 \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

Software Protected Write Waveform



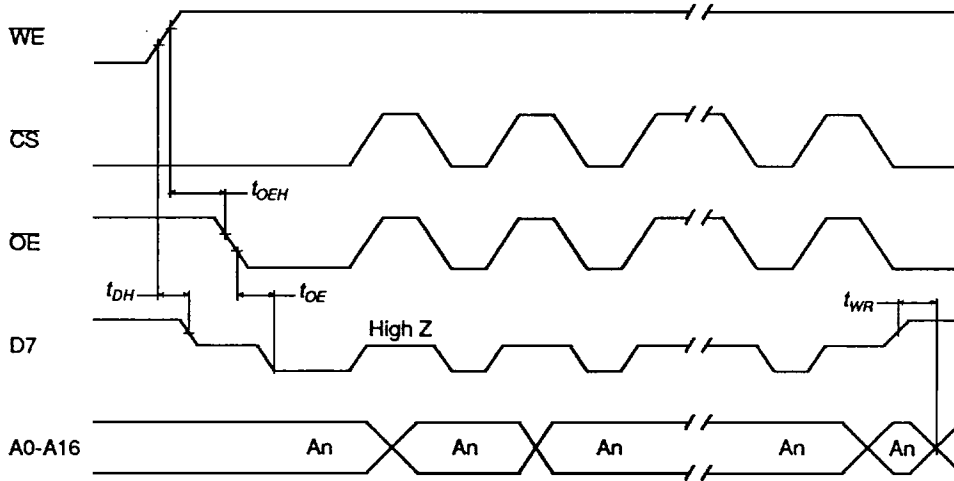
Note: A6 through A16 must specify the page address during each high to low transition of \overline{WE} (or \overline{CE}).
 The example addresses above are for EEPROM 1 on the module - see page 8 for full details.
 \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

DATA Polling Characteristics (1)

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	0	-	-	ns
OE Hold Time	t_{OE}	0	-	-	ns
OE to Output Delay	t_{OE}	-	-	100	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

DATA Polling Waveform

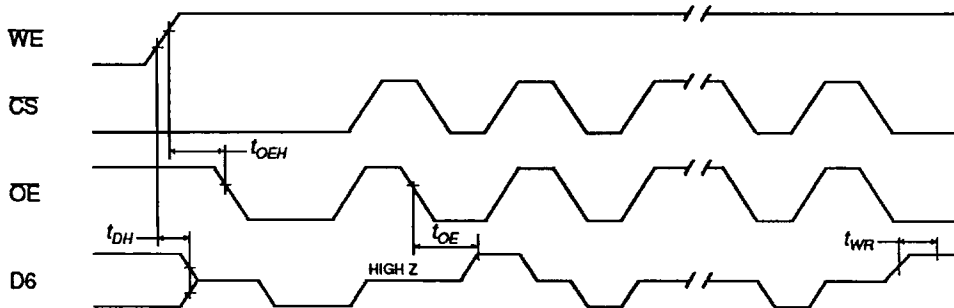


Toggle Bit Characteristics (1)

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	10	-	-	ns
OE Hold Time	t_{OE}	10	-	-	ns
OE to Output Delay	t_{OE}	-	-	100	ns
OE High Pulse	t_{OEHP}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Note : (1) These parameters are sampled and not 100% tested.

Toggle Bit Waveform



- Notes : (1) Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
- (2) Beginning and ending state of D6 may vary.
- (3) Any address location may be used but the address should not vary.

Device Operation

Read

The ME8128SC is accessed in the same way as a static RAM, with the data stored at the memory location determined by the address pins being placed on the output pins when \overline{CS} and \overline{OE} are low, and \overline{WE} is high. Whenever \overline{CS} or \overline{OE} are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on \overline{WE} with \overline{CS} low or a low pulse on \overline{CS} with \overline{WE} low indicates a Write Cycle. The address is latched on the falling edge of \overline{CS} or \overline{WE} , and the data is latched on the first rising edge of \overline{CS} or \overline{WE} . Once a Byte Write has begun it will automatically time itself to completion.

Page Mode Write

This mode allows 2 to 64 bytes of data to be loaded into an EEPROM, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of \overline{WE} (or \overline{CS}) within 100 μ s of the same transition of the previous byte. If this 100 μ s time is exceeded, the load period ends and internal programming starts. A6 to A16 specify the page address (which must be valid during the above transitions) and A0 to A5 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

Chip Erase

All of the memory locations on the ME8128SC module can be erased in 10 ms by placing 12.0V \pm 0.5V onto \overline{OE} and controlling \overline{WE} , A15 and A16 to follow the Chip Erase timing characteristics. This function will operate even if the module is in Software Data Protection Mode as explained later.

DATA Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to Read the device will result in the complement of the written data appearing on D7. Once the Write Cycle is complete true data appears on the outputs and the next Write Cycle may begin.

TOGGLE bit

In addition to \overline{DATA} polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Device Identification

An extra 256 bytes of EEPROM memory are available to the user, arranged as 4 blocks of 64 bytes, accessed by first placing 12V \pm 0.5V on A9. These locations can be used during the initial programming of each EEPROM to record data such as issue number and release date, and subsequent reprogramming can change these locations to record the alterations performed.

The following shows the addresses used to select each block of 64 bytes, which can be Written to or Read from in the same way as the rest of the memory.

BLOCK NUMBER	START ADDRESS	END ADDRESS
1	07FC0	07FFF
2	0FFC0	0FFFF
3	17FC0	17FFF
4	1FFC0	1FFFF

Operating Modes

The table below shows the logic inputs required to control the operating modes of the ME8128SC.

MODE	\overline{CS}	\overline{OE}	\overline{WE}	OUTPUTS
Read	0	0	1	Data Out
Write ⁽¹⁾	0	1	0	Data In
Standby	1	X	X	Floating
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	Floating
Chip Erase	0	V _H	0	Floating

1 = V_H 0 = V_L X = Don't care V_H = 12.0V \pm 0.5V

Note: (1) Refer to AC Programming Waveforms

Hardware Data Protection

Four types of hardware protection give high security against accidental writes:

- If V_{CC} < 3.8V write is inhibited
- At power on, the device times out 5ms before allowing a Write.

- (c) \overline{OE} low, \overline{CS} or \overline{WE} high inhibits writes.
- (d) Pulses of less than 15ns on \overline{WE} or \overline{CS} do not initiate a write cycle.

Software Data Protection

Software controlled data protection, once enabled by the user, necessitates the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of Writes must be performed, and must be reused for each subsequent Write cycle. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

Note that the ME8128SC is supplied with the Software Data Protection feature disabled.

The ME8128SC consists of four 32K x 8 EEPROMs; which device is active at a particular time (subject to OE, WE and CS inputs) is controlled by address lines A15 and A16. The Memory Map of this module is arranged as follows :

EEPROM NUMBER	ADDRESSING RANGE	
	START	END
1	00000	07FFF
2	08000	0FFFF
3	10000	17FFF
4	18000	1FFFF

The Software Data Protection operation mode is available on a single device independent of the mode of the others e.g. one EEPROM could be protected while the others were not. However this situation is undesirable because the current mode of each EEPROM would have to be recorded during operation in order to avoid trying to Write to a device without first issuing the correct command codes.

Because of this it is advisable that if this feature is to be used then all four devices on each module are either disabled or enabled at the same time. Software Data Protection Enable for any device can be achieved by using the following table:

ACTION PERFORMED	EEPROM NUMBER			
	1	2	3	4
LOAD DATA ⁽¹⁾	AA	AA	AA	AA
TO ADDRESS ⁽¹⁾	05555	0D555	15555	1D555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	0AAAA	12AAA	1AAAA
LOAD DATA	A0	A0	A0	A0
TO ADDRESS	05555	0D555	15555	1D555
WRITE ENABLED ⁽²⁾				
LOAD DATA ⁽³⁾	ANY	ANY	ANY	ANY
TO ADDRESS	ANY VALID FOR PAGE WRITE			
LOAD LAST DATA	ANY	ANY	ANY	ANY
TO LAST ADDRESS	ANY VALID FOR PAGE WRITE			
ENTER DATA PROTECTED STATE				

- Notes : (1)Data D7 - D0 (hex); Address A16 - A0 (hex).
- (2) Write Protect Mode will be activated at end of Write even if no other data is loaded.
- (3) 1 to 64 bytes of data may be loaded.

In order to enable Data Protection for the entire ME8128SC module, the sequence of three loads shown above must be performed for each EEPROM in turn, totalling 12 loads in all. Once activated, the same three bytes must be loaded to the same addresses before any Writes will occur to a particular device. All software write commands must obey the Page Write timing specifications:

The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes must be loaded to specific locations for each EEPROM as shown in the table below:

ACTION PERFORMED	EEPROM NUMBER			
	1	2	3	4
LOAD DATA ⁽¹⁾	AA	AA	AA	AA
TO ADDRESS ⁽¹⁾	05555	0D555	15555	1D555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	0AAAA	12AAA	1AAAA
LOAD DATA	80	80	80	80
TO ADDRESS	05555	0D555	15555	1D555
LOAD DATA	AA	AA	AA	AA
TO ADDRESS	05555	0D555	15555	1D555
LOAD DATA	55	55	55	55
TO ADDRESS	02AAA	0AAAA	12AAA	1AAAA
LOAD DATA	20	20	20	20
TO ADDRESS	05555	0D555	15555	1D555
EXIT DATA PROTECTED STATE ⁽²⁾				
LOAD DATA ⁽³⁾	ANY	ANY	ANY	ANY
TO ADDRESS	ANY VALID FOR PAGE WRITE			
LOAD LAST DATA	ANY	ANY	ANY	ANY
TO LAST ADDRESS	ANY VALID FOR PAGE WRITE			

- Notes : (1)Data D7 - D0 (hex); Address A16 - A0 (hex).
- (2) Write Protect Mode will be activated at end of Write even if no other data is loaded.
- (3) 1 to 64 bytes of data may be loaded.

Thus, to disable the Software Data Protection mode for the module 24 bytes have to be loaded.

Note here the use of the word 'load' to describe enabling and disabling the protection modes in preference to 'write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes at those addresses will be overwritten with AA,55,A0, this is not the case. This is because these Writes obey Page Write parameters, where A6 - A16 must remain valid to specify the page address, but during this enable sequence they change. Actual Writes therefore never occur, and data is not corrupted during an enable sequence.

For the same reasons no Writes are performed during the disable routine, in addition to the fact that since Data Protection is enabled no Writes can occur without the correct bytes being loaded in sequence.

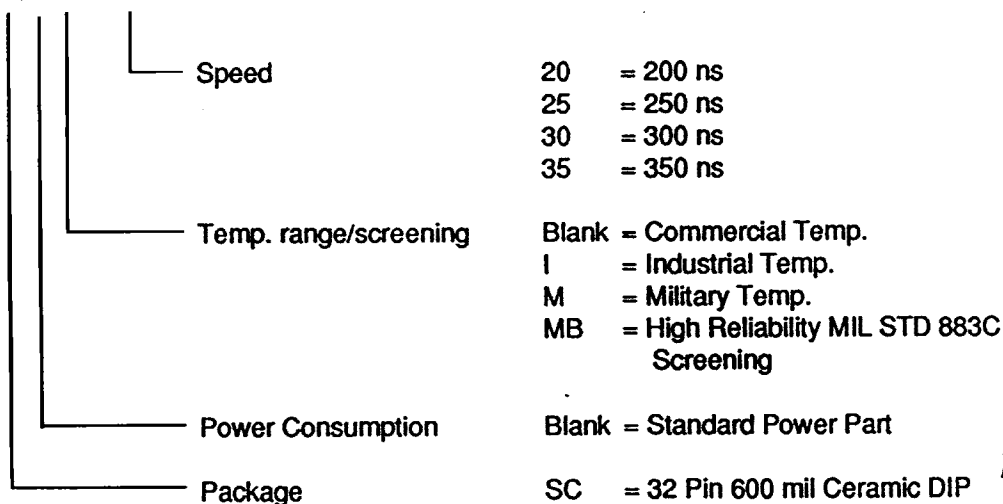
Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical External visual Temperature cycle	2017 Condition B (or manufacturers equivalent) 1010 Condition C (10 Cycles, -65°C to +150°C)	100% 100%
Burn-In Pre Burn-in Electrical Burn-In	Per Applicable device Specifications at $T_A = +25^\circ\text{C}$ (optional) Method 1015, Condition D, $T_A = +125^\circ\text{C}$	100% 100%
Final Electrical Tests Static (dc) Functional Switching (ac)	Per applicable Device Specification a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A = +25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at $T_A = +25^\circ\text{C}$	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	

Ordering Information

ME8128SCMB-20



Mosaic Semiconductor Inc.

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.