National Semiconductor

February 1999

54AC377 • 54ACT377
Octal D Flip-Flop with Clock Enable

General Description

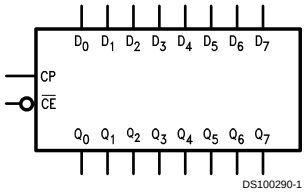
The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

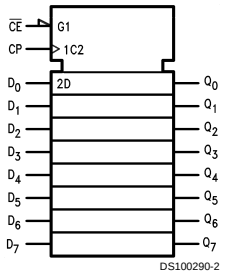
Features

- I_{CC} reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - — 'AC377: 5962-88702
  - — 'ACT377: 5962-87697

Logic Symbols



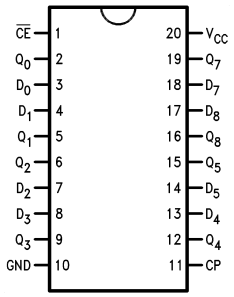
IEEE/IEC



Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams

Pin Assignment for DIP and Flatpak



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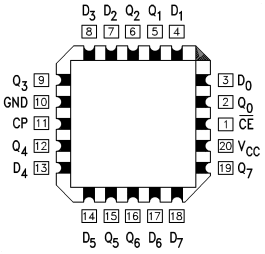
Pin Assignment for LCC



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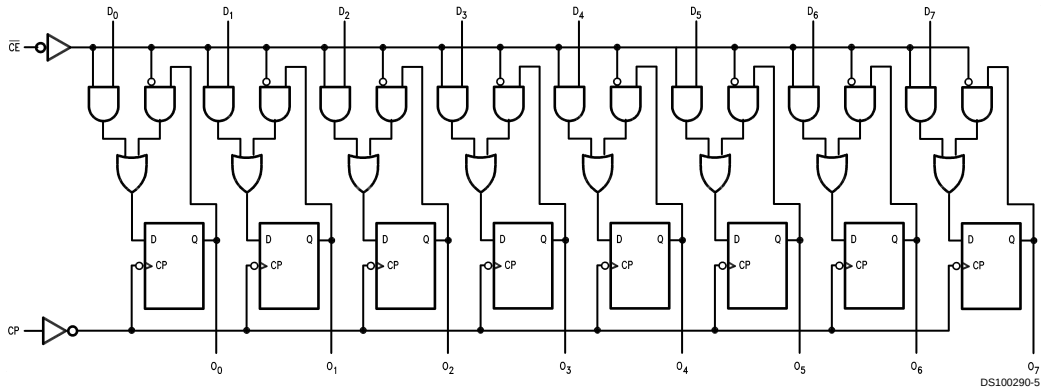
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 µA
		4.5	4.4		
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 µA
		4.5	0.1		
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{OLD}	(Note 4) Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.4 5.4	V	I_{OUT} = −50 µA
					(Note 6) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	3.70 4.70	V	I_{OH} = −24 mA I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
					(Note 6) V_{IN} = V_{IL} or V_{IH}
		4.5 5.5	0.50 0.50	V	I_{OL} = 24 mA I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 7) Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 6: *All outputs loaded; thresholds on input associated with output under test.

Note 7: †Maximum test duration 2.0 ms, one output loaded at a time.

Note 8: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	3.3	75		MHz	
		5.0	95			
t_{PLH}	Propagation Delay CP to Q_n	3.3	1.0	14.0	ns	
		5.0	1.5	10.0		
t_{PHL}	Propagation Delay CP to Q_n	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 10)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	7.5	ns	
		5.0	6.0		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	1.5	ns	
		5.0	2.5		
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3	9.5	ns	
		5.0	6.0		
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3	1.0	ns	
		5.0	2.0		
t_w	CP Pulse Width HIGH or LOW	3.3	6.5	ns	
		5.0	5.0		

Note 10: Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 11)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85		MHz	
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.5	11.0	ns	
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.5	12.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

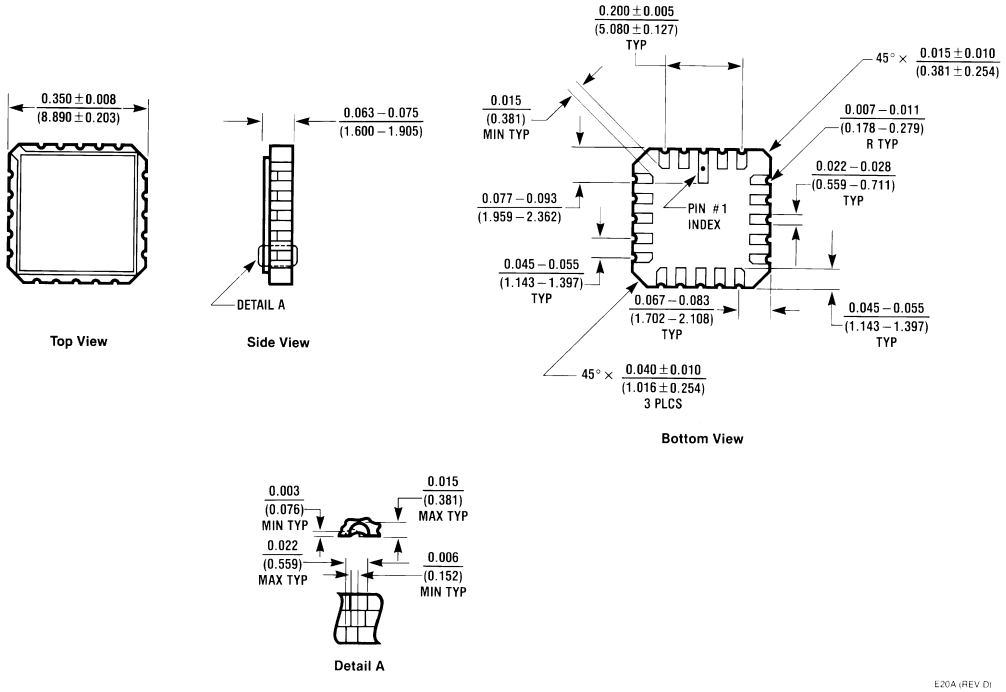
Symbol	Parameter	V_{CC} (V) (Note 12)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	7.0	ns	
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	ns	
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0	7.0	ns	
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0	1.0	ns	
t_w	CP Pulse Width HIGH or LOW	5.0	5.5	ns	

Note 12: Voltage Range 5.0 is 5.0V ±0.5V

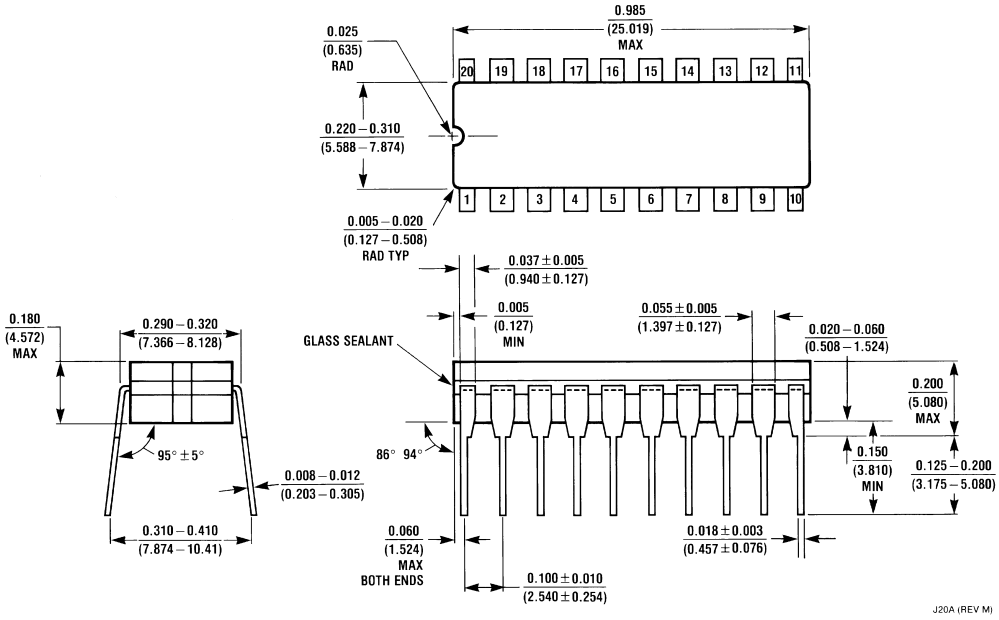
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	90.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

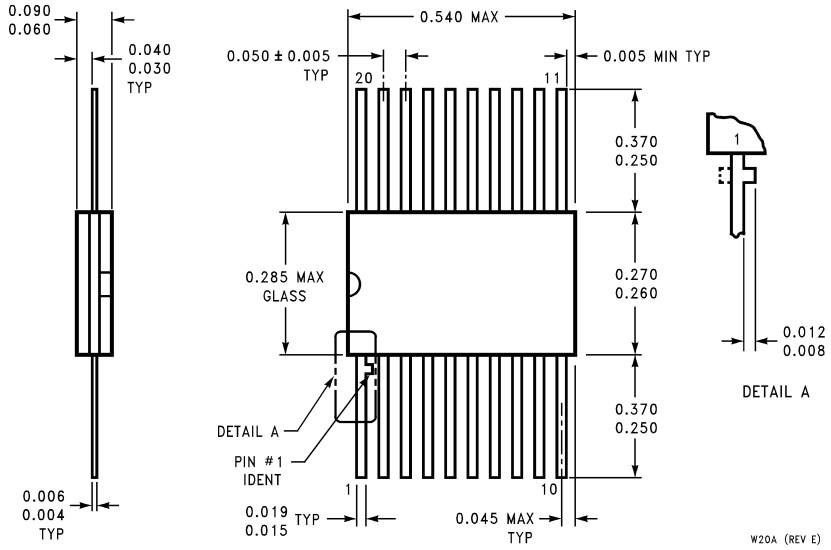


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20 Lead Ceramic Flatpak (F)
NS Package Number W20A

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54ACT377 Octal D Flip-Flop with Clock Enable

Contents

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- See '374 for TRI-STATE version
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Datasheet

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
54AC377 54ACT377 Octal D Flip-Flop with Clock Enable	177 Kbytes	2-Feb-99	View Online	Download	Receive via Email

Please use Adobe Acrobat to view PDF file(s).
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Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	# pins		SPICE	IBIS		Quantity	$US each		
5962-8769701M2A	LCC	20	Full production	N/A	N/A	.	50+	$9.0000	tube of 50	[logo]¢Z¢S¢4¢A 54ACT377 LMQB /Q¢M$E 5962-8769701M2A

5962-8769701MRA	Cerdip	20	Full production	N/A	N/A	.	50+	$8.0000	tube of 20	[logo]¢Z¢S¢4¢A$E 54ACT377DMQB /Q¢M 5962-8769701MRA
5962-8769701MSA	Cerpack	20	Full production	N/A	N/A	.	50+	$9.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 54ACT377FMQB Q¢M 5962-8769701MSA
5962-8769701B2A	LCC	20	Full production	N/A	N/A	.	50+	$27.0000	tube of 50	[logo]¢Z¢S¢4¢A QS $E 27014 5962-8769701B2A
5962-8769701BRA	Cerdip	20	Full production	N/A	N/A	.	50+	$22.0000	tube of 20	[logo] ¢Z¢S¢4¢A$E 5962-8769701BRA 27014 QS
5962-8769701BSA	Cerpack	20	Full production	N/A	N/A	.	50+	$24.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 5962-8769701BSA 27014 QS
5962-8769701S2A	LCC	20	Full production	N/A	N/A	.	50+	$138.0000	tube of 50	[logo]¢Z¢S¢4¢A 27014 Q $E 5962-8769701S2A
5962-8769701SRA	Cerdip	20	Full production	N/A	N/A	.	50+	$138.0000	tube of 20	[logo] ¢Z¢S¢4¢A$E 5962-8769701SRA 27014 Q
5962-8769701SSA	Cerpack	20	Full production	N/A	N/A	.	50+	$138.0000	tube of 19	[logo]¢Z¢S¢4¢A$E 5962-8769701SSA 27014 Q

[Information as of 1-Sep-2000]