HA19209, HA19210

8-Bit Flash Type Analog-to-Digital Converter

Description

The HA19209/210 monolithic bipolar LSIs feature high speed 8-bit A/D conversion with low power dissipation. Digital data output and clock input terminals are compatible with TTL and CMOS. The device is designed for video signal processing applications.

Features

- 8-Bit resolution including overflow
- Low power dissipation: 250mW (typ)
- High speed
- Maximum conversion rate: 30Msps (million samples per second)
- Single power supply: +5V
- Input clock level and digital output signal level compatible with TTL and CMOS (can drive one LS TTL IC)
- Needs no sample and hold circuit
- 28-pin package.

Applications

- Digital television set, digital video tape recorder
- High speed measuring instrumentation
- Industrial equipment with pattern recognition computer

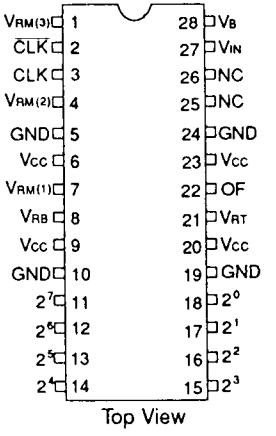
Table 1 shows the difference between HA19209 and HA19210.

Ordering Information

Type No.	Package
HA19209TP	600mil 28-pin plastic DIP (DP-28)
HA19209MP	44-pin plastic QFI (MP-44)
HA19210TP	600mil 28-pin plastic DIP (DP-28)
HA19210MP	44-pin plastic QFI (MP-44)

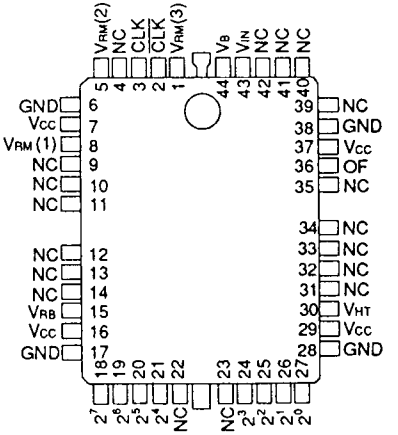
Pin Arrangement

- **HA19209TP,**
- **HA19210TP**



Top View

- **HA19209MP,**
- **HA19210MP**



Top View

Block Diagram

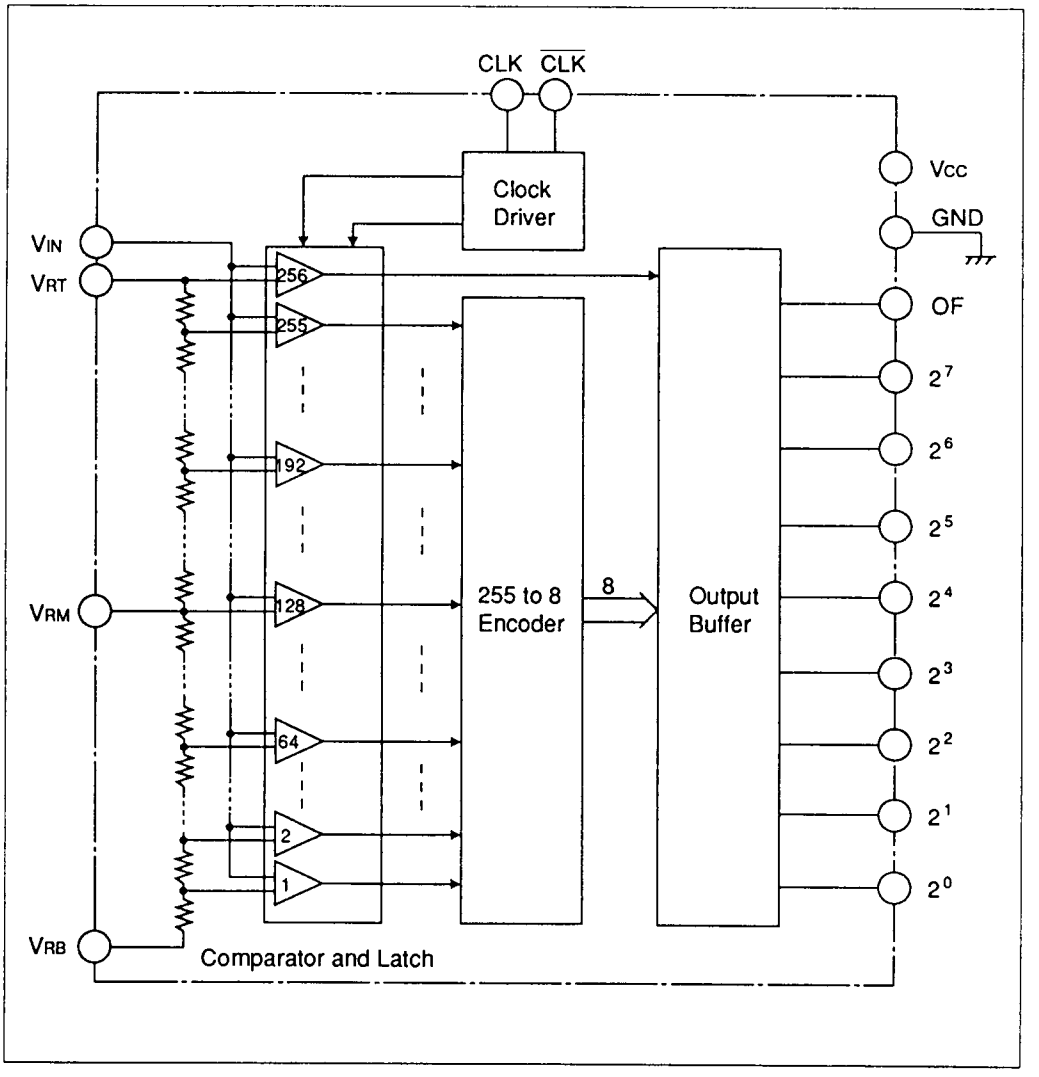


Table 1 Output Code Table

	HA19209						HA19210					
Input Voltage	**OF**	**2^7**	**2^6**	**...**	**2^1**	**2^0**	**OF**	**2^7**	**2^6**	**...**	**2^1**	**2^0**
V_{RB}	0	0	0	...	0	0	0	0	0	...	0	0
V_{RB} + 1 LSB	0	0	0	...	0	1	0	0	0	...	0	1
V_{RB} + 2 LSB	0	0	0	...	1	0	0	0	0	...	1	0
⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
V_{RB} + 127 LSB	0	0	1	...	1	1	0	0	1	...	1	1
V_{RB} + 128 LSB	0	1	0	...	0	0	0	1	0	...	0	0
⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
V_{RT} – 2 LSB	0	1	1	...	1	0	0	1	1	...	1	0
V_{RT} – 1 LSB	0	1	1	...	1	1	0	1	1	...	1	1
V_{RT}	1	1	1	...	1	1	1	0	0	...	0	0

Pin Description (HA19209TP/HA19210TP)

Pin No.	Symbol	Function
1	$V_{RM}(3)$	Reference Voltage Correcting Input
2	$\overline{CLK}$	Clock Input Pin Inversed Phase
3	CLK	Clock Input Pin
4	$V_{RM}(2)$	Reference Voltage Correcting Input
5	GND	Ground Pin
6	Vcc	Power Supply Pin (+5V)
7	$V_{RM}(1)$	Reference Voltage Correcting input
8	V_{RB}	Low Level Reference Input Pin
9	Vcc	Power Supply Pin (+5V)
10	GND	Ground Pin
11	2^7	Digital Output (MSB) Pin
12	2^6	Digital Output Pin
13	2^5	Digital Output Pin
14	2^4	Digital Output Pin
15	2^3	Digital Output Pin
16	2^2	Digital Output Pin
17	2^1	Digital Output Pin
18	2^0	Digital Output (LSB) Pin
19	GND	Ground Pin
20	Vcc	Power Supply (+5V)
21	V_{RT}	High level Reference Input Pin
22	OF	Overflow Output Pin
23	Vcc	Power Supply Pin (+5V)
24	GND	Ground Pin
25	NC	Non Connection Pin
26	NC	Non Connection Pin
27	V_{IN}	Analog Input Pin
28	V_B	Connected to Vcc with 100kΩ

Pin Description (HA19209MP/HA19210MP)

Pin No.	Symbol	Function
1	$V_{RM}(3)$	Reference Voltage Correcting Input
2	$\overline{CLK}$	Clock Input Pin Inversed Phase
3	CLK	Clock Input Pin
4	NC	Non Connection Pin
5	$V_{RM}(2)$	Reference Voltage Correcting input
6	GND	Ground Pin
7	Vcc	Power Supply Pin (+5V)
8	$V_{RM}(1)$	Reference Voltage Correcting Input
9	NC	Non Connection Pin
10	NC	Non Connection Pin
11	NC	Non Connection Pin
12	NC	Non Connection Pin
13	NC	Non Connection Pin
14	NC	Non Connection Pin
15	V_{RB}	Low Level Reference Input Pin
16	Vcc	Power Supply Pin (+5V)
17	GND	Ground Pin
18	2^7	Digital Output (MSB) Pin
19	2^6	Digital Output Pin
20	2^5	Digital Output Pin
21	2^4	Digital Output Pin
22	NC	Non Connection Pin
23	NC	Non Connection Pin
24	2^3	Digital Output Pin
25	2^2	Digital Output Pin
26	2^1	Digital Output Pin
27	2^0	Digital Output (LSB) Pin
28	GND	Ground Pin
29	Vcc	Power Supply Pin (+5V)
30	VRT	High Level Reference Input Pin
31	NC	Non Connection Pin
32	NC	Non Connection Pin
33	NC	Non Connection Pin
34	NC	Non Connection Pin
35	NC	Non Connection Pin
36	OF	Overflow Output Pin
37	Vcc	Power Supply Pin (+5V)
38	GND	Ground Pin
39	NC	Non Connection Pin
40	NC	Non Connection Pin
41	NC	Non Connection Pin
42	NC	Non Connection Pin
43	V_{IN}	Analog Input Pin
44	V_B	Connected to Vcc with 100kΩ

Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+7.0	V
Input Signal Voltage *1	V_{in}	0 to V_{CC}	V
Reference Input Terminal Voltage *1	V_R	0 to V_{CC}	V
Clock Input Voltage *2	V_{CLK}	0 to V_{CC}	V
Power Dissipation	P_T	800	mW
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Notes: *1. V_{in} and V_R should not be lower than 1.2V at the same time.

*2. V_{CLK} and $V_{\overline{CLK}}$ should not be lower than 1.5V at the same time.

Electrical Characteristics (Ta=25°C, V_{CC}=5V, V_{RT}=3.5V, V_{RB}=1.5V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Resolution			8	8	8	bits	V_{CC}=5.0V
Supply Voltage Range		V_{CC}	4.75	5.0	5.25	V	
Reference Terminal	RT	V_{RT}	V_{RB}	3.5	V_{CC} −0.9	V	V_{CC}=5.0V
Voltage Range	RB	V_{RB}	1.2	1.5	V_{RT}	V	V_{CC}=5.0V
	RM	V_{RM}	2.4	2.5	2.6	V	Only for Reference Voltage Correction
Input Signal Voltage Range		V_{in}	V_{RB} −0.1	—	V_{RT} −0.1	V	V_{CC}=5.0V
Input Dynamic Range		V_{RT} − V_{RB}	—	2.0	2.1	Vp-p	
Supply Current		I_{CC}	—	50	90	mA	V_{CC}=5.0V, f_{CLK}=20Msps
Reference Terminal	RT	I_{RT}	—	11	16.6	mA	
Voltage Range	RB	I_{RB}	−16.6	−11	—	mA	
Input Current		I_{in}	—	70	200	µA	V_{in}=4.1V
Input Capacitance		C_{in}	—	40	—	pF	f_{IN}=1MHz, V_{RB}<V_{in}<V_{RT}
High Level Digital Output		V_{OH1}	3.8	4.2	—	V	I_{OH}=−400µA
Voltage		V_{OH2}	3.5	4.0	—	V	I_{OH}=−5mA
Low Level Digital Output Voltage		V_{OL}		0.6	0.75	V	I_{OL}=400µA
Clock Input Current		I_I	−100	—	100	µA	V_{CLK}: 0V to 2.7V

Electrical Characteristics (Ta=25°C, V_{CC}=5V, V_{RT}=3.5V, V_{RB}=1.5V, unless otherwise specified) (cont)

High Level Clock Input Voltage		V_{IH}	2.0	—	V_{CC}	V	
Low Level Clock Input Voltage		V_{IL}	0	—	0.8	V	
Static Linearity	Differential	D.N.L.	−0.5	—	+0.5	LSB	Figure 3-5
Error	Integral	I.N.L	—	—	2.0	LSB_{p-p}	
Maximum Conversion Rate		f_{CLK} max.	20	30	—	Msps	f_{in}=3.58MHz (figure 3-5)
Differential Gain		DG	—	1.0	—	%	f_{CLK}=20Msps,
Differential Phase		DP	—	0.5	—	Degree	NTSC, 40IRE Unlocked (figure 3-5)
Clock Pulse Width		t_{WH}	30	35	—	ns	f_{CLK}=20Msps
		t_{WL}	10	15	—	ns	
Digital Output Propagation Delay		t_{PD}	23	28	33	ns	
Digital Output Rise Time		t_{TLH}	—	8	10	ns	R_L=2kΩ, C_L=10pF
Digital Output Fall Time		t_{THL}	—	20	24	ns	

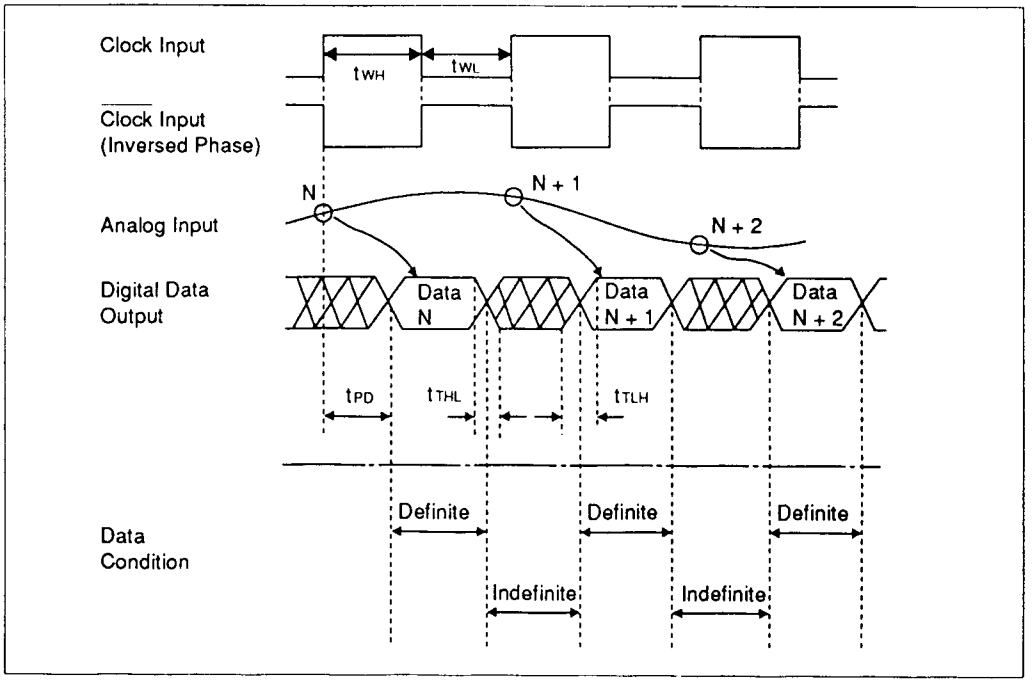


Figure 1 Sample Timing

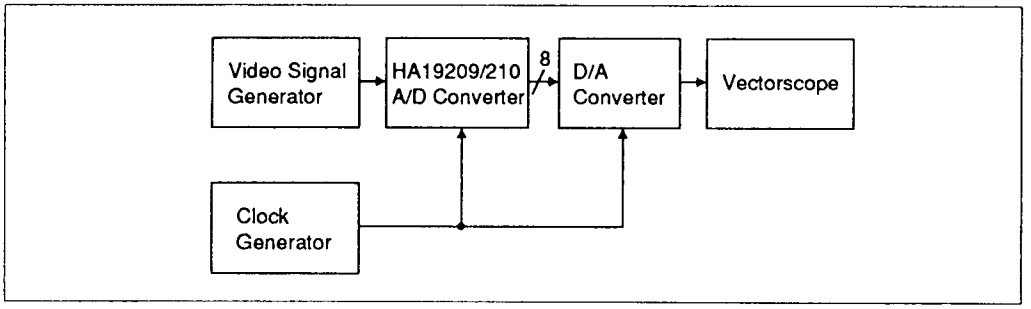


Figure 2 Test Circuit Block Diagram

Differential Gain (DG), Differential Phase (DP)

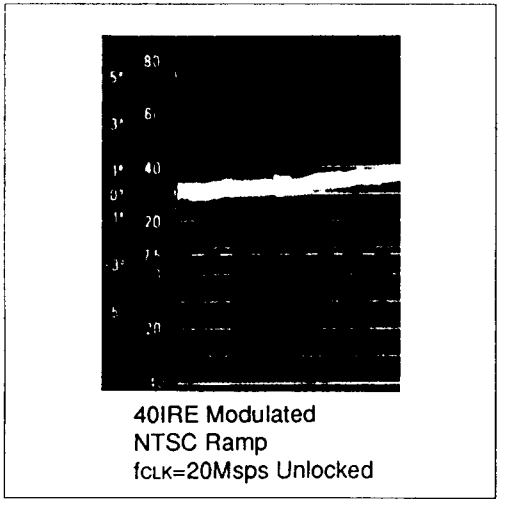


Figure 3 Differential Phase (DP)

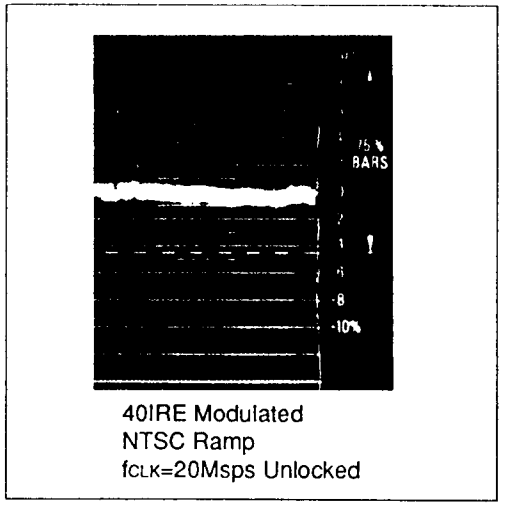


Figure 4 Differential Gain (DG)

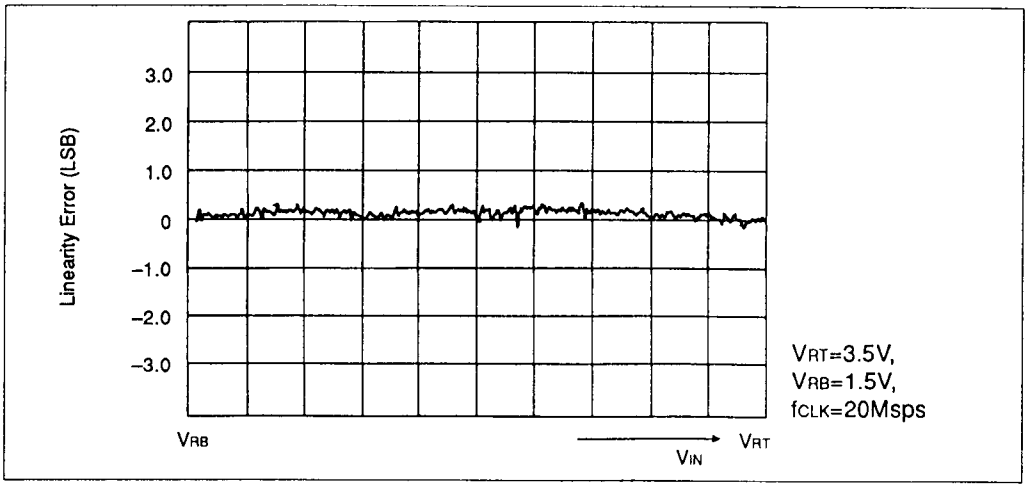


Figure 5 Static Linearity (N.L.)

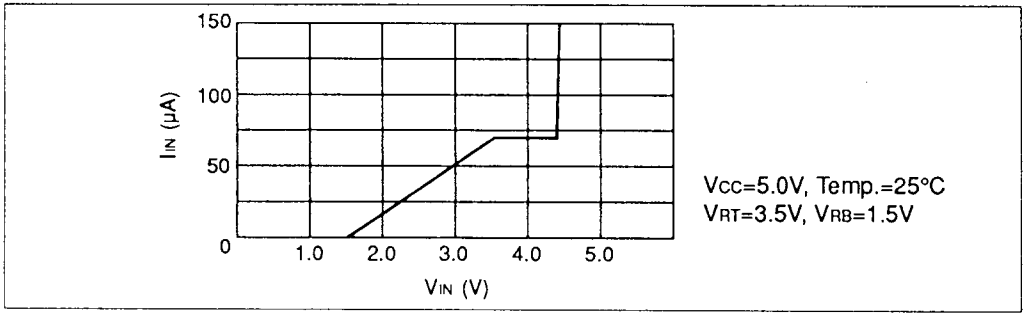


Figure 6 Analog Input Terminal DC Characteristic

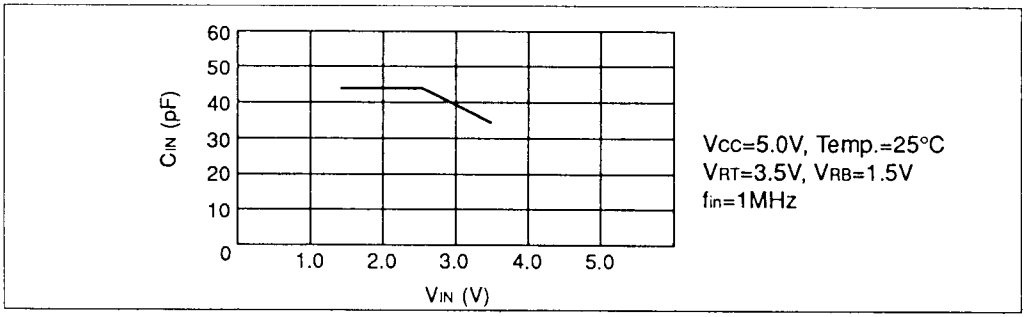


Figure 7 Input Capacitance vs. Input DC Level

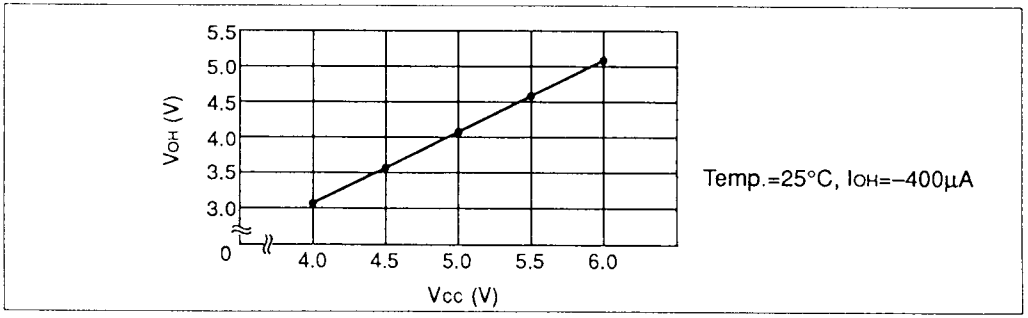


Figure 8 High Level Digital Output vs. Supply Voltage

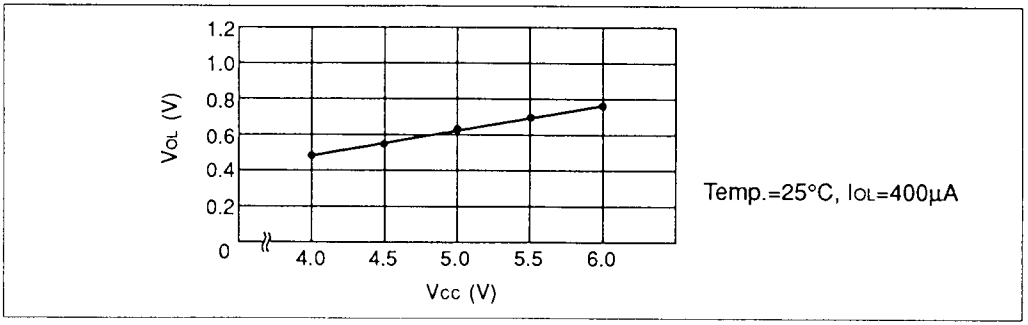


Figure 9 Low Level Digital Output vs. Supply Voltage

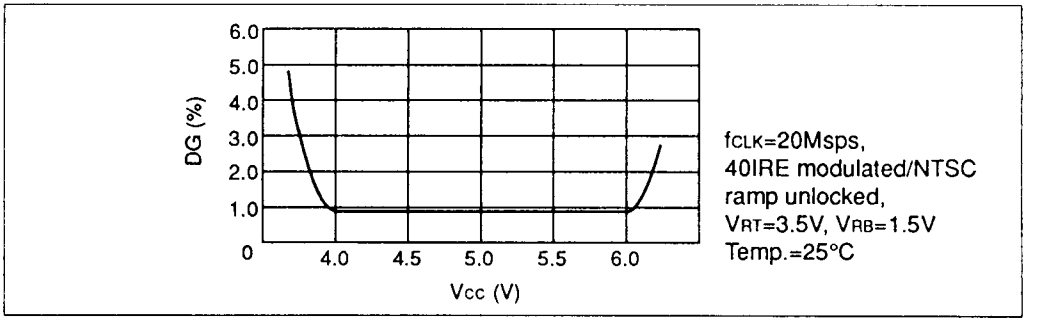


Figure 10 Differential Gain vs. Supply Voltage

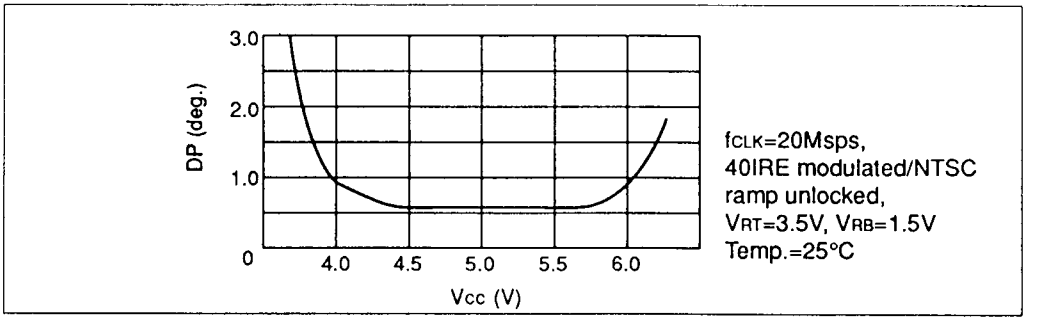


Figure 11 Differential Phase vs. Supply Voltage

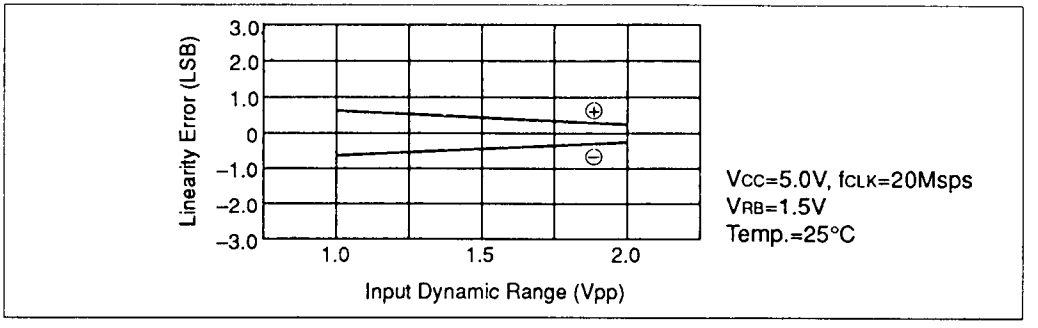


Figure 12 Static Linearity Error vs. Input Dynamic Range