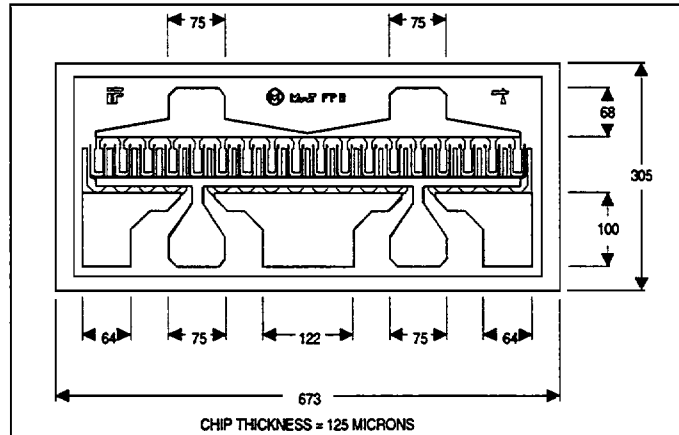


# MwT-8

## 16 GHz High Power GaAs FET

- 0.6 WATT POWER OUTPUT AT 12 GHz
- +40 dBm THIRD ORDER INTERCEPT
- HIGH ASSOCIATED GAIN
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 1200 MICRON GATE WIDTH
- DIAMOND-LIKE CARBON PASSIVATION
- CHOICE OF CHIP AND ONE PACKAGE TYPE

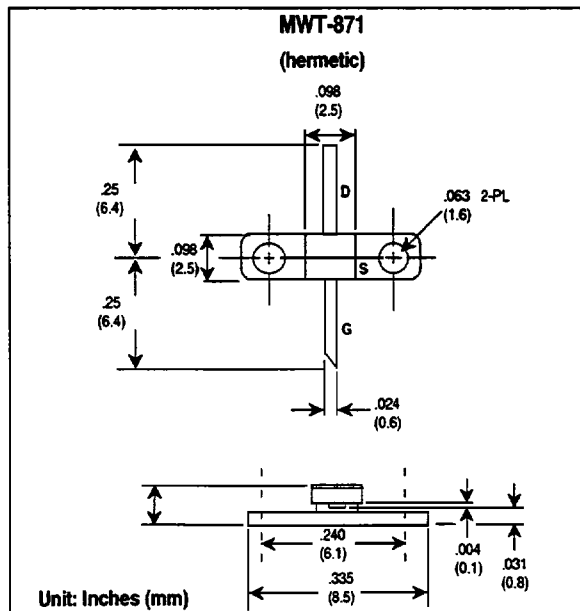


### DESCRIPTION

The MwT-8 GaAs MESFET is ideally suited to narrow-band applications such as cellular telephone, PCN, point-to-point communications links, and other wireless applications as the driver transistor for the output power amplifier. The third-order intercept performance of the MwT-8 is excellent, typically 12 dB above the 1 dB compression point. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

### RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MwT-8 HP MwT-871 HP	
				MIN	TYP
P1dB	Output Power at 1dB Compression VDS=6.0 V IDS= 180 mA	12 GHz	dBm	27.0	28.0
SSG	Small Signal Gain VDS=6.0 V IDS= 180 mA	12 GHz	dB	7.0	7.5
PAE	Power Added Efficiency VDS=6.0 V IDS= 180 mA	12 GHz	%	25	35
IDSS	Recommended IDSS Range for Optimum P1dB		mA		320-440



## DC SPECIFICATIONS AT Ta = 25 °C

\* Overall Rth depends on case mounting

SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
<b>Idss</b>	Saturated Drain Current Vds=4.0 V VGS=0.0 V	mA	120		480
<b>Gm</b>	Transconductance Vds=2.0 V VGS=0.0 V	mS	144	160	
<b>Vp</b>	Pinch-off Voltage Vds=3.0 V IDS=8.0 mA	V		-2.0	-5.0
<b>BVGSO</b>	Gate-to-Source Breakdown Voltage Igs=-0.8 mA, Igd=0	V	-6.0	-12.0	
<b>BVGDO</b>	Gate-to-Drain Breakdown Voltage Igd=-0.8 mA, Igs=0	V	-8.0	-12.0	
<b>Rth</b>	Thermal Resistance* MwT-8 Chip MwT-871	°C/W			45 60*

## MAXIMUM RATINGS AT Ta = 25 °C

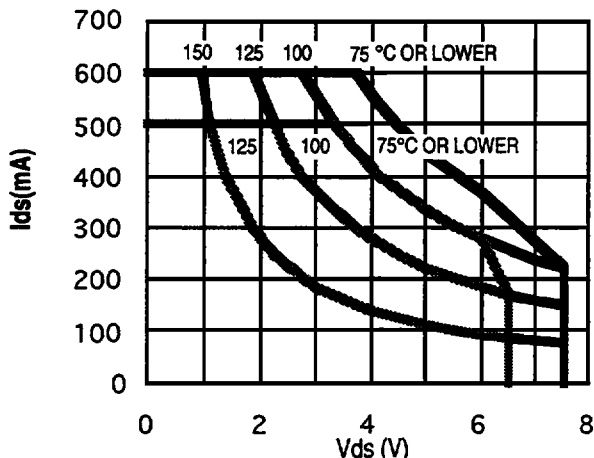
SYMBOL	PARAMETER	UNITS	CONT MAX <sup>1</sup>	ABSOLUTE MAX <sup>2</sup>
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	480	720

- NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.  
2. Exceeding any one of these limits may cause permanent damage.

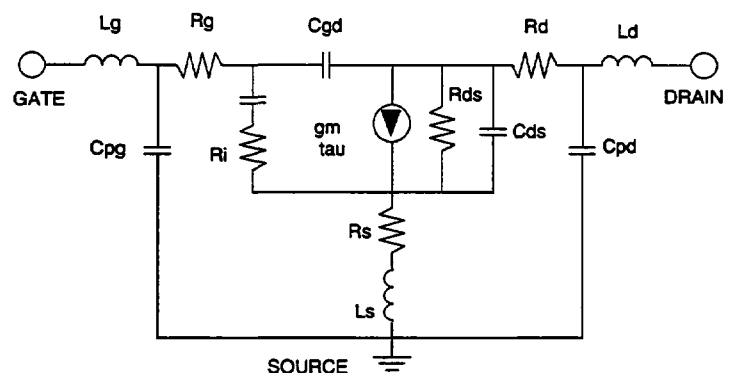
### SAFE OPERATING LIMITS

vs. Case Temperature

— Absolute Maximum  
— Continuous Maximum



### DEVICE EQUIVALENT CIRCUIT MODEL

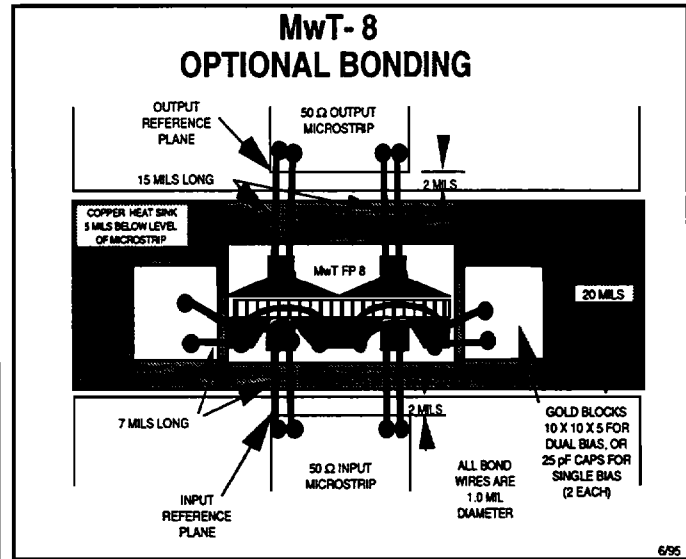
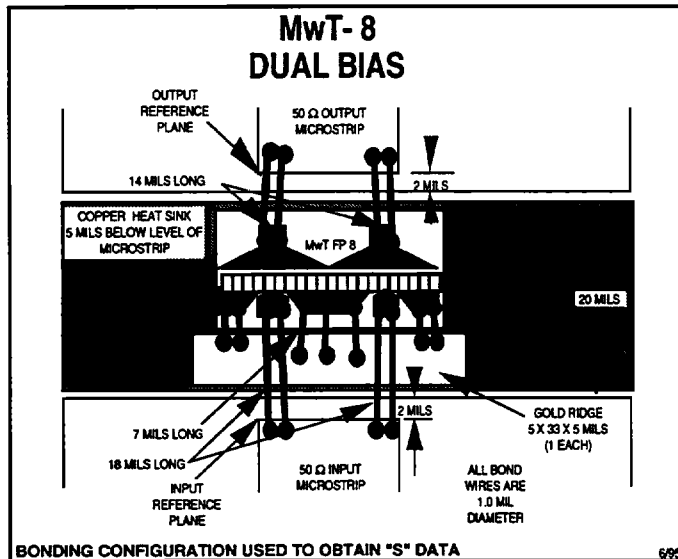


PARAMETER		VALUE	
Gate Bond Wire Inductance	Lg	0.12	nH
Gate Pad Capacitance	Cpg	0.25	pF
Gate Resistance	Rg	0.2	Ω
Gate-Source Capacitance	Cgs	1.4	pF
Channel Resistance	Ri	1.0	Ω
Gate-Drain Capacitance	Cgd	0.05	pF
Transconductance	gm	150.0	mS
Transit time	tau	1.0	psec

PARAMETER		VALUE	
Source Resistance	Rs	0.30	Ω
Source Inductance	LS	0.055	nH
Drain-Source Resistance	Rds	60.0	Ω
Drain-Source Capacitance	Cds	0.10	pF
Drain Resistance	Rd	0.30	Ω
Drain Pad Capacitance	Cpd	0.2	pF
Drain Inductance	Ld	0.10	nH

## RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-8 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.



## BIN SELECTION

Every MwT-8 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS	125	140	160	180	200	220	240-	260-	280-	300-	320-	340-	360-	380-	400-	420-	440	460
(mA)	140	160	180	200	220	240	260	280	300	320	340	360	380	400	420	440	460	480

## BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

## TYPICAL COMMON SOURCE SCATTERING PARAMETERS

MwT-8 CHIP: VDS = 6.0 V, IDS = 0.6 IDSS = 180 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.94	-62.5	7.29	140.3	.037	55.7	.40	-46.1
2.00	.92	-100.8	5.34	117.0	.054	37.6	.34	-75.7
3.00	.91	-126.9	3.99	98.6	.061	24.8	.31	-94.7
4.00	.87	-140.7	3.02	88.3	.060	20.6	.30	-108.2
5.00	.89	-149.8	2.56	80.2	.058	21.3	.30	-115.8
6.00	.92	-159.2	2.21	70.4	.059	18.8	.32	-121.6
7.00	.90	-166.4	1.85	61.9	.059	15.6	.34	-127.2
8.00	.88	-170.4	1.61	56.3	.057	16.1	.36	-131.5
9.00	.90	-174.4	1.45	50.1	.055	14.9	.39	-134.7
10.00	.91	-179.1	1.32	43.5	.047	17.5	.42	-137.1
12.00	.93	174.1	1.10	32.2	.039	30.2	.49	-143.8
14.00	.90	168.3	.90	21.1	.049	37.5	.55	-148.8
16.00	.92	164.1	.76	12.3	.052	39.5	.61	-153.0
18.00	.94	158.5	.66	4.0	.053	49.2	.67	-156.7
20.00	.92	153.3	.56	-3.7	.052	54.3	.71	-157.3

MwT-871HP: VDS = 6.0 V, IDS = 180 mA

FREQUENCY (GHz)	S11		S21		S12		S22		MSG dB
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	
1.00	.88	-79.2	7.13	124.2	.04	39.1	.25	-62.2	22.2
2.00	.81	-125.4	4.88	90.2	.06	17.2	.23	-95.3	19.4
3.00	.79	-153.5	3.53	64.9	.06	3.9	.24	-116.1	17.5
4.00	.80	-173.7	2.79	43.9	.07	-4.5	.27	-133.4	16.1
5.00	.80	168.8	2.31	26.4	.08	-15.3	.32	-150.8	14.6
6.00	.83	154.4	2.00	9.4	.08	-22.5	.36	-166.0	13.8
7.00	.84	140.9	1.85	-6.3	.09	-31.9	.39	179.2	13.0
8.00	.86	129.1	1.69	-20.9	.11	-41.7	.45	163.9	11.8
9.00	.88	116.9	1.72	-38.1	.12	-62.3	.49	147.2	11.5
10.00	.89	103.4	1.60	-54.5	.13	-74.5	.53	131.9	10.8
11.00	.86	90.5	1.54	-72.4	.14	-85.9	.55	117.2	10.6
12.00	.85	83.4	1.51	-86.0	.13	-96.5	.56	104.5	10.4

### DEVICE HANDLING PROCEDURE

- 1) Open package in clean room environment only.
- 2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
- 3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
- 4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
- 5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
- 6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
- 7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
- 8) CAUTION: Handling of chips other than as specified above may cause permanent damage.