

FEATURES	DESCRIPTION
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- 45 ns Multiply-Accumulate Time
- Replaces TRW TMC2210, Cypress CY7C510, IDT 7210L, and AMD Am29510
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DESC SMD No. 5962-88733
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
 - 64-pin Sidebrazed, Hermetic DIP
 - 68-pin Ceramic PGA
 - 68-pin Plastic LCC, J-Lead
 - 68-pin Ceramic LCC

The **LMA1010** and **LMA2010** are high-speed, low power 16-bit multiplier-accumulators. The **LMA1010** and **LMA2010** are functionally identical; they differ only in packaging. Full military ambient temperature range operation is achieved with advanced CMOS technology.

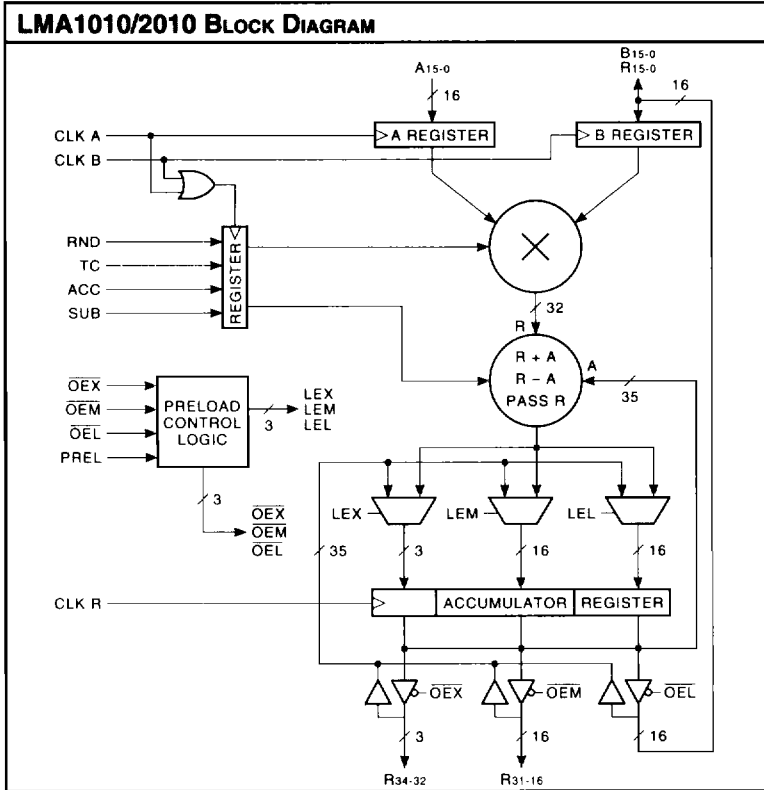
The **LMA1010** and **LMA2010** produce the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched on the rising edges

of **CLK A** and **CLK B** respectively. **RND**, **TC**, **ACC**, and **SUB** controls are latched on the rising edge of the logical OR of **CLK A** and **CLK B**. **TC** specifies the input as two's complement (**TC HIGH**) or unsigned magnitude (**TC LOW**). **RND**, when **HIGH**, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

ACC and **SUB** control accumulator operation. **ACC HIGH** results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of **CLK R**. **ACC** and **SUB HIGH** results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register.

With **ACC LOW**, no accumulation occurs and the next product is loaded directly into the accumulator register.



The **LMA1010/2010** output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is 3 bits long. The output signals **R15-0** and input signals **B15-0** share the same bidirectional pins.

Each output register has an independent output enable control. In addition to providing three-state control of the output buffers, when **OEX**, **OEM**, or **OEL** are **HIGH** and **PREL** is **HIGH**, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of **CLK R**. The interrelation of **PREL** and the enable controls is summarized in Table 1.

Multiplier-Accumulators

16 x 16-bit Multiplier-Accumulator

MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
VCC supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ VCC ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ VCC ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	VCC = Min., I _{OH} = -2.0 mA	3.5			V
V _{OL}	Output Low Voltage	VCC = Min., I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		VCC	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{IX}	Input Current	Ground ≤ V _{IN} ≤ VCC (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ VCC (Note 12)			±20	μA
I _{CC1}	VCC Current, Dynamic	(Notes 5, 6)		12	25	mA
I _{CC2}	VCC Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

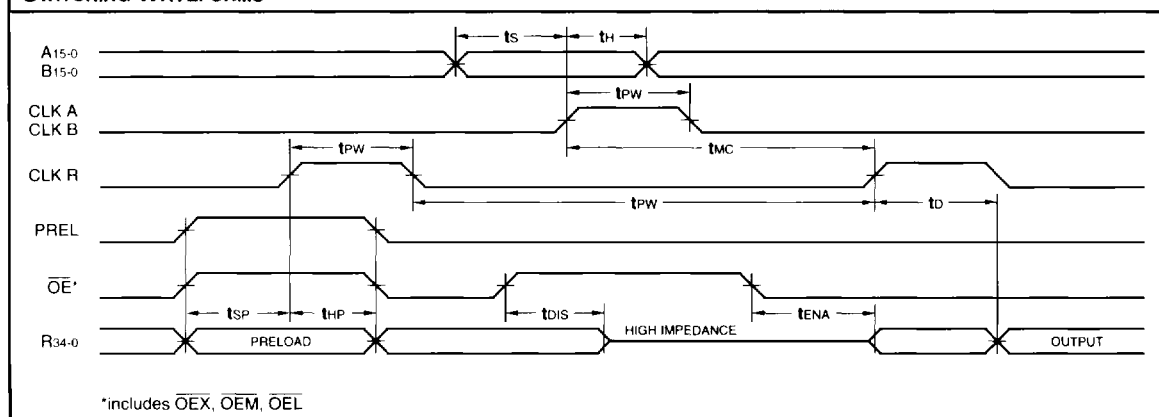
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LMA1010/2010-					
		65		55		45	
		Min	Max	Min	Max	Min	Max
t _{MC}	Clocked Multiply Time		65		55		45
t _{PW}	Clock Pulse Width	15		15		15	
t _S	Input Register Setup Time	15		15		12	
t _H	Input Register Hold Time	2		2		2	
t _{SP}	Preload Setup Time	15		15		12	
t _{HP}	Preload Hold Time	2		2		2	
t _D	Output Delay		30		25		25
t _{ENA}	Three-State Output Enable Delay (Note 11)		30		30		30
t _{DIS}	Three-State Output Disable Delay (Note 11)		30		25		25

MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LMA1010/2010-					
		75		65		55	
		Min	Max	Min	Max	Min	Max
t _{MC}	Clocked Multiply Time		75		65		55
t _{PW}	Clock Pulse Width	20		15		15	
t _S	Input Register Setup Time	20		15		15	
t _H	Input Register Hold Time	2		2		2	
t _{SP}	Preload Setup Time	20		15		15	
t _{HP}	Preload Hold Time	2		2		2	
t _D	Output Delay		35		30		30
t _{ENA}	Three-State Output Enable Delay (Note 11)		35		30		30
t _{DIS}	Three-State Output Disable Delay (Note 11)		35		25		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV2F}{4}$$

where

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tENA/tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For tENABLE and tDISABLE measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

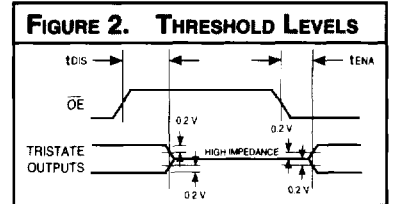
- a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.
- b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.
- c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from

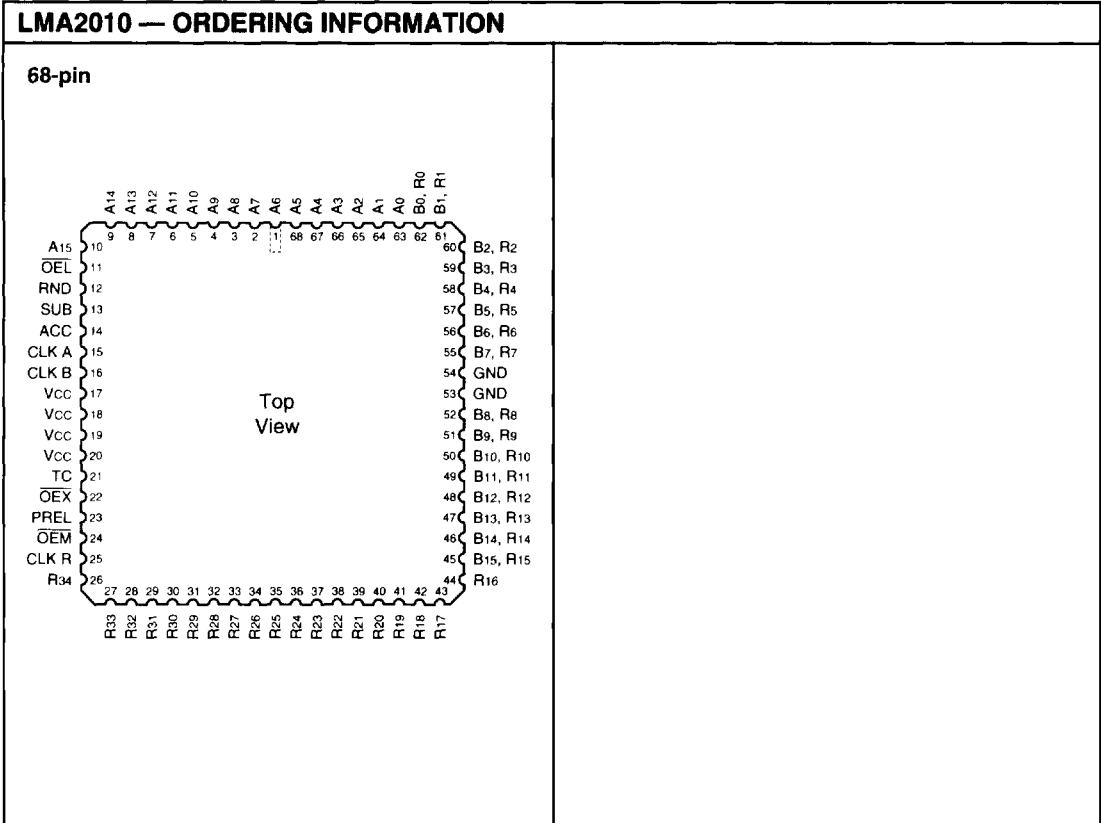
the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.



LMA1010 — ORDERING INFORMATION		
64-pin		68-pin
Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMA1010DC65	LMA1010GC65
55 ns	LMA1010DC55	LMA1010GC55
45 ns	LMA1010DC45	LMA1010GC45
-55°C to +125°C — COMMERCIAL SCREENING		
75 ns	LMA1010DM75	LMA1010GM75
65 ns	LMA1010DM65	LMA1010GM65
55 ns	LMA1010DM55	LMA1010GM55
-55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns	LMA1010DMB75	LMA1010GMB75
65 ns	LMA1010DMB65	LMA1010GMB65
55 ns	LMA1010DMB55	LMA1010GMB55



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Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
0°C to +70°C — COMMERCIAL SCREENING				
65 ns	LMA2010JC65			
55 ns	LMA2010JC55			
45 ns	LMA2010JC45			
-55°C to +125°C — COMMERCIAL SCREENING				
75 ns				
65 ns				
55 ns				
-55°C to +125°C — MIL-STD-883 COMPLIANT				
75 ns		LMA2010KMB75		
65 ns		LMA2010KMB65		
55 ns		LMA2010KMB55		