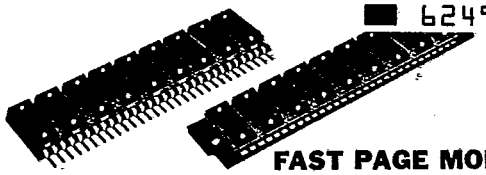

MH1M09A0J-8,-10,-12/ MH1M09A0JA-8,-10,-12

FAST PAGE MODE 1048576-WORD BY 9-BIT DYNAMIC RAM

DESCRIPTION

The MH1M09A0J, JA is 1048576 word x 9 bit dynamic RAM and consists of nine industry standard 1M x 1 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required.

FEATURES

- Performance ranges

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH1M09A0J-8 MH1M09A0JA-8	80	160	1800
MH1M09A0J-10 MH1M09A0JA-10	100	190	1575
MH1M09A0J-12 MH1M09A0JA-12	120	220	1350

- Utilizes industry standard 1M RAMs in SOJ
- 30 pins Single In-line Package
- Single +5V (±10%) supply operation
- Low standby power dissipation 24.8mW (max) CMOS input level
- Low operation power dissipation:
  MH1M09A0J-8, MH1M09A0JA-8 . . . . . 3.46W (max)
  MH1M09A0J-10, MH1M09A0JA-10 . . . 2.97W (max)
  MH1M09A0J-12, MH1M09A0JA-12 . . . 2.48W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF x 9) decoupling capacitors
- 512 refresh cycles every 8ms, A_9 Pin is not need for refresh
- Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{CAS}$ ($\overline{CASP}$) control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.
- Bit nine (DP, QP) controlled by $\overline{CASP}$ is generally used for parity.

PIN CONFIGURATION (TOP VIEW)

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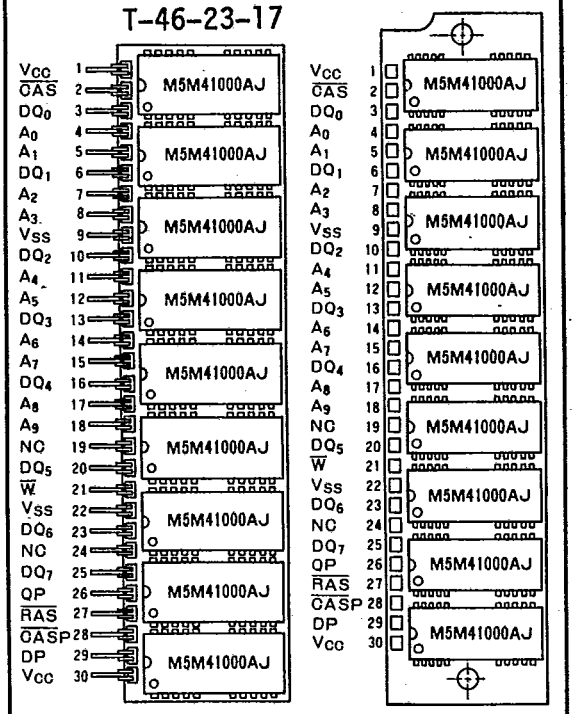


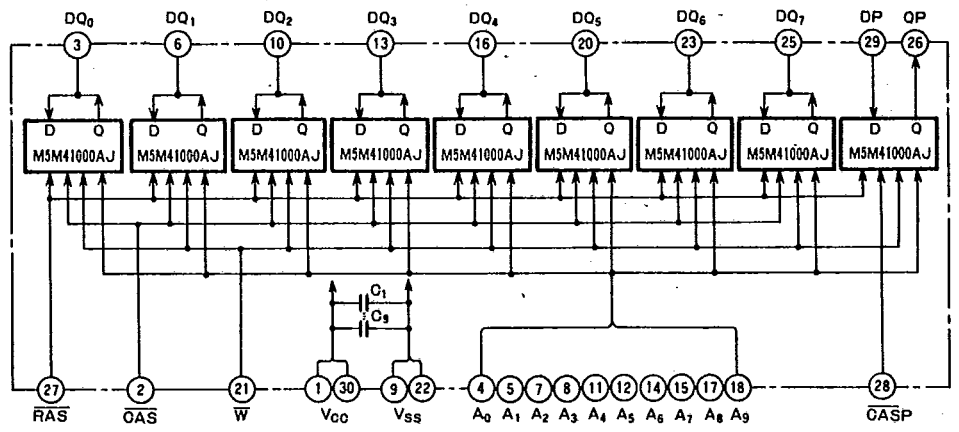
Outline
30N5A(MH1M09A0JA) 30N9A(MH1M09A0J)

NC: NO CONNECTION

APPLICATION

Main memory unit for computers, Refresh memory.

BLOCK DIAGRAM



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FUNCTION

The MH1M09A0J, JA provide, in addition to normal read, and early write operations, a number of other functions, e.g., fast-page mode. $\overline{RAS}$-only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	9	W
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage all inputs	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−20		20	μA
I_I	Input current		0V≦V_{IH}≦6.5V, Other input pins=0V	−90		90	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	MH1M09A0-8	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$=min, output open			630	mA
		MH1M09A0-10				540	
		MH1M09A0-12				450	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CAS}=V_{IH}$, output open			18	mA
			$\overline{RAS}=\overline{CAS}\geqq V_{CC}-0.5$, output open			4.5	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	MH1M09A0-8	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}=min, output open			630	mA
		MH1M09A0-10				540	
		MH1M09A0-12				450	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	MH1M09A0-8	$\overline{RAS}=V_{IL}$, $\overline{CAS}$= cycling t_{PC}=min, output open			540	mA
		MH1M09A0-10				450	
		MH1M09A0-12				360	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH1M09A0-8	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min, output open			630	mA
		MH1M09A0-10				540	
		MH1M09A0-12				450	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_i=25mVrms			60	pF
$C_{(DQ)}$	Data input/data output capacitance				17	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				75	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				75	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				70	pF
$C_{I(\overline{CASP})}$	Input capacitance, $\overline{CASP}$ input				15	pF
$C_{I(DP)}$	Input capacitance				15	pF
$C_{O(DP)}$	Output capacitance	V_O=V_{SS}, f=1MHz, V_i=25mVrms			12	pF

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SWITCHING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
			Min	Max	Min	Max	Min	Max	
t_{OAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		25		30	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		80		100		120	ns
t_{CAA}	Column address access time	(Note 6, 9)		40		50		60	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		45		55		65	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.

8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.

9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.

10: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

11: $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 20\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Early Write, Fast-Page Mode Cycles)

(Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 12, 13)

Symbol	Parameter		Limits						Unit
			MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		70		80		90		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	25	60	25	75	25	90	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	35		35		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	20	40	20	50	20	60	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	15	0	20	0	25	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		15		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		20		20		20		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 12: The timing requirements are assumed t_T = 5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in note 7, 9.

15: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for t_{CP} of fast page mode cycle.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(min)}$, access time is assumed by t_{CAA} for read cycle.

18: $t_{ASC(max)}$ is specified as a reference point only of address access time.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

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Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	25	10000	30	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		25		30		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		40		50		60		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 20: Either t_{RCH} or t_{RRH} must be satistied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter		Limits						Unit
			MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width		80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	25	10000	30	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		25		30		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 21)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		20		25		ns
t_{WP}	Write pulse width		15		20		25		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low		15		20		25		ns

Note 21 : When $t_{WCS} < t_{WCS(min)}$, Data input will contend with the data output because of the common I/O feature.

Fast Page Mode Cycle (Read, Early write Cycles)

Symbol	Parameter		Limits						Unit
			MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode cycle time		50		60		70		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read, write cycle		130	100000	160	100000	185	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle		20	10000	25	10000	30	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 22)	10	25	10	25	15	30	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		25		30		ns

Note 22 : $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)

Symbol	Parameter	Limits						Unit
		MH1M09A0-8		MH1M09A0-10		MH1M09A0-12		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		20		25		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 23 . Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

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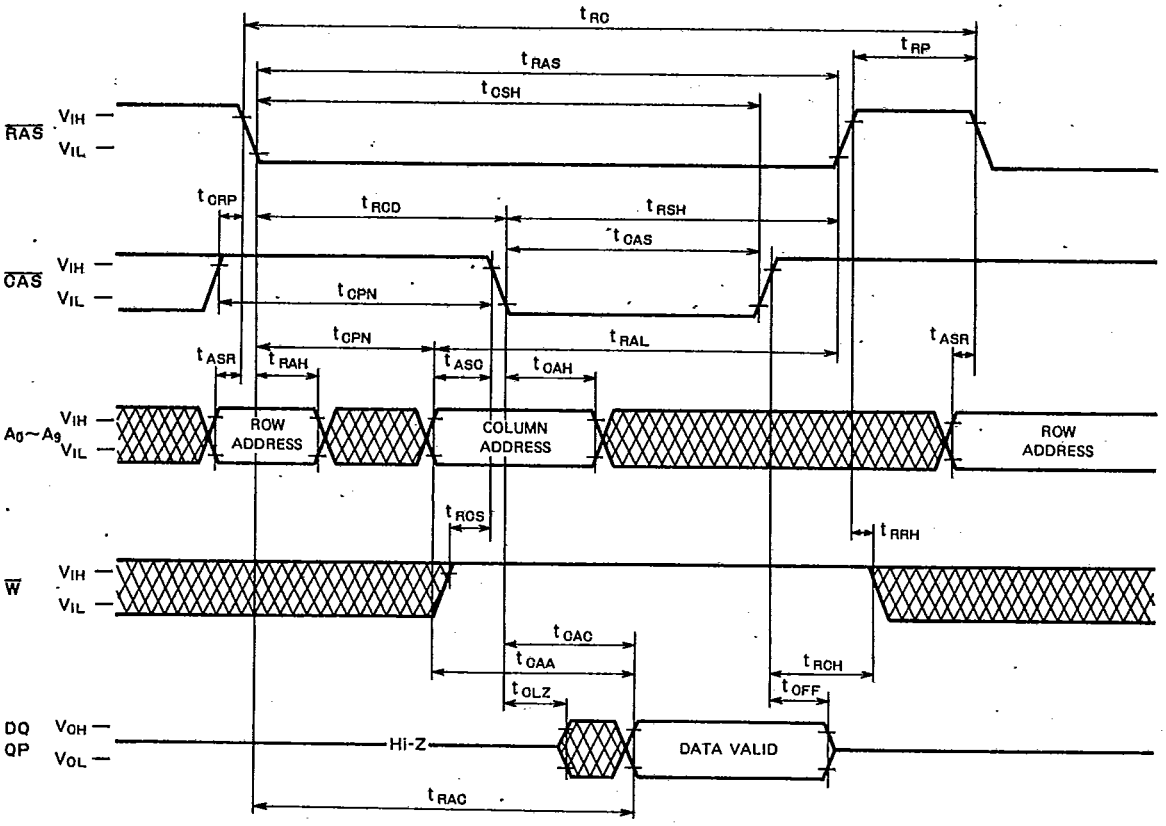
Timing Diagrams (Note 24)

Read Cycle



Note 24 Indicates the don't care input.

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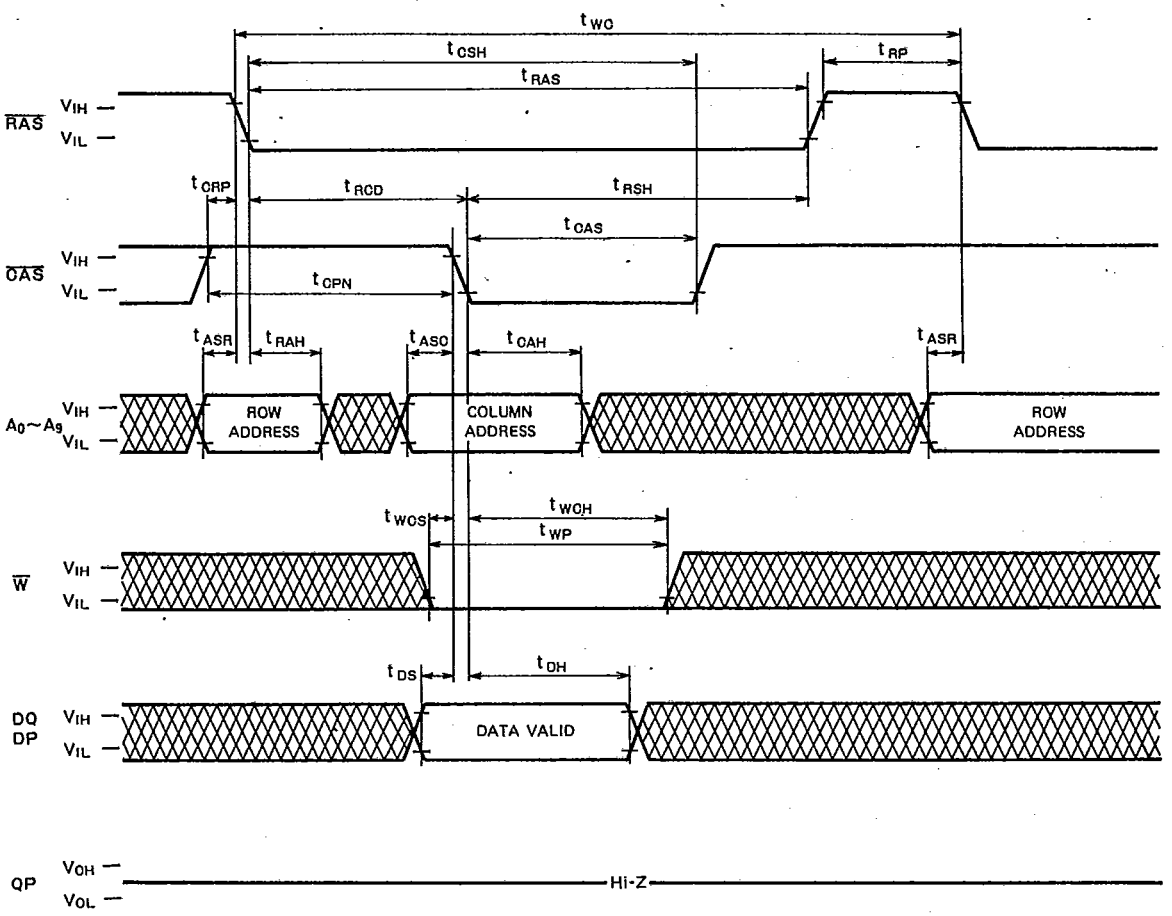
Early Write Cycle



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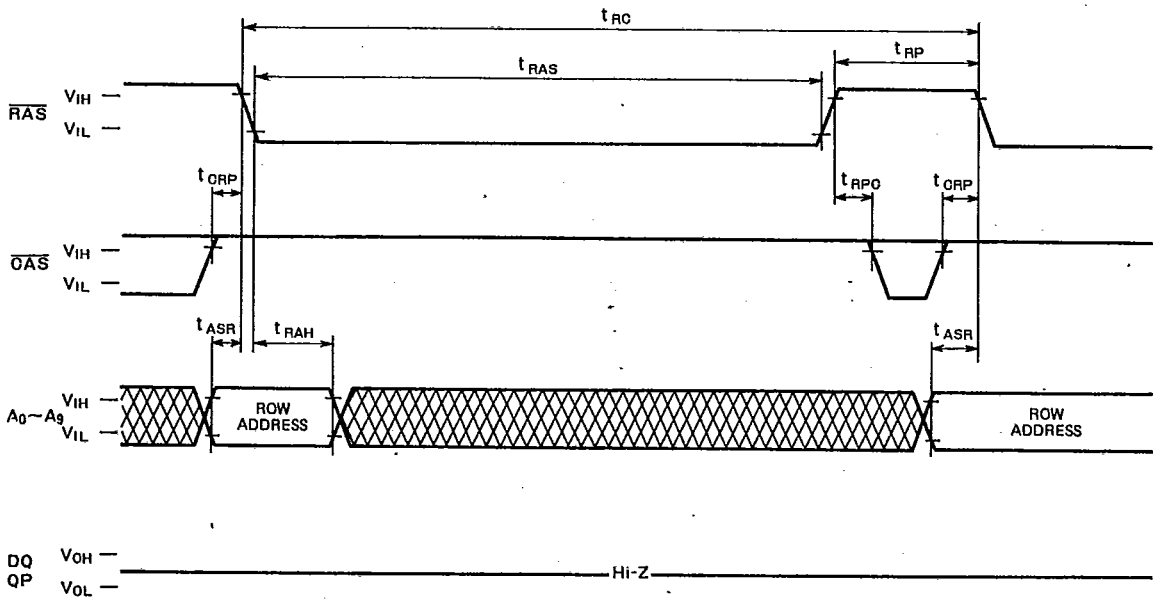
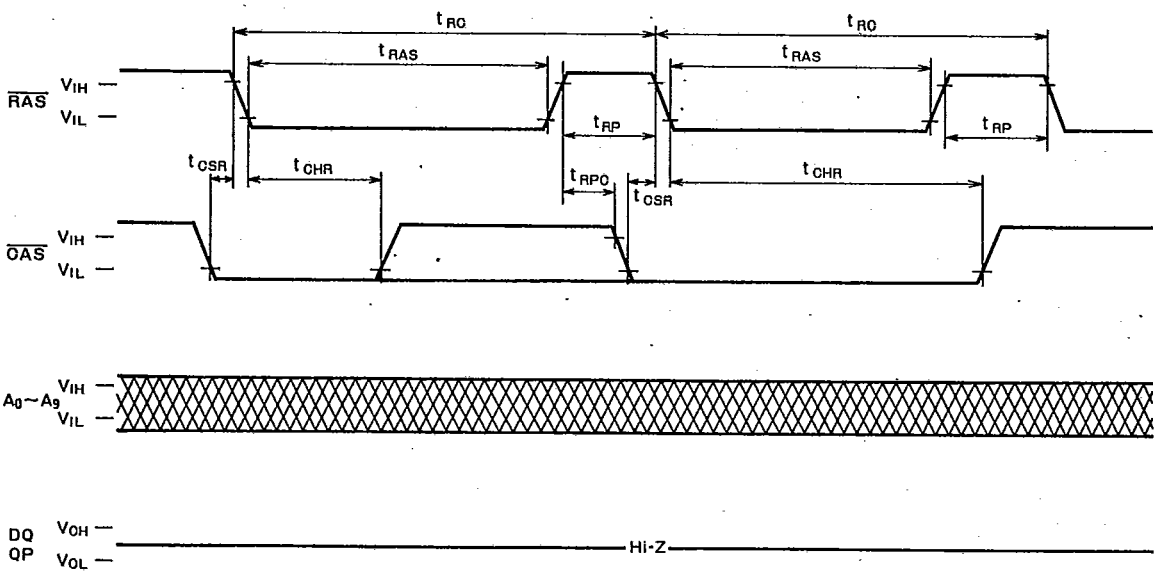
$\overline{RAS}$ only Refresh Cycle (Note 25)



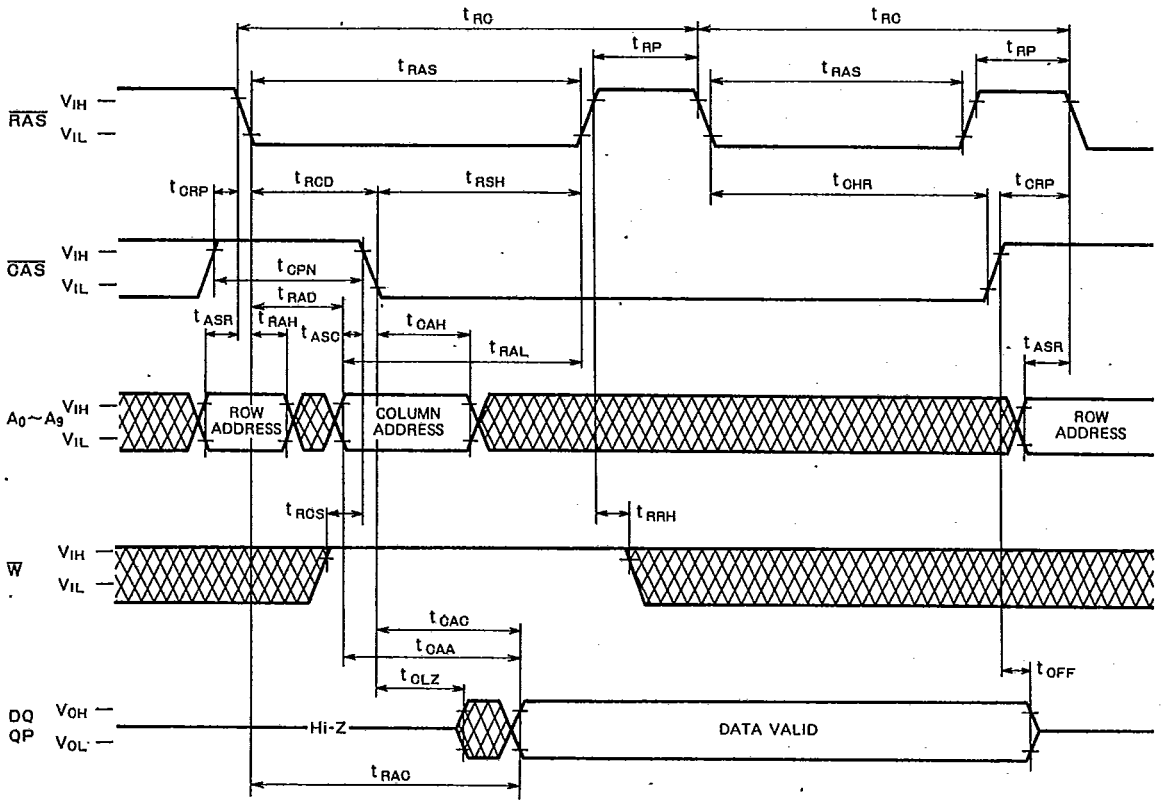
Note 25 : $\overline{W}$, DP = don't care, A_9 may be V_{IH} or V_{IL}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)



Note 26 : $\overline{W}$, DP = don't care

Hidden Refresh Cycle



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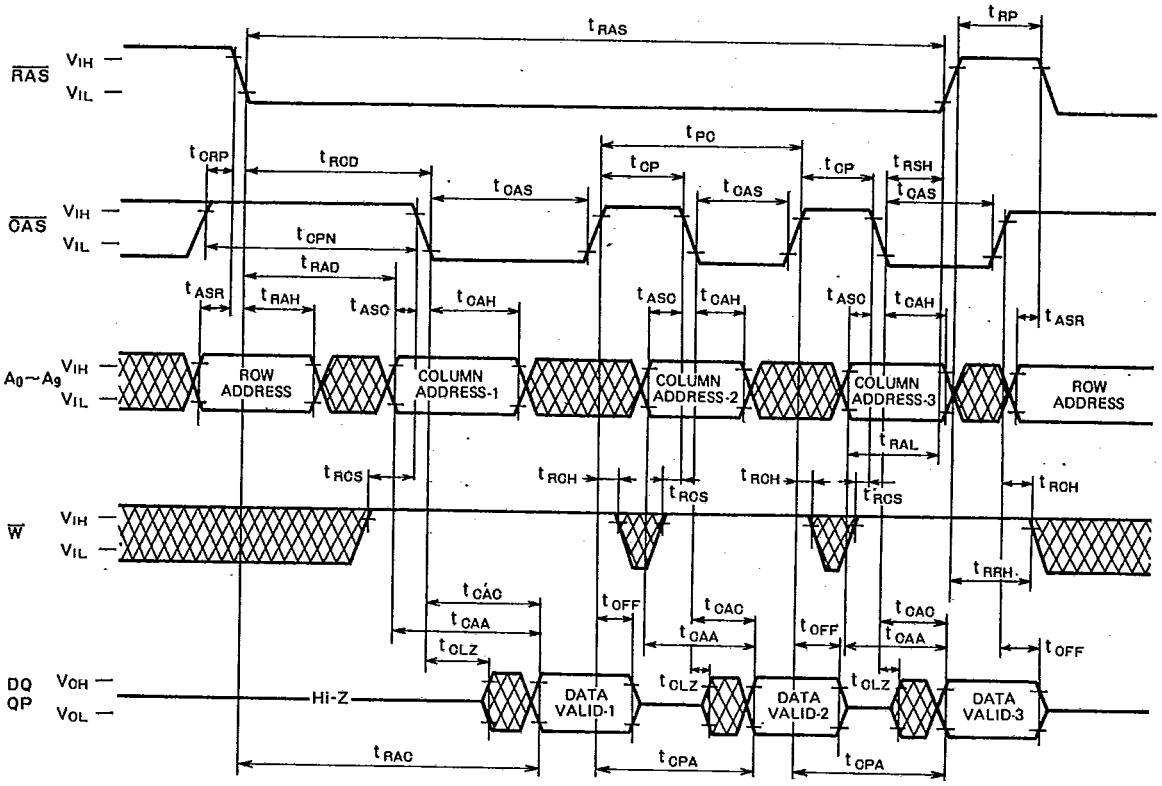
Fast-Page-Mode Read Cycle



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Fast-Page-Mode Early Write Cycle