

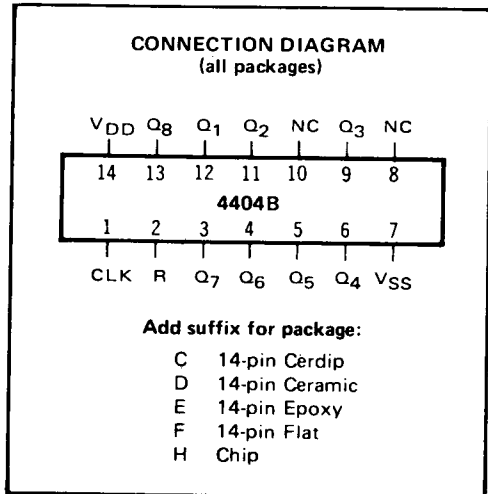
CMOS 8-STAGE BINARY COUNTER

FEATURES

- ◆ 8-Stage Synchronous Counter
- ◆ Buffered Outputs from all 8 Stages
- ◆ Direct Reset
- ◆ Fully Static Operation – DC to 8MHz @ 10Vdc

DESCRIPTION

The 4404B consists of eight synchronous, single-phase clocked counting stages, with the Q output of each stage accessible. The counter is reset to all "zeroes" by a high level on the Reset line. Each stage of the counter utilizes a master-slave flip-flop configuration. The state of the counter is advanced one step in binary order on the negative-going transition of the input clock pulse.



TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

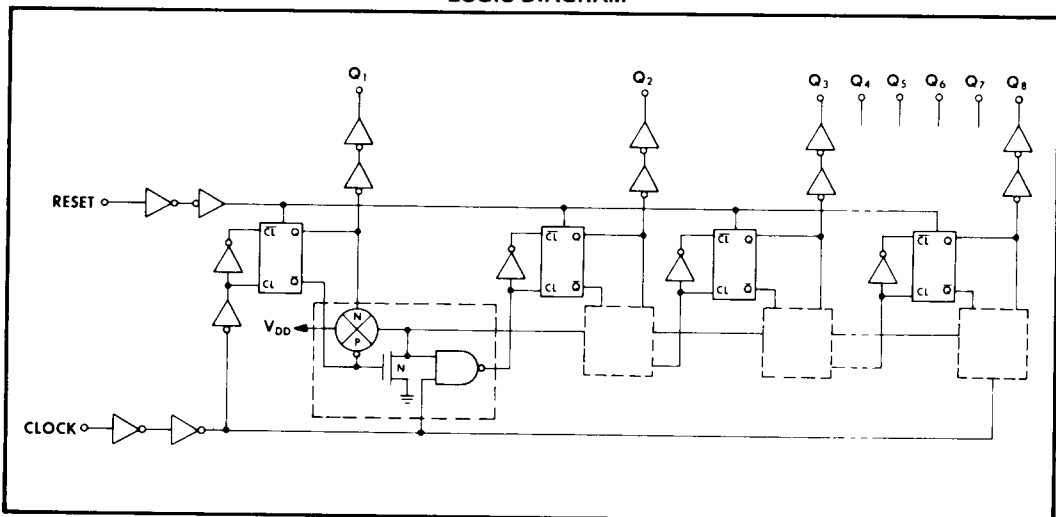
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc
 Operating Temperature T_A
 C, D, F, H Device -55 to +125 °C
 E Device -40 to +85 °C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS ¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μA _{dc}
			—	10	—	0.1	10	—	300	
			—	15	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
² T_{LOW} = -55°C for C, D, F, H device.
 = -40°C for E device.
 T_{HIGH} = +125°C for C, D, F, H device.
 = + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION					
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	250	ns
		10	—	125	
		15	—	100	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	ns
		10	—	50	
		15	—	40	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	125	ns
		10	—	65	
		15	—	50	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2.0	4.0	MHz
		10	4.0	8.0	
		15	5	10	
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	—	μs
		10	5	—	
		15	3	—	
RESET OPERATION					
PROPAGATION DELAY TIME	t _{PHL}	5	—	175	ns
		10	—	75	
		15	—	60	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	100	ns
		10	—	50	
		15	—	40	
RESET REMOVAL TIME	t _{rem}	5	—	200	ns
		10	—	90	
		15	—	65	

