November 1990
PRELIMINARY

Micro Linear

ML4415, ML4415R
ML4416, ML4416R

15 Channel Read/Write Circuit

GENERAL DESCRIPTION

The ML4415, ML4416 devices are bipolar monolithic read/write circuits designed for use with fixed disk ferrite center-tapped recording heads. They provide a low noise read path, write current control, and data protection circuitry for all channels.

These multiplexed read/write data channels exhibit features not found in similar read/write circuits such as improved write current stability and elimination of write current "glitches" during power up.

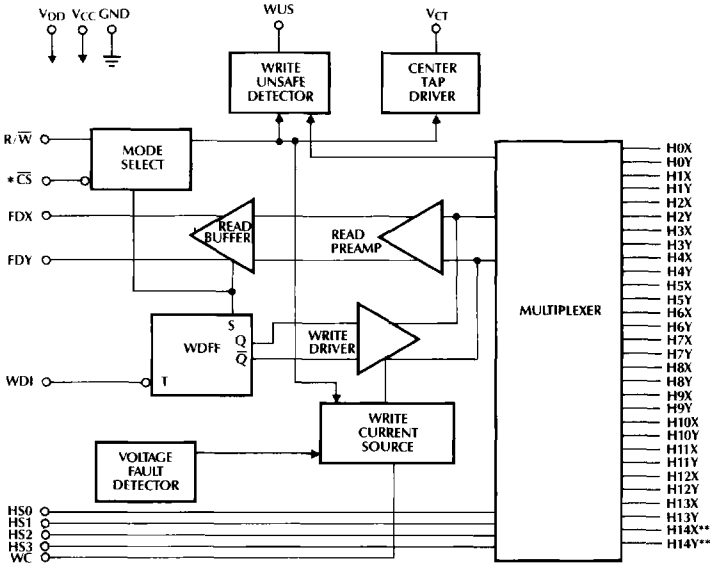
The ML4416 has fourteen read/write data channels and a chip select pin. The chip select pin allows additional read/write circuits in the system by enabling or disabling a particular chip. The ML4415 has fifteen read/write data channels and no chip select pin.

The ML4415R and ML4416R versions include on-chip damping resistors.

FEATURES

- Write current disable during power up
- Enhanced write current stability
- Designed for center-tapped ferrite heads
- ML4415 provides 15 read/write channels
- ML4416 — easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals
- Programmable write current source
- +5V, +12V power supplies

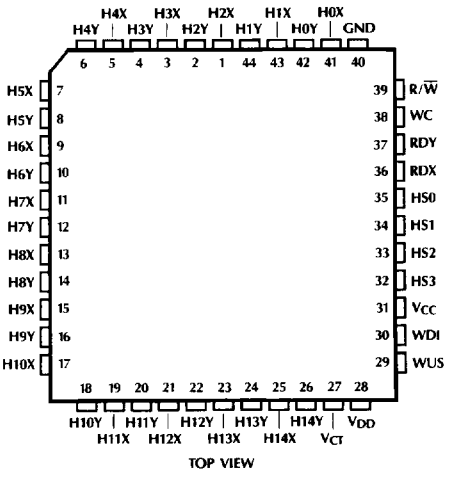
BLOCK DIAGRAM



* ML4416 ONLY
** ML4415 ONLY

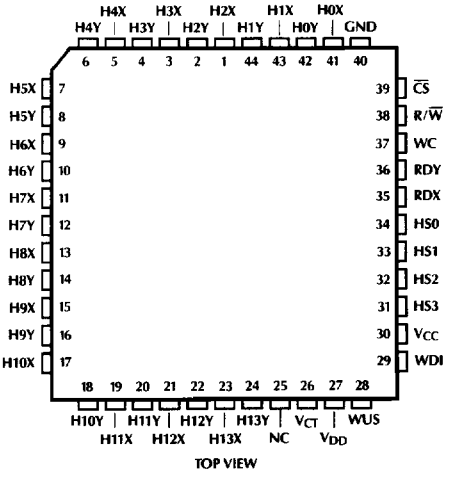
PIN CONNECTIONS

ML4415CQ, ML4415RCQ
44-Pin PCC



TOP VIEW

ML4416CQ, ML4416RCQ
44-Pin PCC



TOP VIEW

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PIN DESCRIPTION

NAME	FUNCTION
HS0–HS3	Head Select (14 heads for the ML4416, and 15 heads for ML4415).
$\overline{CS}$	Chip Select (low level enables, ML4416 only)
R/W	Read/Write (high level select Read Mode)
WUS	Write Unsafe, open collector output (high level indicates an unsafe writing condition)
WDI	Write Data In (negative transition toggles head current direction)

NAME	FUNCTION
H0X–H14X	X head connections
H0Y–H14Y	Y head connections
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
V_{DD}	+12 volts
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14V_{DC}
- $V_{DD}2$ ..... −0.3 to 14V_{DC}
- V_{CC} ..... −0.3 to 6V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ... −0.3 to V_{CC} +0.3V_{DC}
- Head Ports ..... −0.3 to $V_{DD}1$ +0.3V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14V_{DC}

Write Current (I_W) 60mA

Output Current
- Read Data (RDX, RDY) ..... −10mA
- Center Tap Current (I_{CT}) ..... −60mA
- Write Unsafe (WUS) 12mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 135°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12V ± 10%
- V_{CC} ..... 5V ± 10%

Head Inductance
- L_H ..... 5 to 15μH

Damping Resistor (R_D, ML4415R or ML4416R) .. 500 to 2000Ω

RCT Resistor (1/4 Watt) ..... 120Ω ± 5%

Write Current (I_W) ..... 10 to 40mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = V_{DD}2 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $R_{CT} = 120\Omega \pm 5\%$, $I_W = 40mA$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode		31	35	mA
		Write Mode		26	30	mA
I_{DD}	V_{DD} Supply Current	Read Mode		29	35	mA
		Write Mode		17+I_W	20+I_W	mA
		Idle Mode		17	20	mA
P_D	Power Dissipation	Read Mode		550	655	mW
		Write Mode I_W = 40mA, R_{CT} = 0Ω		890	960	mW
		Idle Mode		378	455	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2			V_{DC}
V_{IL}	Low Voltage				0.8	V_{DC}
I_{IH}	High Current	V_{IH} = 2.0V			100	μA
I_{IL}	Low Current	V_{IL} = 0.8V	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	I_{OL} = 8mA (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	V_{OH} = 5V (Unsafe)			100	μA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{HCW}	Head Current (per side)	Write Mode $0 \leq V_{CC} \leq 3.7V$ $0 \leq V_{DD}1 \leq 8.7V$	−200	0.15	200	μA
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		40	mA
K	Write Current Constant		2.375	2.5	2.625	
V_{HD}	Differential Head Voltage Swing		7.0	10.2		V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance			8.8	15	pF
R_{OD}	Differential Output Resistance	ML4415, 4416	10k			Ω
		T_J = 25°C ML4415R, 4416R	600		960	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250	490		kHz
A_I	I_{WC} to Head Current Gain			0.99		mA/mA
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	V_{IN} = 1mV$_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	85	106	115	V/V
DR	Dynamic Range	DC Input Voltage (V_I) Where Gain Falls 10%, $V_{IN} = V_I + 0.5mV_{P-P}$ @ 300kHz	−3	±7	+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5Ω$, V_{IN} = 1mV$_{P-P}$	30	40		MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, L_H = 0, R_H = 0		1.2	1.5	nV/√Hz
C_{IN}	Differential Input Capacitance	f = 5MHz		14	20	pF
R_{IN}	Differential Input Resistance	f = 5MHz, T_J = 25°C ML4415, 4416	2k	15K		Ω
		V_{IN} = 6mV$_{P-P}$ ML4415R, 4416R	460		860	Ω
I_{HCR}	Head Current (per side)	Read or Idle Mode $0 \leq V_{CC} \leq 5.5V$ $0 \leq V_{DD}1 \leq 13.2V$	−200		200	μA
I_{IN}	Input Bias Current (1 side)			8.5	45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT}$ + 100mV$_{P-P}$ @ f = 5MHz	50	77		dB
PSRR	Power Supply Rejection Ratio	100mV$_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: V_{IN} = 100mV$_{P-P}$ @ 5MHz and Selected Channel: V_{IN} = 0mV$_{P-P}$	45	57		dB
V_{OS}	Output Offset Voltage	Read Mode	−460	±29	+460	mV
		Write or Idle Mode	−20	±1	+20	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	4.5	5.5	6.5	V
		Write or Idle Mode		5.6		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	(RDX, RDY) = 6V Write or Idle Mode	−100	±15	100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	±2.1	±2.7		mA

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ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1$ = 12V ± 10%, V_{CC} = 5V ± 10%, R_{CT} = 120Ω ± 5%, I_W = 35mA, L_H = 10μH, R_D = 750Ω (ML4415, ML4416), f_{DATA} = 5MHz, 0°C ≤ T_A ≤ 70°C (Notes 2 and 3)

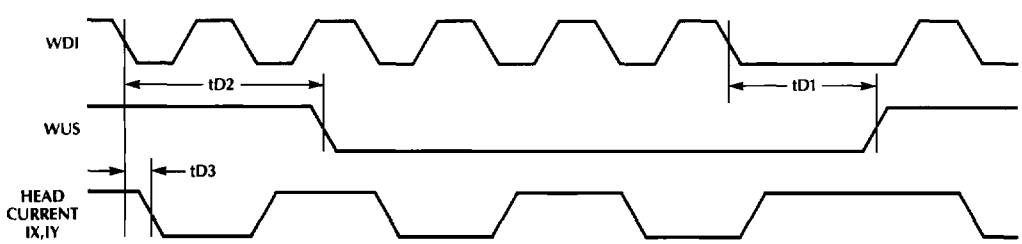
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output		.105	1	μs
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.036	1	μs
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope		.165	1	μs
t_{WI} or t_{RI}	$\overline{CS}$ to Unselect Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current		.084	1	μs
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope		.045	1	μs
tD1	Safe to Unsafe Write Unsafe Delay	I_W = 35mA	1.6	3.9	8	us
tD2	Unsafe to Safe Write Unsafe Delay	I_W = 35mA		.387	1	us
tD3	Prop. Delay Head Current	L_H = 0, R_H = 0 From 50% points		23	25	ns
	Asymmetry Head Current	WDI has 50% Duty Cycle and 1nS Rise/Fall Time		0.9	2	ns
	Rise/Fall Head Current	10% and 90% Points		5	20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_j) should not exceed 135°C.

TIMING DIAGRAM



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

For any selected head, the ML4415/4416 functions as a read amplifier when in the Read mode, or as a write current switch when in the Write mode. Pins HS0, HS1 and HS2 determine head selection while pin R/W controls the Read/Write mode. A detected "write-unsafe" condition is indicated by pin WUS.

READ MODE

When the ML4415, 4416 is in the Read Mode, it operates as a low-noise differential amplifier on the selected channel. In Read mode the write data flip-flop is set and both the write unsafe detector and the write current source are deactivated. The center tap voltage is also lowered. Pins RDX and RDY provide differential emitter follower outputs which are in phase with the X and Y head input pins.

Note that during the Read or Chip Deselect mode the internal write current is deactivated, thus making external write current gating unnecessary.

WRITE MODE

The ML4415, 4416 operates as a write-current switch when in the Write mode. Write current magnitude is determined by the following relationship:

$I_W = K/R_{WC}$

Where: K = Write Current Constant

R_{WC} = Resistance connected between pin WC and GND.

The head current is toggled between the X and Y side of the selected head by a negative transition WDI (Write Data Input). When switching the ML4415, 4416 to write mode, the WDFF (Write Data Flip-Flop) is initialized to pass write current through the X-side of the head.

The ML4415, 4416 exhibit enhanced write current stability, compared to similar read/write circuits, which reduces the problem of oscillation. This is a result of increased internal write current compensation. Also, write current "glitches" during power-up, common in similar read/write circuits, are eliminated with an exclusive write current disabling function.

The WUS (Write Unsafe) pin is an open collector output that gives a logic high level for any of the following unsafe write conditions:

- Open head
- Open head center-tap
- Too low WDI frequency
- Read mode selected
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

The ML4415, 4416 also offers a voltage fault detection circuit that prevents write current during power-loss or power-up.

Table 1.

Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	H0
0	0	0	1	H1
0	0	1	0	H2
0	0	1	1	H3
0	1	0	0	H4
0	1	0	1	H5
0	1	1	0	H6
0	1	1	1	H7
1	0	0	0	H8
1	0	0	1	H9
1	0	1	0	H10
1	0	1	1	H11
1	1	0	0	H12
1	1	0	1	H13
1	1	1	0	H14*

* ML4415 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

Table 2.

Mode Select

$\overline{CS}$**	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

** ML4416 only
0 = Logic Level Low
1 = Logic Level High
X = Don't Care

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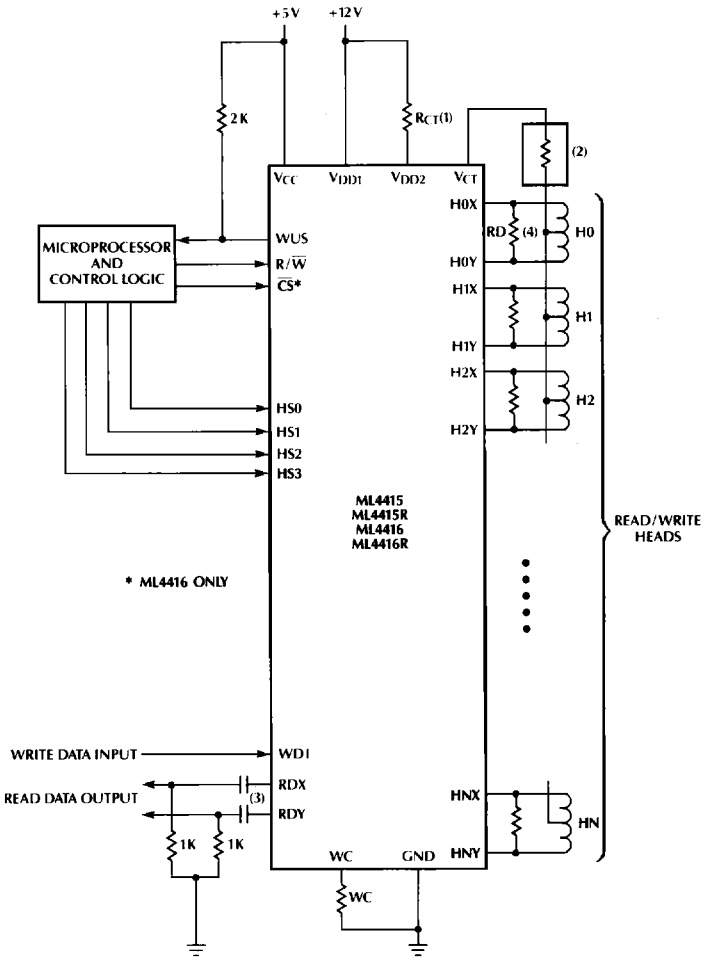
TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 120 (40/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite head optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20pF maximum. RDX and RDY output current must be limited to 100μA.
4. Damping resistors not required on ML4415R, 4416R.

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML4415CQ	MOLDED PCC (Q44)	15
ML4415RCQ	MOLDED PCC (Q44)	15
ML4416CQ	MOLDED PCC (Q44)	14 with $\overline{CS}$
ML4416RCQ	MOLDED PCC (Q44)	14 with $\overline{CS}$

May 1992
PRELIMINARY

Micro Linear

ML4417/ML4427

Zoned Bit Recording Circuit

GENERAL DESCRIPTION

The ML4417/27 is a bipolar monolithic integrated circuit that simplifies the design of zoned bit recording systems in hard disk drives. It contains a VCO capable of operating at frequencies up to 95 MHz, a charge pump, and the active electronics required for a loop filter to form a variable rate data encoding and decoding system.

The ML4417/27 also includes a code clock output and the dividers required for an interface clock output whose frequency is equal to the code clock output frequency divided by 1.5. This feature simplifies the use of RLL (1, 7) coding for improved storage density.

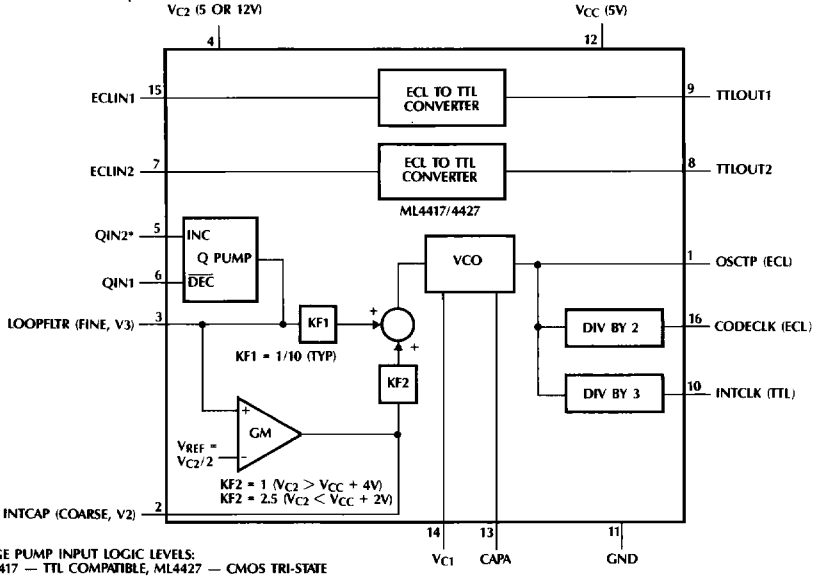
In addition, the ML4417/27 includes two uncommitted ECL to TTL level translators to simplify interfacing with TTL-based systems. The ML4417/27 is designed for operation from 12V and 5V supplies, but may be operated from a single 5V supply if desired.

The ML4417 has TTL-compatible logic input levels on the charge pump, and the ML4427 has a charge pump control input, which, when driven by a CMOS tri-state output, eliminates one logic interface line to the circuit.

FEATURES

- Wide VCO Range (3:1 Range to 95 MHz)
- Allows RLL (1, 7) or (2, 7) Encoding
- SO-16 (Narrow) Packaging
- Coarse and Fine VCO Control Inputs
- Two Uncommitted ECL to TTL Converters
- 12V, 5V or Single 5V Operation

BLOCK DIAGRAM



* CHARGE PUMP INPUT LOGIC LEVELS:
ML4417 — TTL COMPATIBLE, ML4427 — CMOS TRI-STATE