

# T6L08

## GATE DRIVER FOR TFT LCD PANELS

The T6L08 is a 240-channel-output gate driver for TFT LCD panels. In addition to high-voltage operation (liquid crystal drive voltage = max 42 V), this device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, this device can be used for various TFT LCD panel drive systems.

The T6L08 offers high integration circuit due to CMOS technology.

### Features

- LCD drive output pins : 240 pins
- LCD drive voltage : Max VEE + 42 V
- Data transfer method : Bidirectional shift register
- Operating temperature : -20 to 75°C
- Package : Tape carrier package (TCP)

Unit : mm

T6L08	USER AREA PITCH	
	IN	OUT

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

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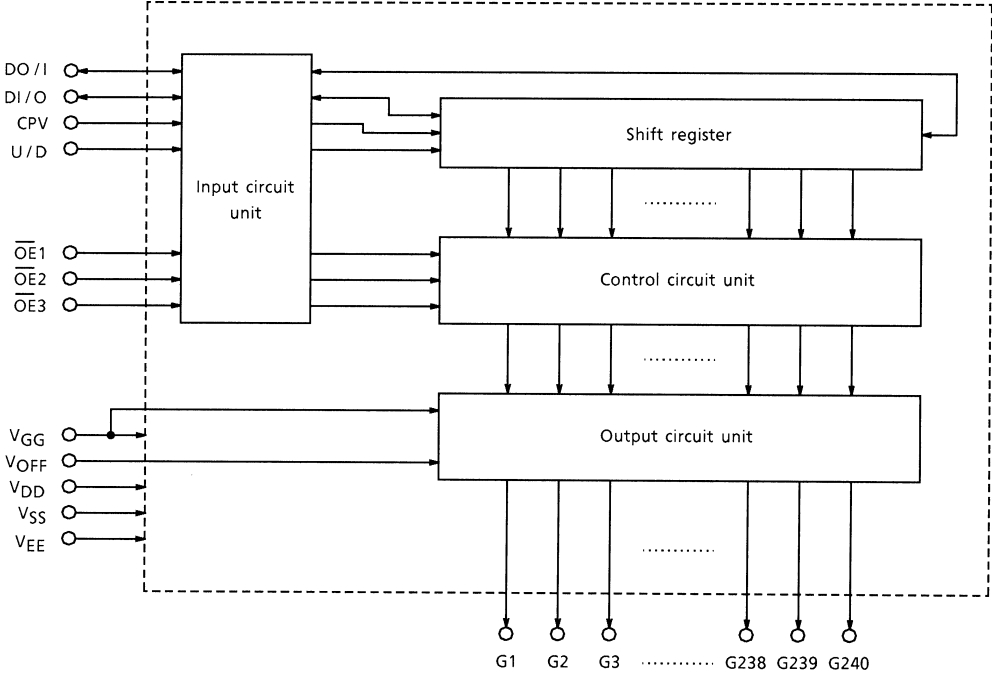
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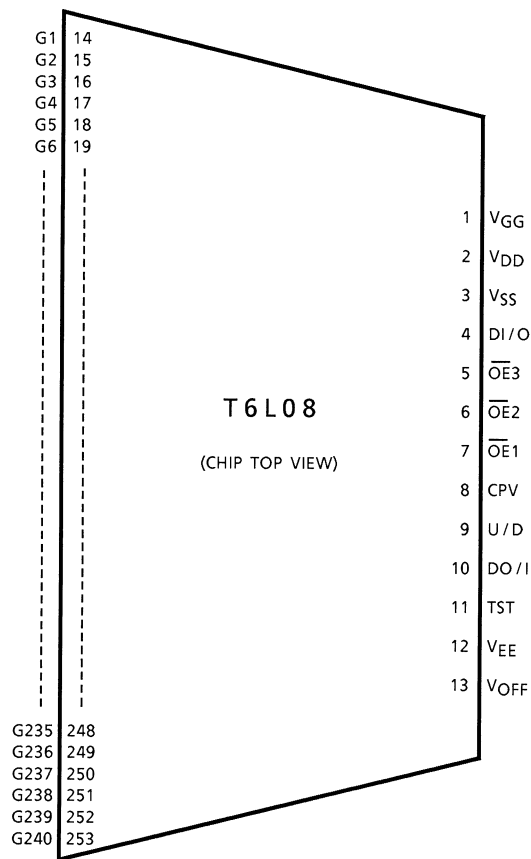
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Block Diagram



**Pin Assignment**



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

## Pin Function

Pin Name	I / O	Function									
DI / O DO / I	I / O	<p>Vertical shift data I / O pins. These pins are used to input and output shift data. These pins are switched between input and output by setting the U / D pin as shown below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>U / D</th> <th>DI / O</th> <th>DO / I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>When set for input This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.</p> <p>When set for output When two or more T6L08s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</p>	U / D	DI / O	DO / I	H	Input	Output	L	Output	Input
U / D	DI / O	DO / I									
H	Input	Output									
L	Output	Input									
U / D	Input	<p>Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. When U / D is high, data is shifted in the direction G1 → G2 → G3 → G4 → G5 → ... → G240 When U / D is low, the direction is reversed to give G240 → G239 → G238 → G237 → ... → G1 The voltage applied to this pin must be a DC-level voltage that is either high (<math>V_{DD}</math>) or low (<math>V_{SS}</math>).</p>									
CPV	Input	<p>Vertical shift clock This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</p>									
$\overline{OE}$ 1 to 3	Input	<p>Output enable input These signals control the data appearing at the LCD panel drive pins (G1 to G240). The <math>V_{OFF}</math> voltage is output when <math>\overline{OE}</math> 1 to 3 are high; normal shift data is output when <math>\overline{OE}</math> 1 to 3 are low.</p>									
$V_{OFF}$	Input	<p>Analog input pin If the shift register data is low (= logic 0), the voltage on this pin is forwarded to the output pin corresponding to the shift register. If <math>\overline{OE}</math> 1 to 3 are high, the voltage on this pin is output irrespective of whether the shift register data is high or low.</p>									
TST	Input	<p>Test pin Leave this pin open.</p>									
G1 to 240	Output	<p>LCD panel drive pins These pins output the shift register data, or the voltage applied to <math>V_{GG}</math> or <math>V_{OFF}</math>, depending on the control signals <math>\overline{OE}</math> 1 to 3.</p>									
$V_{GG}$	—	Power supply for LCD drive									
$V_{DD}$	—	Power supply for the internal logic									
$V_{SS}$	—	Power supply for the internal logic									
$V_{EE}$	—	Power supply for LCD drive and the internal logic									

## Device Operation (See Timing Diagram)

### (1) Shift data transfer method

The input shift data is latched into the internal register synchronously with the rising edge of the shift clock CPV. When the data is shifted to the next register at the next rising edge of CPV, new input shift data is simultaneously latched into.

In the case of shift data output, the data in the last shift register is output synchronously with the falling edge of CPV (the output high voltage level is VDD; the output low voltage level is VSS).

U / D	DI / O	DO / I	Data Transfer Method
H	Input	Output	DI / O → G1 → G2 → G3 → ..... → G240 → DO / I
L	Output	Input	DO / I → G240 → G239 → G238 → ..... → G1 → DI / O

### (2) LCD panel drive outputs

If the shift register data corresponding to an output pin is high (= logic 1), the pin outputs VGG; if the shift register data is low (= logic 0), the pin outputs VOFF.

However, if  $\overline{OE}$  1 to 3 corresponding to the output pins are high, the pins output VOFF irrespective of whether the shift register data is high or low. The LCD panel drive outputs are controlled by  $\overline{OE}$  as shown below.

Output Enable Pin		Lcd Panel Drive Outputs	
H / L	$\overline{OE}$ 1 to 3	LCD Panel Drive Pins Controlled By $\overline{OE}$	Output
L	$\overline{OE}$ 1	G1, G4, G7, G10 ..... G235, G238	Normal data output
	$\overline{OE}$ 2	G2, G5, G8, G11 ..... G236, G239	
	$\overline{OE}$ 3	G3, G6, G9, G12 ..... G237, G240	
H	$\overline{OE}$ 1	G1, G4, G7, G10 ..... G235, G238	VOFF
	$\overline{OE}$ 2	G2, G5, G8, G11 ..... G236, G239	
	$\overline{OE}$ 3	G3, G6, G9, G12 ..... G237, G240	

### (3) Voltage setting

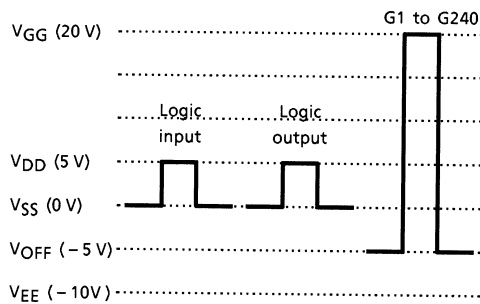
(Example 1) Negative voltage output

Logic input : High = 5 V or low = 0 V amplitude  
 Supply voltage :  $V_{GG} = 20\text{ V}$   
 $V_{DD} = 5\text{ V}$   
 $V_{OFF} = -5\text{ V}$   
 $V_{EE} = -10\text{ V}$   
 LCD panel drive output : High level =  $V_{GG}$  (20 V)  
 Low level =  $V_{GG}$  (-5 V)

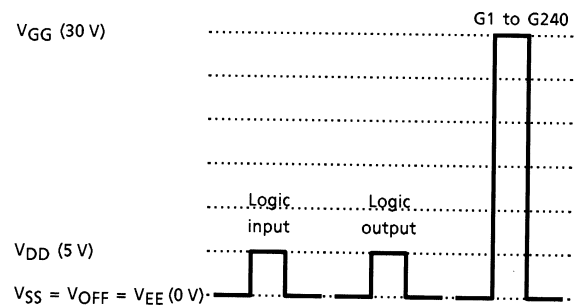
(Example 2) Positive voltage output

Logic input : High = 5 V or low = 0 V amplitude  
 Supply voltage :  $V_{GG} = 30\text{ V}$   
 $V_{DD} = 5\text{ V}$   
 $V_{OFF} = V_{SS} = V_{EE} = 0\text{ V}$   
 LCD panel drive output : High level =  $V_{GG}$  (30 V)  
 Low level =  $V_{OFF}$  (0 V)

(\*) Logic input pins : DI / O or DO / I, CPV,  $\overline{OE}$  1 to 3, U / D



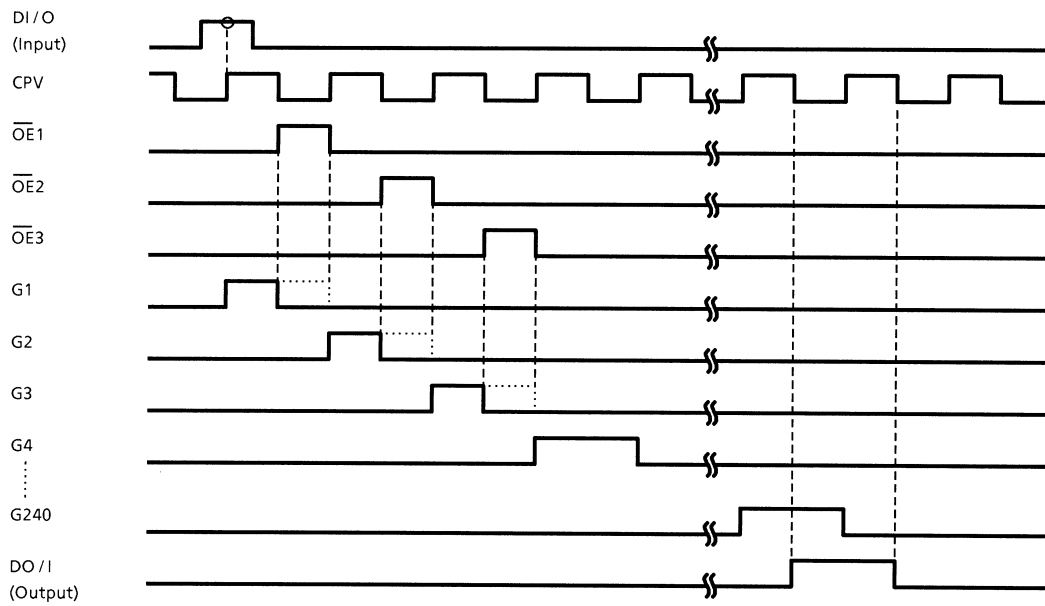
(Example 1)



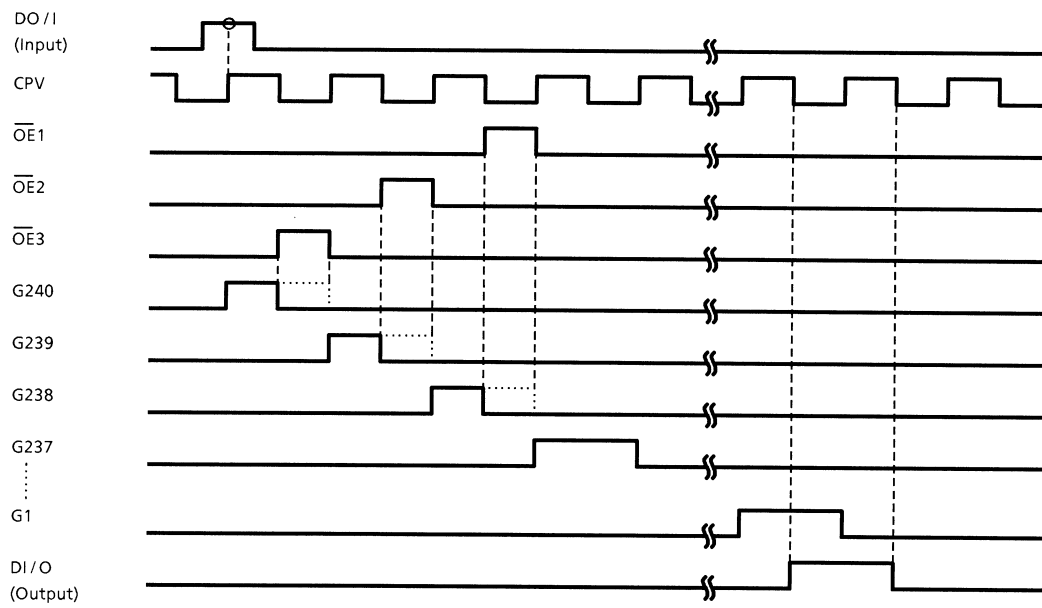
(Example 2)

## Timing Diagrams

- UP mode (U / D = high)



- DOWN mode (U / D = low)



**Absolute Maximum Ratings ( $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Rating	Unit
Supply Voltage (1)	$V_{GG} - V_{EE}$	15.0 to 45.0	V
Supply Voltage (2)	$V_{DD}$	-0.3 to 7.0	V
Supply Voltage (3)	$V_{EE}$	-16.0 to 0.3	V
Input Voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Analog Input Voltage	$V_{OFF}$	$V_{EE} - 0.3$ to $V_{GG} + 0.3$	V
Storage Temperature	$T_{STG}$	-55 to 125	°C

**Recommended Operating Conditions ( $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Rating	Unit
Supply Voltage (1)	$V_{GG} - V_{EE}$	15.0 to 42.0	V
Supply Voltage (2)	$V_{DD}$	4.5 to 5.5	V
Supply Voltage (3)	$V_{EE}$	-15.0 to 0	V
Operating Temperature	$T_{op}$	-20 to 75	°C
Operating Frequency	$F_{CPV}$	DC to 100	kHz
Output Load Capacitance	$C_L$	300 (max)	pF / pin
Analog Input Voltage	$V_{OFF}$ (Note 1)	-15.0 to 0	V

Note 1:  $V_{EE} \leq V_{OFF}$

## Electrical Characteristics

### DC Characteristics

(Referenced to  $V_{GG} - V_{EE} = 42\text{ V}$  at  $T_a = -20$  to  $75^\circ\text{C}$  unless otherwise noted)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input Voltage	Low Level	$V_{IL}$	—		$V_{SS}$	—	$0.2 \times (V_{DD} - V_{SS}) + V_{SS}$	V	(Note 2)
	High Level	$V_{IH}$			$0.8 \times (V_{DD} - V_{SS}) + V_{SS}$	—	$V_{DD}$		
Output Voltage	Low Level	$V_{OL}$	—	$I_{OL} = 40\ \mu\text{A}$	$V_{SS}$	—	$V_{SS} + 0.3\text{ V}$	V	DI / O, DO / I
	High Level	$V_{OH}$		$I_{OH} = -40\ \mu\text{A}$	$V_{DD} - 0.3\text{ V}$	—	$V_{DD}$		
Output Resistance	Low Level	$R_{OL}$	—	$V_{OUT} = V_{OFF} + 0.5\text{ V}$	—	—	1500	$\Omega$	G1 to G240
	High Level	$R_{OH}$		$V_{OUT} = V_{GG} - 0.5\text{ V}$	—	—	1500		
Input Leakage Current		$I_{IN}$	—		-1.0	—	1.0	$\mu\text{A}$	(Note 2)
Current Consumption (1)		$I_{GG}$	—	$f_{CPV} = 100\text{ kHz}$	—	—	200	$\mu\text{A}$	$V_{GG}$
Current Consumption (2)		$I_{DD}$	—		—	—	900	$\mu\text{A}$	$V_{DD}$
Current Consumption (3)		$I_{SS}$	—		-200	—	200	$\mu\text{A}$	$V_{SS}$

Note 2: Input pins include ... DI / O, DO / I, U / D, CPV,  $\overline{OE}$  1 to 3

## AC Characteristics

(Referenced to  $V_{GG} - V_{EE} = 42\text{ V}$  at  $T_a = -20$  to  $75^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock Period	$t_{CPV}$	—	—	10	—	—	$\mu\text{s}$
CPV Pulse Width (H)	$t_{CPVH}$	—	—	4	—	—	$\mu\text{s}$
CPV Pulse Width (L)	$t_{CPVL}$	—	—	4	—	—	$\mu\text{s}$
OE Enable Time	$t_{wOE}$	—	—	1	—	—	$\mu\text{s}$
Data Set-up Time	$t_{sDI}$	—	—	1	—	—	$\mu\text{s}$
Data Hold Time	$t_{hDI}$	—	—	1	—	—	$\mu\text{s}$
Output Delay Time (1)	$t_{pdDO}$	—	$C_L = 50\text{ pF}$	—	—	1	$\mu\text{s}$
Output Delay Time (2)	$t_{pdG}$	—	$C_L = 300\text{ pF}$	—	—	1	$\mu\text{s}$
Output Delay Time (3)	$t_{pdOE}$	—	$C_L = 300\text{ pF}$	—	—	1	$\mu\text{s}$

