

# Surface Mount Quartz Crystal Oscillator PG and LG series



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## Description:

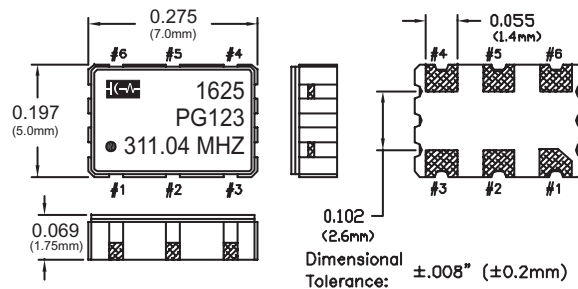
Connor-Winfield's PGxxx and LGxxx series are 5x7mm surface mount, fixed frequency crystal controlled oscillators (XO) designed for applications requiring tight frequency stability, wide temperature range, and low jitter. Operating at 2.5 or 3.3Vdc supply voltage, the PGxxx series provides LVPECL differential outputs, while the LGxxx provides LVDS differential outputs. Enable/Disable function is available on Pad 1 or 2.



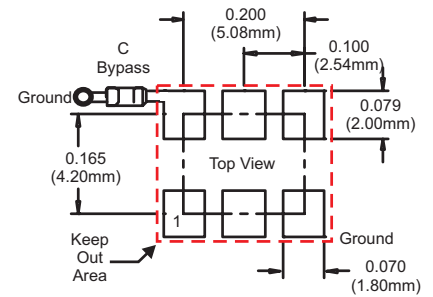
## Features:

- Frequency Range 10 MHz to 1.5 GHz
- 3.3 or 2.5 Vdc Operation
- 5x7 mm SMT Package
- Frequency Stabilities Available:
  - $\pm 20$  ppm,  $\pm 25$  ppm,  $\pm 50$  ppm
  - or  $\pm 100$  ppm
- Temperature Ranges Available:
  - 0 to 70°C, -40 to 85°C, 0 to 85°C
  - or -20 to 70°C
- Low Jitter: 0.6ps RMS Typical
- Differential LVPECL or LVDS outputs
- Tri-State Enable/Disable on Pad 1 or 2
- Tape and Reel Packaging
- RoHS Compliant / Lead Free

## Package Outline



## Suggested Pad Layout



Keep Out Area: Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

## Pad Connections

Models: PGxx2, PGxx3, LGxx2, LGxx3

- 1: Enable / Disable (OE)
- 2: N/C
- 3: Ground:
- 4: Output Q
- 5: Complementary Output  $\bar{Q}$
- 6: Supply Voltage (Vcc)

## Pad Connections

Models PGxx4, PGxx5, LGxx4, LGxx5

- 1: N/C
- 2: Enable / Disable (OE)
- 3: Ground:
- 4: Output Q
- 5: Complementary Output  $\bar{Q}$
- 6: Supply Voltage (Vcc)

## Ordering Information

PG	1	2	3	-311.04M
Oscillator Type	Temperature Range	Frequency Tolerance	Supply Voltage E/D Function	Output Frequency
LVPECL Clock Series 5x7 mm PG=LVPECL LG=LVDS	1 = 0 to 70°C 2 = -40 to 85°C 3 = 0 to 85°C 4 = -20 to 70°C	4 = $\pm 20$ ppm 1 = $\pm 25$ ppm 2 = $\pm 50$ ppm 3 = $\pm 100$ ppm	2 = 2.5 Vdc, E/D Pad 1 3 = 3.3 Vdc, E/D Pad 1 4 = 2.5 Vdc, E/D Pad 2 5 = 3.3 Vdc, E/D Pad 2	Frequency Format -xxx.xM Min.* -xxx.xxxxxxM Max*

\*Amount of numbers after the decimal point.  
M = MHz

Example Part Numbers:

PG123-311.04M = 5x7 mm package,  $\pm 50$  ppm, 0 to 70°C, 3.3 Vdc, LVPECL Output, E/D Pad 1, Output Frequency 311.04 MHz

LG224-622.08M = 5x7 mm package, +/-50ppm, -40 to 85°C, 2.5 Vdc, LVDS Output, E/D Pad 2, Output Frequency 622.08 MHz



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Date **21 June 2016**



## Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.2	Vdc	
Input Voltage	-0.5	-	Vcc+0.5	Vdc	

## Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Center Frequency: (Fo)	10	-	1500	MHz	
Operating Temperature Range: (See Ordering Information)					
Temperature Code 1	0	-	70	°C	
Temperature Code 2	-40	-	85	°C	
Temperature Code 3	0	-	85	°C	
Temperature Code 4	-20	-	70	°C	
Total Frequency Tolerance: (See Ordering Information)					
Tolerance Code 4	-20.0	-	20.0	ppm	1
Tolerance Code 1	-25.0	-	25.0	ppm	1
Tolerance Code 2	-50.0	-	50.0	ppm	1
Tolerance Code 3	-100.0	-	100.0	ppm	1
Supply Voltage: (Vcc)					
Supply Voltage Code 2 or 4	2.375	2.5	2.625	Vdc	±5%
Supply Voltage Code 3 or 5	3.135	3.3	3.465	Vdc	±5%
Supply Current	-	30	60	mA	
Start-Up Time:	-	-	10	ms	

## Jitter / Phase Noise Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Jitter					
Period Jitter	-	6	8	ps RMS	
Integrated Phase Jitter	-	0.6	1	ps RMS	
SSB Phase Noise for Fo = 312.5 MHz					
@ 100 Hz offset	-	-75	-	dBC/Hz	
@ 1 KHz offset	-	-105	-	dBC/Hz	
@ 10 KHz offset	-	-115	-	dBC/Hz	
@ 100 KHz offset	-	-120	-	dBC/Hz	
@ 1 MHz offset	-	-130	-	dBC/Hz	
@ 10 MHz offset	-	-150	-	dBC/Hz	

## Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable / Disable Function Option:					
Models xGxx2, xGxx3 E/D Pad 1, N/C Pad 2					
Models xGxx4, xGxx5 E/D Pad 2, N/C Pad 1					
Enable Voltage (V <sub>IH</sub> )	70% Vcc	-	-	Vdc	
Disable Voltage (V <sub>IL</sub> )	-	-	30% Vcc	Vdc	2
Enable Time	-	-	200	ns	
Disable Time	-	-	50	ns	

## Enable / Disable Function

Function: (Pad 1 or 2)	Output
Low	Disabled (High Impedance)
High or Open	Enabled



## LVPECL Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	50	-	Ohms	3
Output Voltage: Vcc = 2.5 Vdc					
High (VOH)	1.475	-	-	V	
Low (VOL)	-	-	0.880	V	
Output Voltage: Vcc = 3.3 Vdc					
High (VOH)	2.275	-	-	V	
Low (VOL)	-	-	1.680	V	
Duty Cycle at 50% of output voltage swing	45	50	55	%	
Rise / Fall Time: 20% to 80%	-	350	500	ps	

## LVDS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	100	-	Ohms	
Output Differential Voltage (Vod)	250	-	450	mV	4
Output Swing (Differential Output Pk to Pk)	500	700	900	mV	
Duty Cycle at 50% of output voltage swing	45	50	55	%	
Differential Rise / Fall Time: 20% to 80%	-	150	350	ps	

## Package Characteristics

Package	Hermetically sealed ceramic package and metal cover
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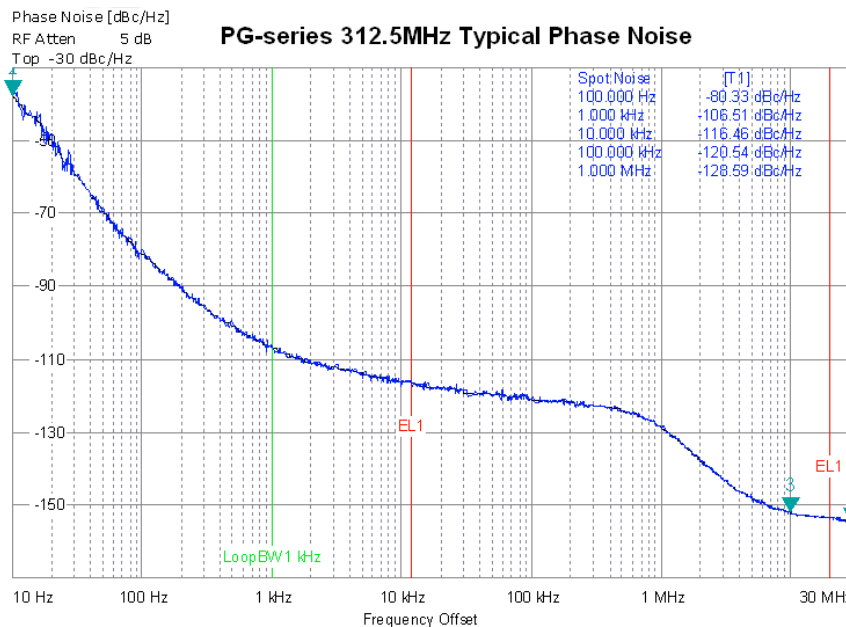
## Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process;	RoHS compliant lead free. See soldering profile on page 4.

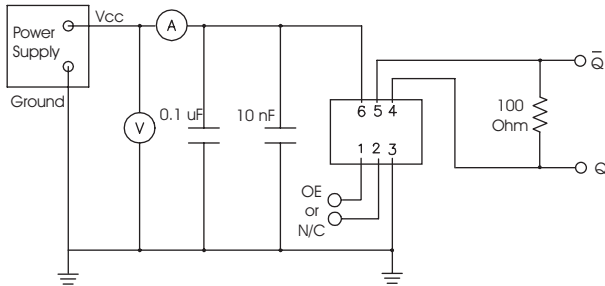
### Notes:

1. Includes calibration @ 25°C, frequency stability vs. change in temperature, supply voltage and load variations, shock and vibration and 20 years aging.
2. When the oscillator is disabled the outputs go to tri-state level (high impedance) which floats to VOL. Outputs are enabled with no connection on E/D pad.
3. LVPECL outputs must be terminated into 50 ohms to Vcc - 2V or Thevenin equivalent.
4. Vod is measured with a 100 ohm resistor between the true and the complementary outputs.

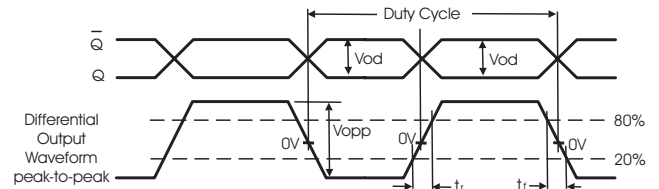
## Phase Noise Plot



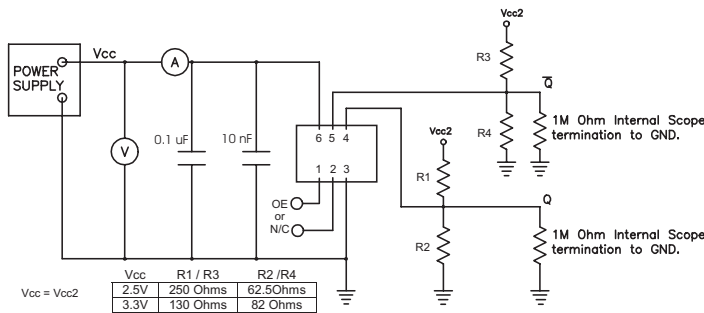
## LVDS Test Circuit



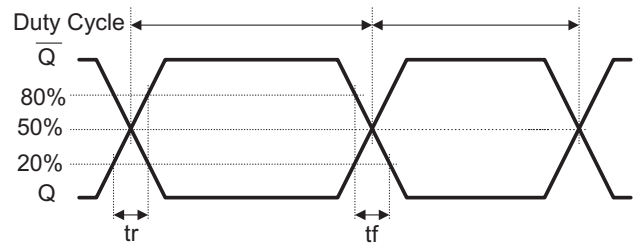
## LVDS Output Waveform



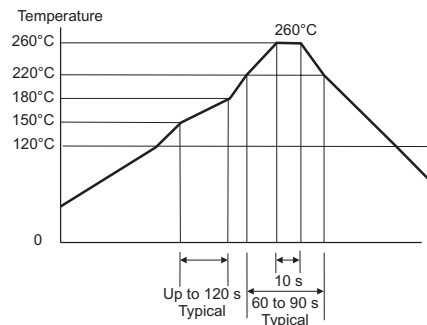
## LVPECL Test Circuit



## LVPECL Output Waveform

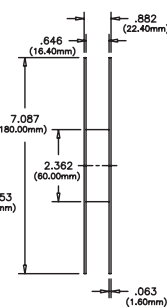
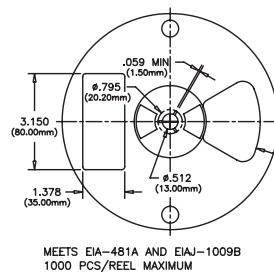
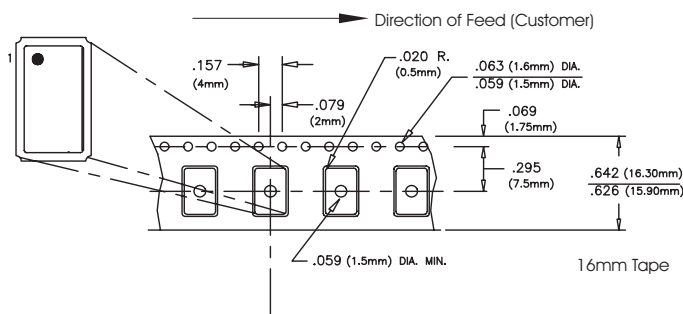


## RoHS Solder Profile



Meets IPC/JEDEC J-STD-020C

## Tape and Reel Dimensions



Revision	Revision Date	Note
00	08/28/12	Data Sheet Release
01	01/14/15	Added LDVS Information
02	06/07/16	Updated period jitter and rise/fall time.

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