HD64646

LCD Timing Controller (LCTC)

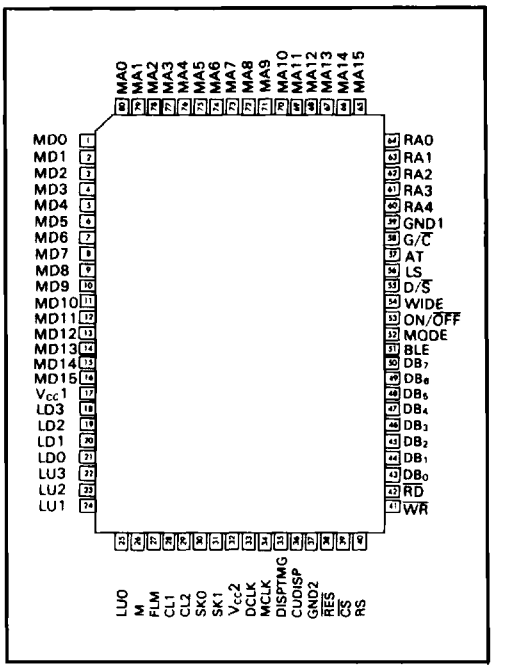
Description

The HD64646 LCTC is a modified version of the HD64645 LCTC with differente LCD interface timing.
The HD64646 is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106 (column/common)
- CPU interface:
  80 family
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80A)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	FP-80
HD64645	4 MHz	80 System	FP-80
HD64646	4 MHz	80 System	FP-80B

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Differences Between HD64645 and HD64646

Fig.1 and Fig.2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Fig.1 shows the case without skew function and fig.2 shows the case with skew function.
In Fig.1 "High" period between CL2 and CL1 of HD64645 overlap.
HD64646 has no overlap like HD64645, and except for overlap parts HD64646 is the same as HD64645 functionally.
Besides, in case of skew function, phase relation between CL1 and CL2 changes. As Fig.2 shows, data transfer period and CL1 "High" period of HD64646 never overlap in case of skew function.

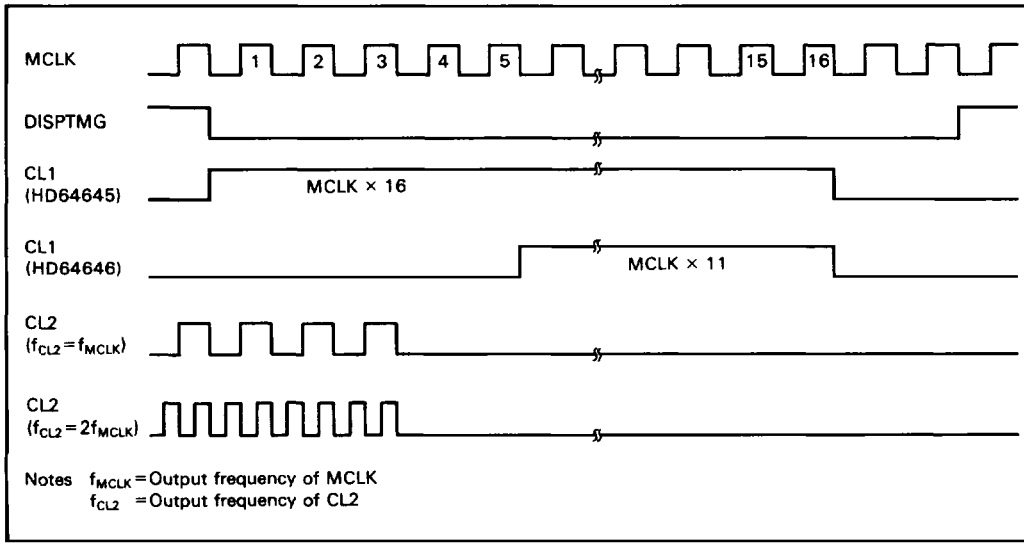

Figure 1. Differences between HD64645 and HD64646 (no skew)

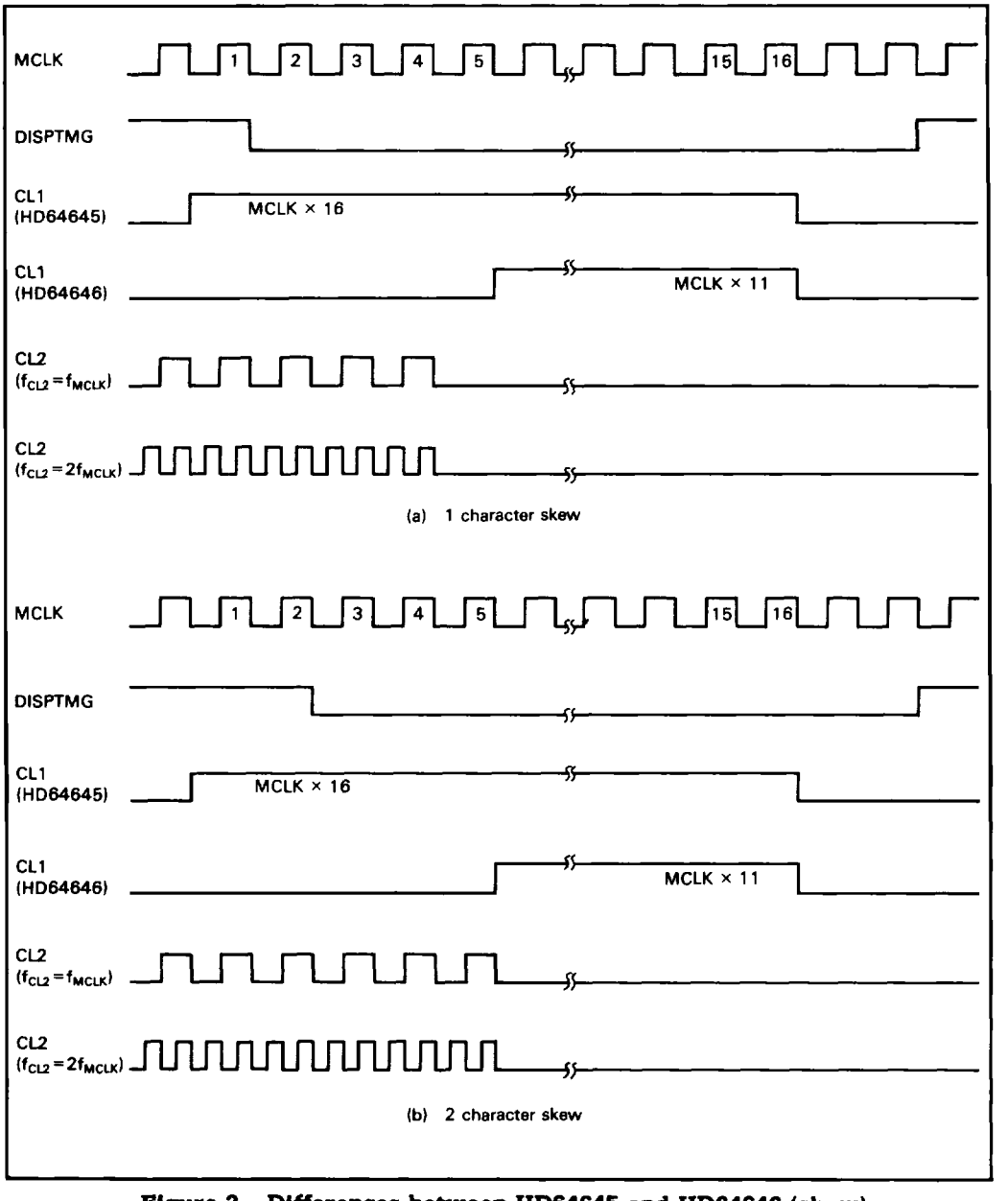

Figure 2. Differences between HD64645 and HD64646 (skew)

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Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.
2. With respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{RES}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{OFF}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400μA
Input leakage current	All inputs except DB_0−DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0−DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes : 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM
2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.
3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	3
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

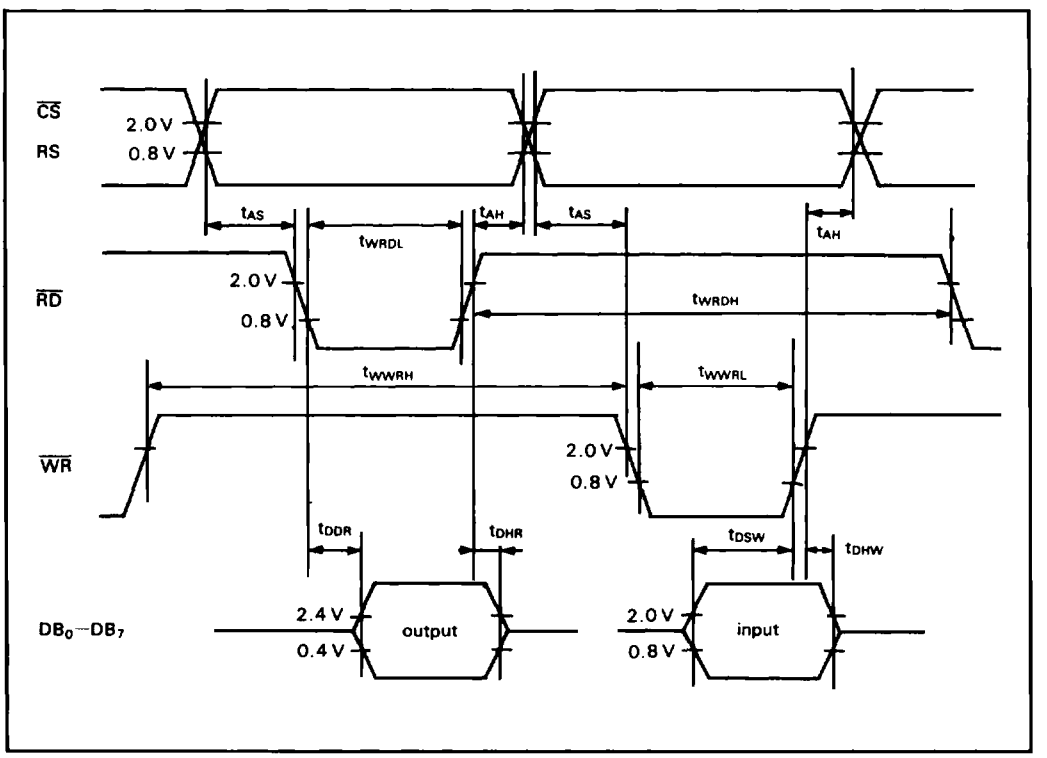

Figure 3. CPU Interface

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AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	4
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			60	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

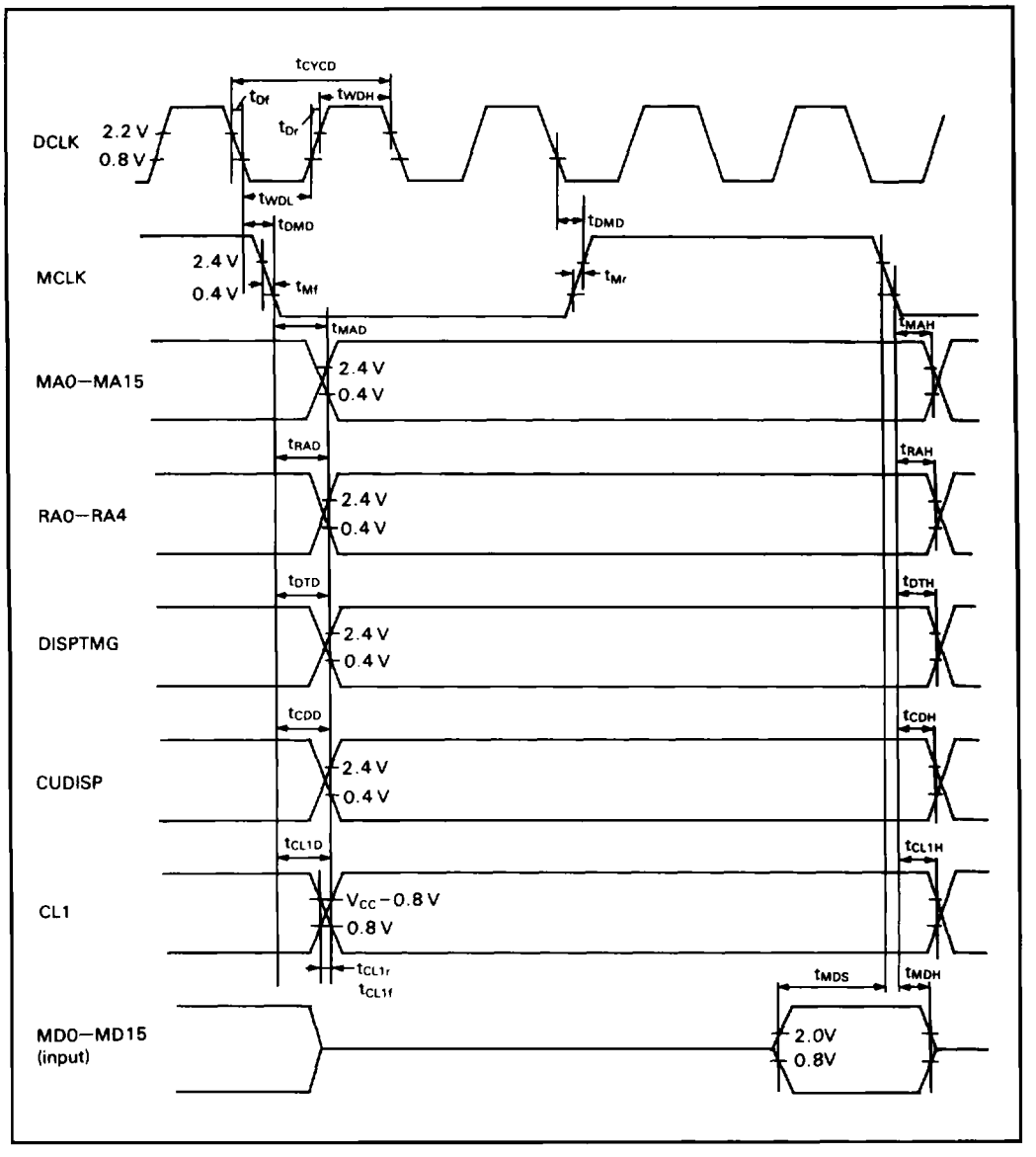

Figure 4. Memory Interface

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AC Characteristics (Cont)

LCD Interface 1 (at f_{CL2}=3MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 2 (at f_{CL2}=5MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{Fs}	500	–	–	ns	5
FLM hold time	t_{FH}	200	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

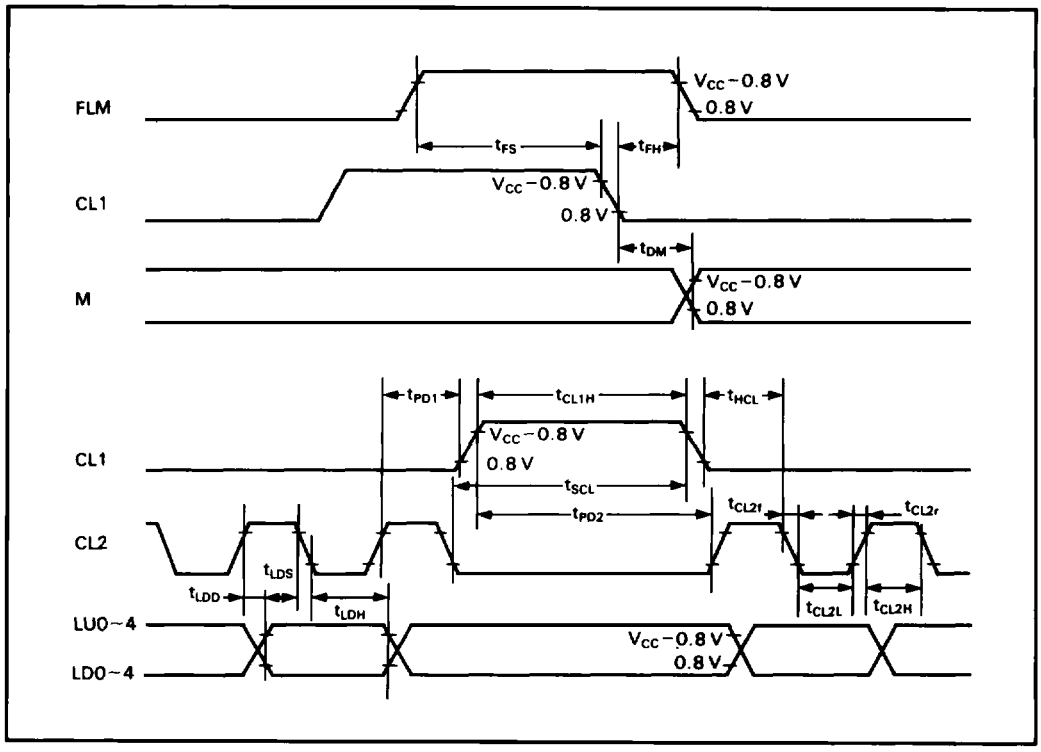

Figure 5. LCD Interface

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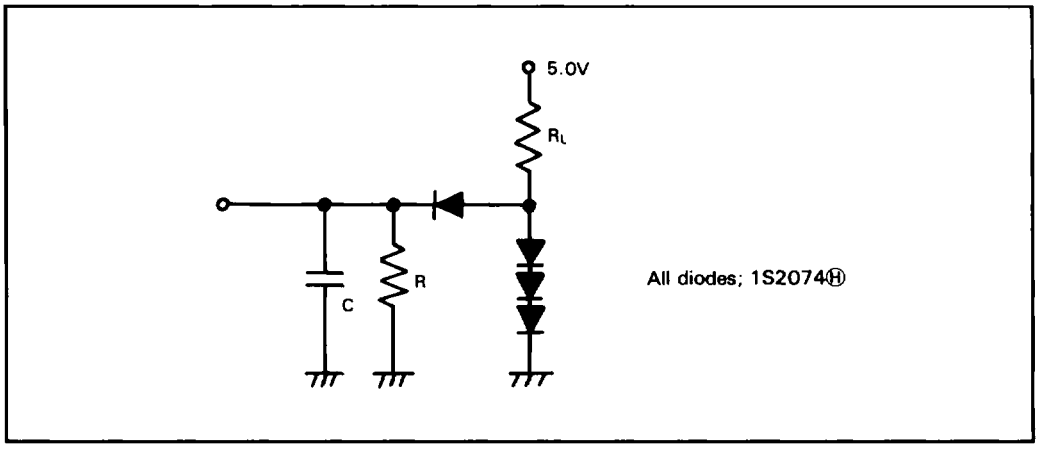
AC Characteristics

TTL Load

Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF