FEATURES

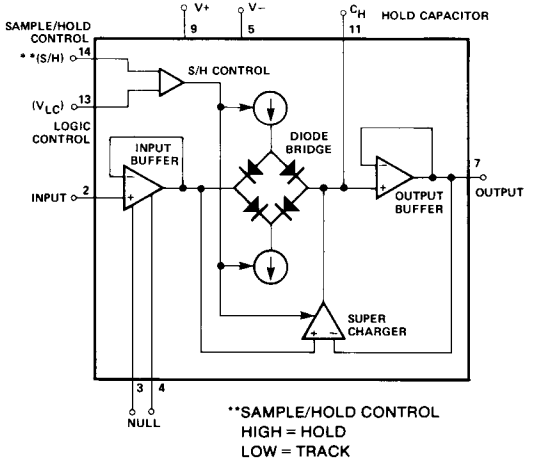
- **Meets System Performance Requirements in Multi-Channel CODECs**
- **Trimmed for Minimum Zero-Scale Error 0.6mV**
- **Low Droop Rate Over Temperature 1600μV/ms**
- **Low Aperture Time 50ns**
- **Fast Acquisition Time 10V Step to 0.1% 3.5μs**
- **High Slew Rate 10V/μs**
- **High Sample-Current to Hold-Current Ratio .. 1.7×10^8**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible***
- **Low Power Dissipation**
- **Low Cost**
- **Feedthrough Attenuation Ratio 96dB**

ORDERING INFORMATION†

V_{ZS} (mV)	HERMETIC 14-PIN DIP	OPERATING TEMPERATURE RANGE
1.6	SMP-81EY	IND
3.5	SMP-81FY	IND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The SMP-81 precision sample-and-hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM encoders. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

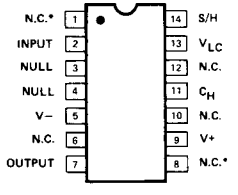
HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and low droop rate of the SMP-81 are achieved by PMI's ion implant super beta process. The high input impedance permits high source impedance applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include high accuracy, 0.6mV of combined offset voltage and step transfer error, and very low feedthrough. A diode bridge switch design allows minimum charge transfer step. On-chip zener-zap trimming eliminates nulling for most applications.

FAST ACQUISITION

A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

*Pins 1 and 8 are not internally connected. In unity gain applications, the SMP-81 can replace HA-2425, SHM-IC-1 and AD-583 directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ minus V–) 36V
Derate Above 100°C ..... 10mW/°C
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Control Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Hold Capacitor Short-Circuit Duration ..... 60 sec
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at $V_S \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-25°C \leq T_A \leq +85°C$, unless otherwise noted.

			SMP-81E			SMP-81F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ (500µsec after Hold Command)	—	0.6	1.6	—	0.9	3.5	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	105	225	—	120	450	nA
Leakage (Droop) Current	I_{DR}		—	0.5	10	—	0.5	20	nA
Droop Rate	dVC_H/dt		—	1600	2000	—	2000	4000	µV/ms
Input Resistance	R_{IN}	(See Note)	0.6	2.0	—	0.3	1.4	—	GΩ
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99960	0.99980	—	0.99955	0.99978	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	µs
Aperture Time	t_{ap}		—	50	—	—	50	—	nsec
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	—	10	—	—	10	—	V/µs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3$ volts	30	50	—	20	50	—	mA
Feedthrough Attenuation Ratio	F_A	Input $-20V_{p-p}$ 1kHz, $R_L = 5K\Omega$ (See Note)	86	96	—	80	90	—	dB
Full Power Bandwidth	F_P	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	±10	±11.5	—	±10	±11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	90	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	mW
Logic Control Input Current	I_{LC}		-6	-3	—	-9	-3	—	µA
Logic Input Current	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	—	-15	-45	—	-15	-45	µA
		Hold Mode $V_{S/H} = 5.0V$	—	0.6	—	—	0.6	—	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	V
Hold Mode Settling Time	t_{HM}	5V step to within 1mV of final value	—	1.5	—	—	1.5	—	µs

NOTE: Guaranteed by design.

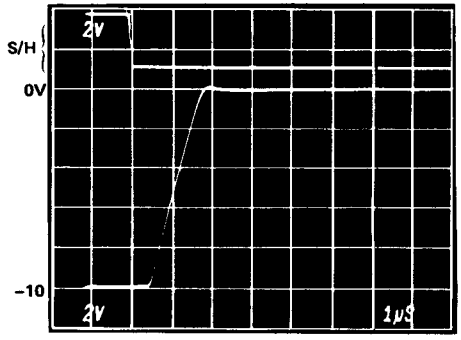
DICE

For applicable DICE information, see SMP-11 Data Sheet.

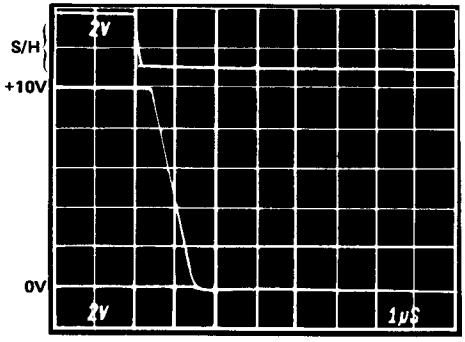
TYPICAL PERFORMANCE CHARACTERISTICS

SMP-81 ACQUISITION TIMES

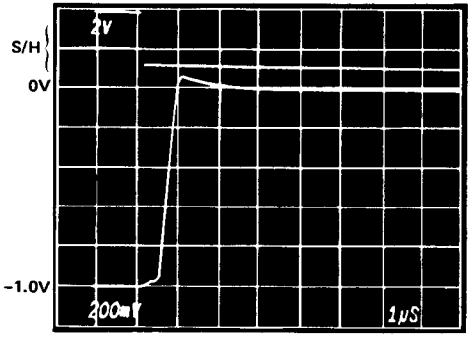
ACQUISITION TIME
– 10V TO 0V



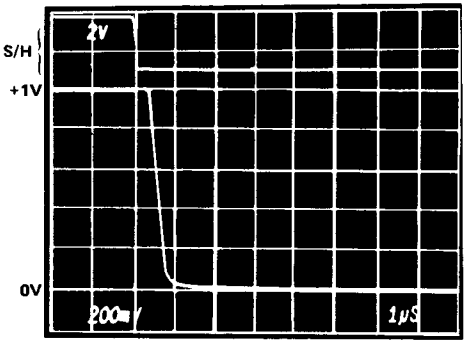
ACQUISITION TIME
+ 10V TO 0V



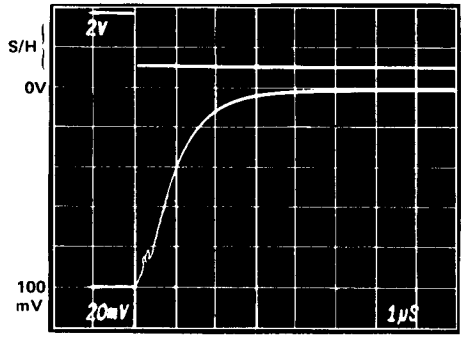
ACQUISITION TIME
– 1.0V TO 0V



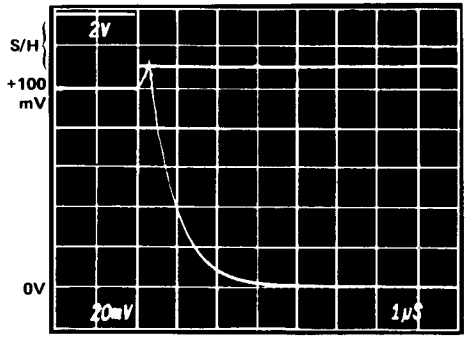
ACQUISITION TIME
+ 1.0V TO 0V

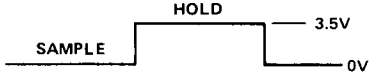


ACQUISITION TIME
– 100mV TO 0V



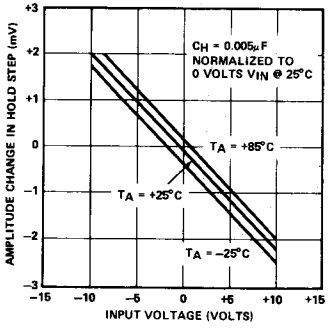
ACQUISITION TIME
+ 100mV TO 0V



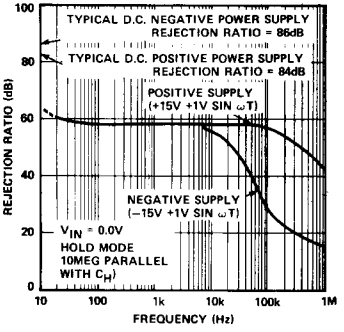


TYPICAL PERFORMANCE CHARACTERISTICS

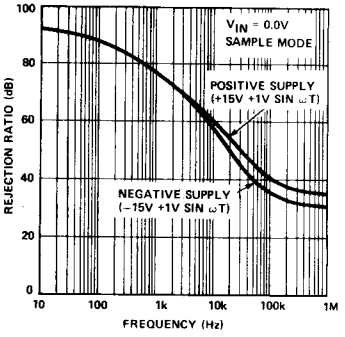
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



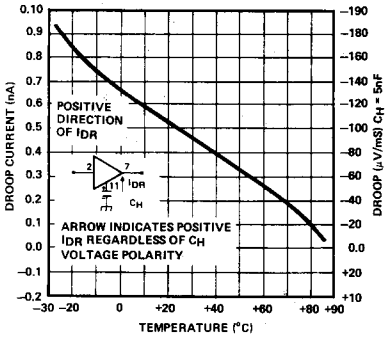
HOLD-MODE POWER SUPPLY REJECTION



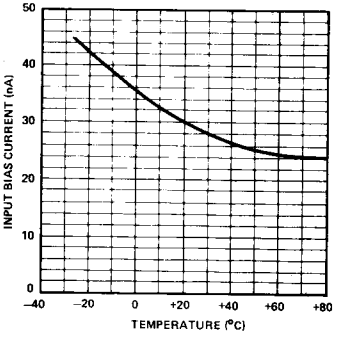
SAMPLE-MODE POWER SUPPLY REJECTION



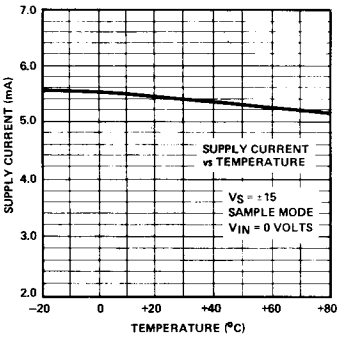
LEAKAGE (DROOP) CURRENT vs TEMPERATURE



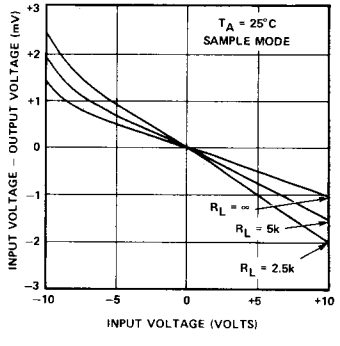
INPUT BIAS CURRENT vs TEMPERATURE



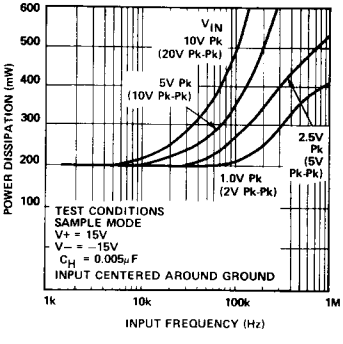
SAMPLE-MODE SUPPLY CURRENT vs TEMPERATURE



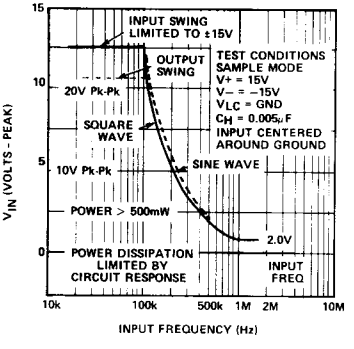
GAIN ERROR



POWER DISSIPATION vs FREQUENCY INPUT = V_P sin ωt

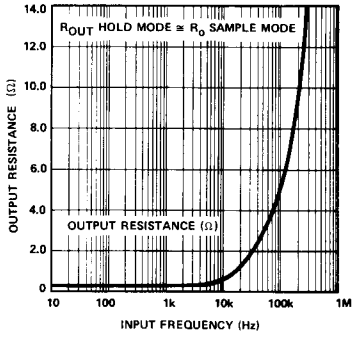


MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY

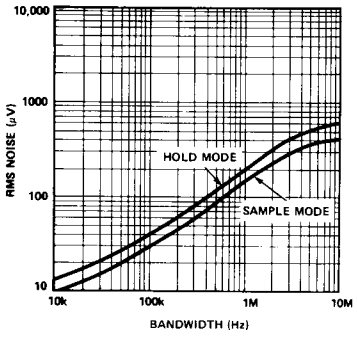


TYPICAL PERFORMANCE CHARACTERISTICS

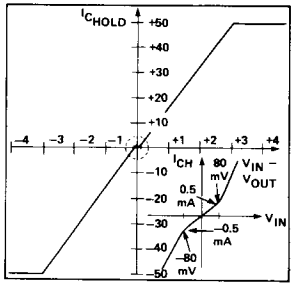
OUTPUT RESISTANCE vs FREQUENCY



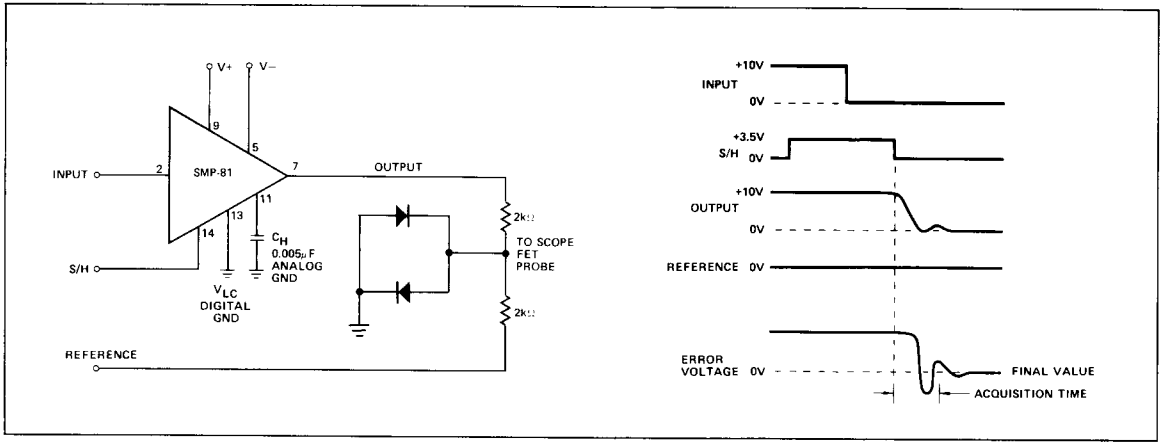
OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE



ACQUISITION TIME TEST CIRCUIT



APPLICATIONS INFORMATION

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for $C_H = 5000pF$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}\,(mV) = \frac{5\,(pC) \times 10^3}{C_H\,(pF)} - 1$$

A C_H of 5000pF has been empirically determined to be an optimum value for 8-channel shared CODEC operation.

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in Figure 1, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HNIL interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC}.

SAMPLE/HOLD MODE INTERFACE CIRCUITRY

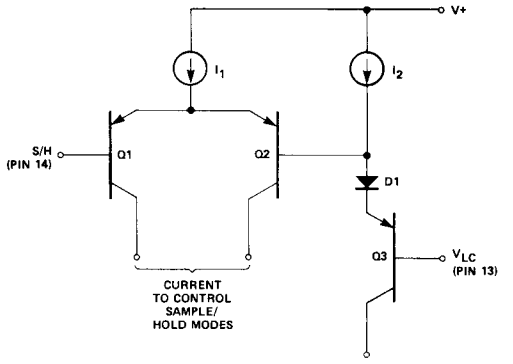


Figure 1

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.

ZERO-SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero. Figure 2 shows the recommended 10kΩ trim pot connected to V+ if user needs better V_{ZS} than 1.6mV.

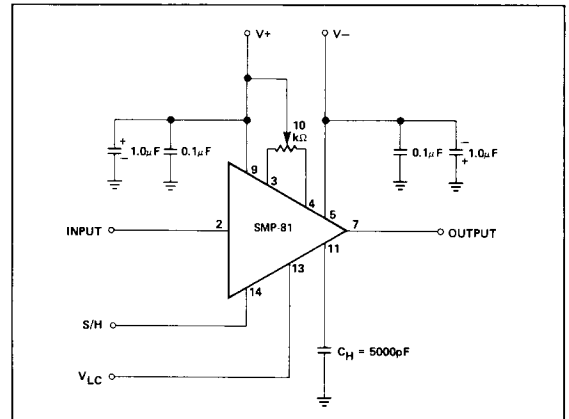


Figure 2

GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path. A guard trace surrounding the hold capacitor node pin 11, minimizes PC board leakage problems, see Figure 3.

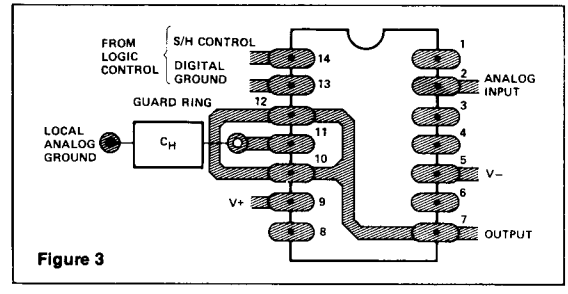


Figure 3

TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER