

TPIC2406 INTELLIGENT-POWER QUAD MOSFET LATCH

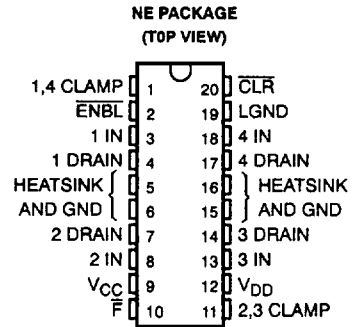
D3378, FEBRUARY 1990

- Output Voltage up to 60 V
- 4 Output Channels of 700-mA Nominal Current Per Channel
- Pulsed Current 3 A Per Channel
- Low $r_{DS(on)}$. . . 0.5 Ω Typ
- Avalanche Energy . . . 50 mJ
- Thermal Shutdown Protection with Fault (Overtemperature) Output
- NE Package Designed for Heat Sinking
- Integral Output Clamp Diodes
- Input Transparent Latches for Data Storage
- Asynchronous Clear to Turn Off All Outputs
- Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current

description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

Each device features four inverting open-drain outputs each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The \overline{CLR} function is asynchronous and turns all four outputs off regardless of data inputs. Taking \overline{ENBL} low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs will be held off while \overline{CLR} is low, but will return to the states on the data inputs when \overline{CLR} goes high. When \overline{ENBL} is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If the \overline{CLR} input is taken low, the data in the latches is cleared, turning all outputs off. If \overline{CLR} is taken high again, \overline{ENBL} must be cycled low to read new data into the latch.



**FUNCTION TABLE
(each channel)**

FUNCTION	INPUTS			OUTPUT	FAULT
	\overline{ENBL}	\overline{CLR}	IN	Y	F
NORMAL OPERATION	X	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q ₀	H
THERMAL SHUTDOWN	X	X	X	H	L

H = high-level, L = low-level, X = irrelevant

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

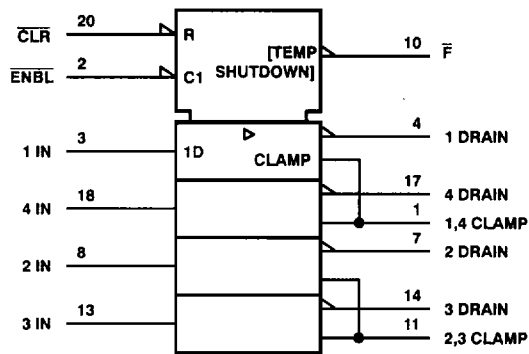
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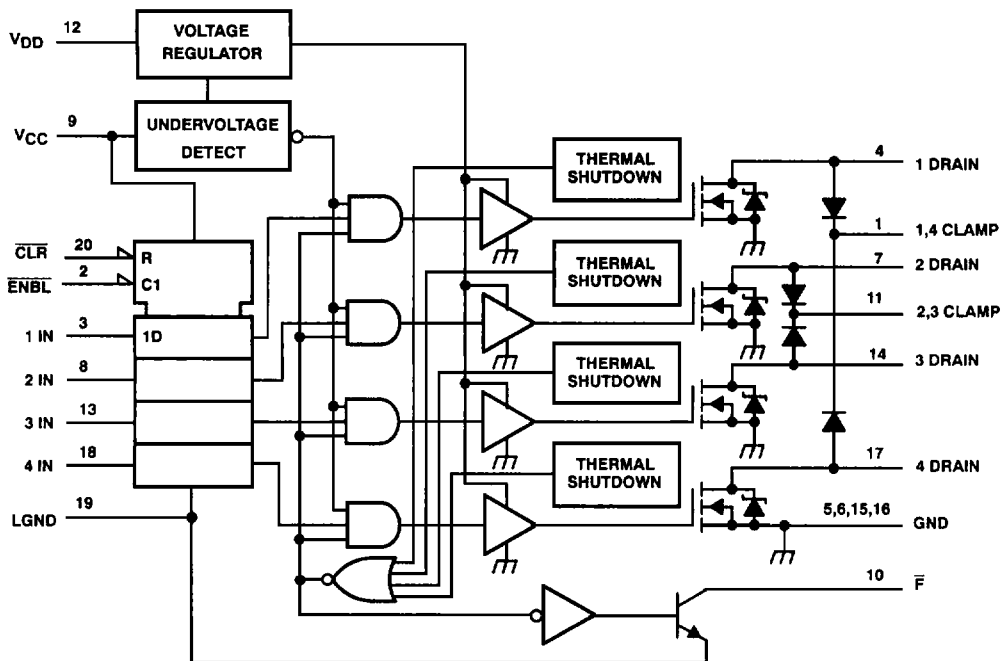
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logic symbol†

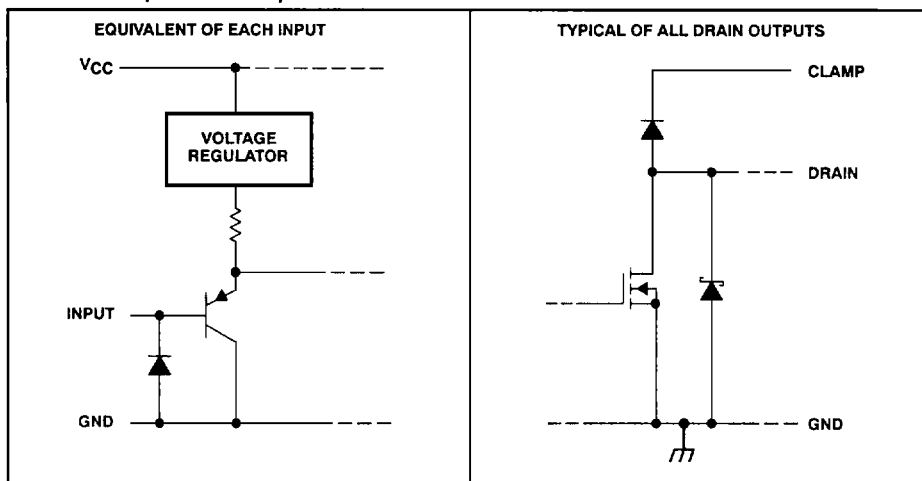


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over – 40°C to 125°C case temperature range (unless otherwise noted)

Logic supply voltage, V_{CC} (see Note 1)	7 V
Power MOSFET driver supply voltage, V_{DD}	60 V
Logic input voltage, V_I	7 V
Power MOSFET drain-source voltage, V_{DS}	60 V
\bar{F} output voltage	7 V
Clamp diode voltage	60 V
Continuous source-drain diode anode current	1.25 A
Pulsed source-drain diode anode current	6 A
Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25^\circ\text{C}$ (see Note 2 and Figures 5 through 8)	3 A
Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25^\circ\text{C}$	770 mA
Peak drain current, single output, I_{DM} , $T_A = 25^\circ\text{C}$ (see Note 3)	12.5 A
Single-pulse avalanche energy, E_{AS}	50 mJ
Continuous total dissipation at or below 25°C free-air temperature (see Note 4)	2.5 W
Continuous total dissipation at or below 100°C case temperature (see Note 4)	6 W
Operating junction temperature range, T_J	– 40°C to 150°C
Storage temperature range	– 40°C to 150°C
Lead temperature	260°C

- NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
 2. Pulse duration = 10 ms, duty cycle = 6%.
 3. Pulse duration $\leq 100 \mu\text{s}$, duty cycle $\leq 2\%$.
 4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}	4.5		5.5	V
Output supply voltage, V_{DD}	10		35	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.6	V
Setup time, t_{SU} , data before \overline{ENBL} ↑ (see Figure 1)	100			ns
Hold time, t_H , data after \overline{ENBL} ↑ (see Figure 1)	100			ns
Pulse duration, t_W (see Figure 1)	\overline{ENBL} low	300		ns
	CLR low			
Operating case temperature, T_C	-40		125	°C

electrical characteristics, $V_{CC} = 5\text{ V}$, $V_{DD} = 14\text{ V}$, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-source breakdown voltage	$I_D = 1\text{ mA}$	60			V
$V_{F(K)}$ Clamp diode forward voltage	$I_F = 1.25\text{ A}$, See Notes 5 and 6			1.6	V
V_{SD} Source-drain diode forward voltage	$I_S = 1.25\text{ A}$, See Notes 5 and 6			1.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = \sim 12\text{ mA}$			-1.5	V
V_{OL} \overline{F} low-level output voltage	$I_{OL} = 4\text{ mA}$		0.4		V
I_{IH} High-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			0.1	mA
I_{CC} Logic supply current	$I_O = 0$, All outputs off			10	mA
I_N Nominal current	$V_{DS(on)} = 0.5\text{ V}$, $T_C = 85^\circ\text{C}$, $I_N = I_D$, See Notes 5, 6, and 7		700		mA
I_{DD} Output supply current	$I_O = 0$, All outputs off			6	mA
$I_{R(K)}$ Clamp-diode reverse current	$V_{DS} = 55\text{ V}$, $V_O = 0$			1	μA
	$V_{DS} = 55\text{ V}$, $V_O = 0$, $T_C = 125^\circ\text{C}$			10	
I_{DSX} Off-state drain current	$V_R = 55\text{ V}$			1	μA
	$V_R = 55\text{ V}$, $T_C = 125^\circ\text{C}$			10	
$I_{O(\overline{F})}$ High-level fault leakage current	$V_{OH} = 5.5\text{ V}$			1	μA
$r_{DS(on)}$ Static drain-source on-state resistance	$I_D = 1.25\text{ A}$	See Notes 5 and 6	0.5	0.6	Ω
	$I_D = 1.25\text{ A}$, $T_C = 125^\circ\text{C}$		0.8	1	
	$I_D = 3\text{ A}$		0.55	0.65	

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C at case temperature.

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switching characteristics, $V_{CC} = 5\text{ V}$, $V_{DD} = 24\text{ V}$, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level drain output from clock	$C_L = 30\text{ pF}$, See Figure 1		450		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from clock			550		ns
t_{TLH}	Transition time, low-to-high-level of source-drain output			35		ns
t_{THL}	Transition time, high-to-low-level of source-drain output			30		ns
t_{DLH}	Delay time, low-to-high-level drain output from input	$C_L = 30\text{ pF}$, See Figure 2, $I_D = I_N = 700\text{ mA}$		380		ns
t_{DHL}	Delay time, high-to-low-level drain output from input			380		ns
t_{RLH}	Rise time, low-to-high-level of source-drain output			35		ns
t_{FHL}	Fall time, high-to-low-level of source-drain output			70		ns
t_a	Reverse-recovery-current rise time	$I_F = 3\text{ A}$, See Notes 5 and 6, $di/dt = 100\text{ A}/\mu\text{s}$, See Figure 3		45		ns

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

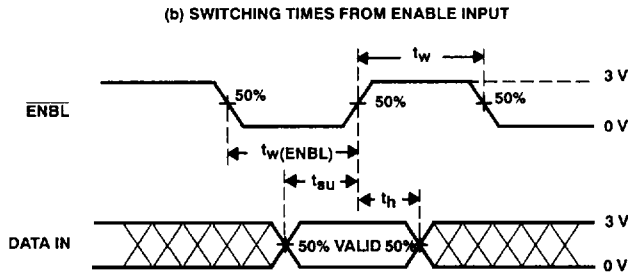
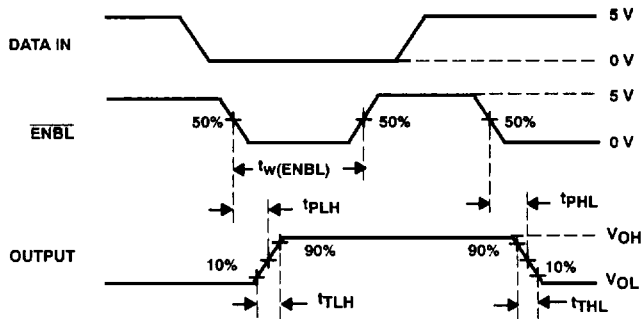
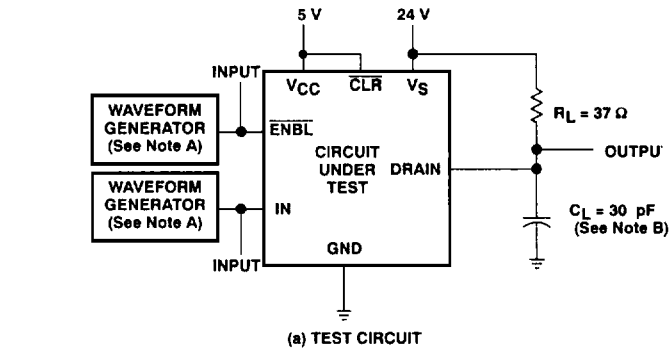
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	All four outputs with equal power			8.33	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance				50	$^\circ\text{C}/\text{W}$

operating characteristics over -40°C to 125°C case temperature range

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Undervoltage shutdown	3		4.5	V
	Thermal shutdown temperature		155		$^\circ\text{C}$
	Thermal shutdown hysteresis		15		$^\circ\text{C}$

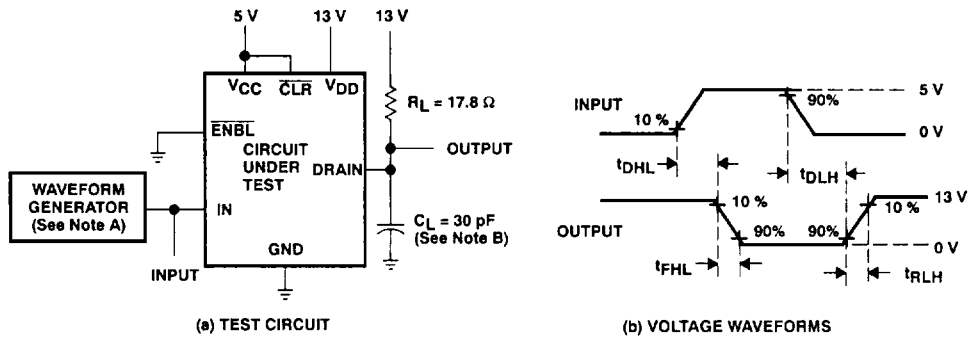
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, PRR = 5 kHz, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

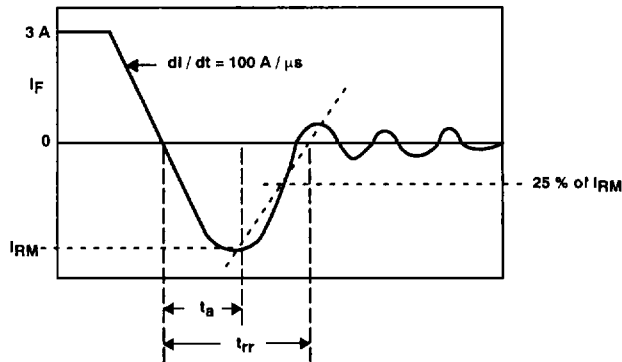
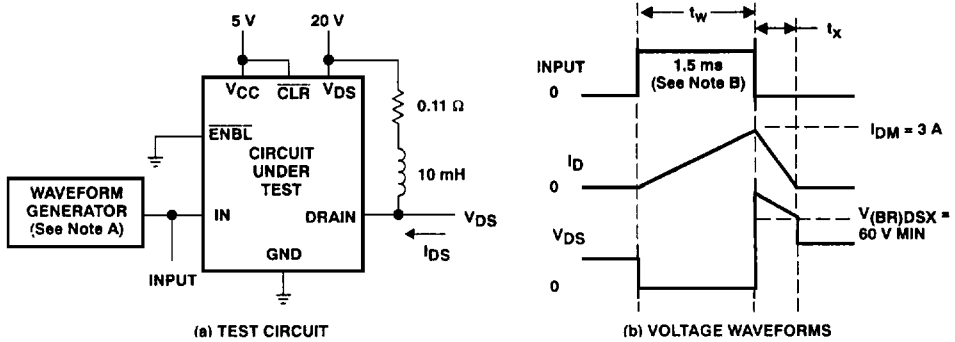


FIGURE 3. REVERSE-RECOVERY-CURRENT WAVEFORMS OF SOURCE-DRAIN DIODE

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 1$ ms, PRR = 5 kHz, $Z_0 = 50 \Omega$.
B. Input pulse duration is increased until peak current $I_{DM} = 3$ A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{DM} \times V_{(BR)DSX} \times t_x}{2} = 50 \text{ mJ min.}$$

FIGURE 4. SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT AND WAVEFORMS

MAXIMUM RATINGS

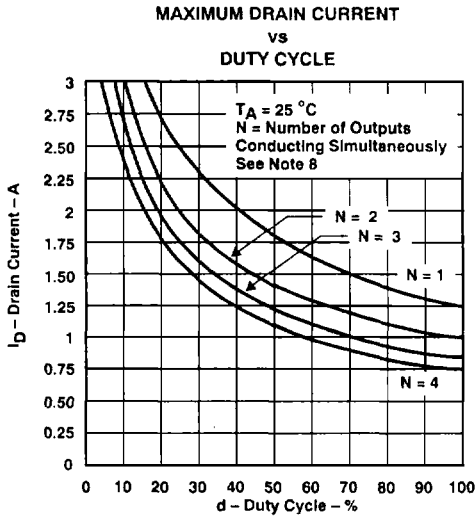


FIGURE 5

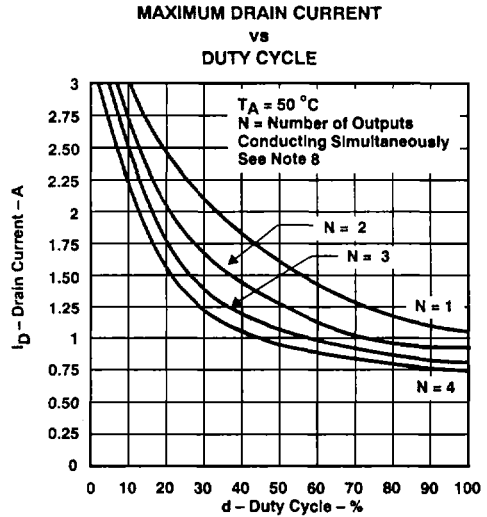


FIGURE 6

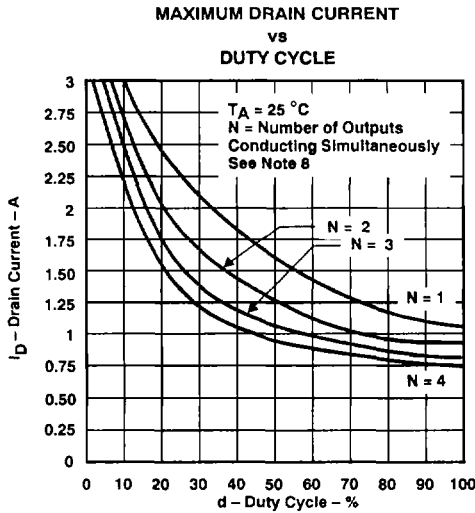


FIGURE 7

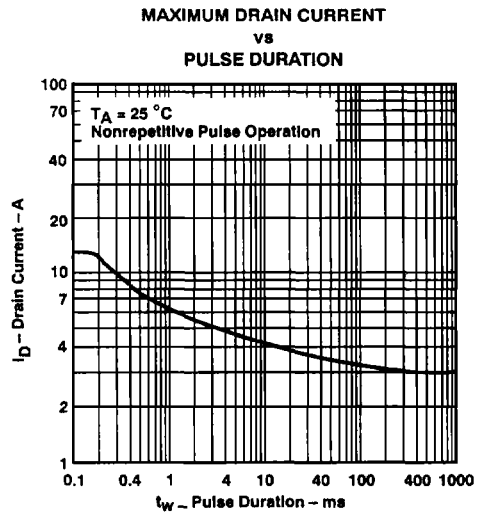
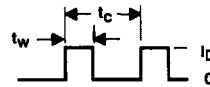


FIGURE 8

NOTE 8: For Figures 5, 6, and 7, $d = \frac{t_w}{t_c} = \frac{10 \text{ ms}}{t_c}$. Where t_w and t_c are defined by the following:



MAXIMUM RATINGS

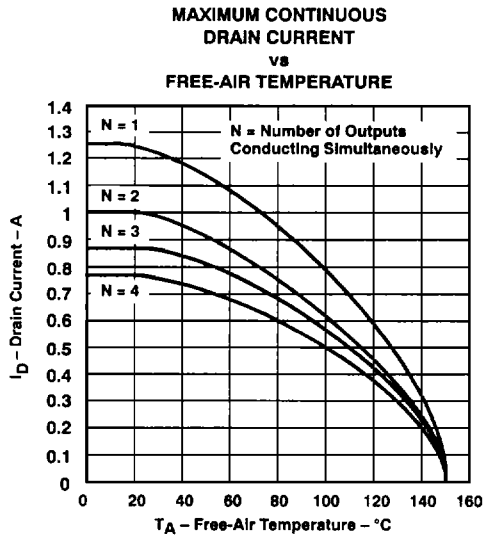


FIGURE 9

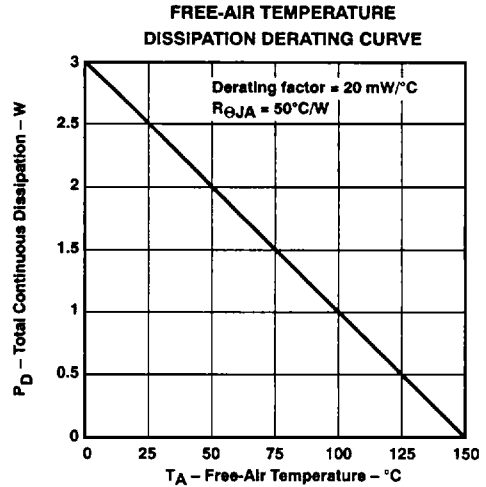


FIGURE 10

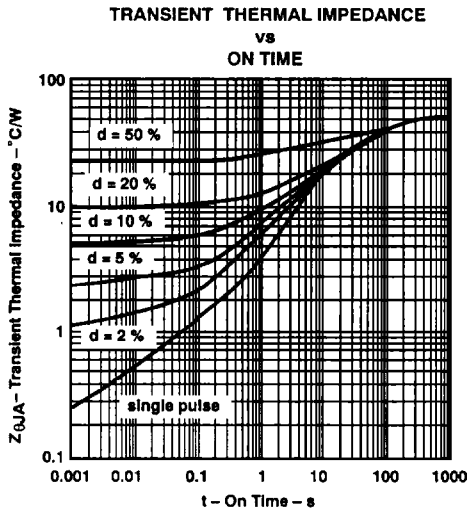


FIGURE 11

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

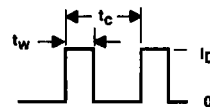
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$$d = t_w/t_c$$



TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE
ON-RESISTANCE
vs
DRAIN CURRENT

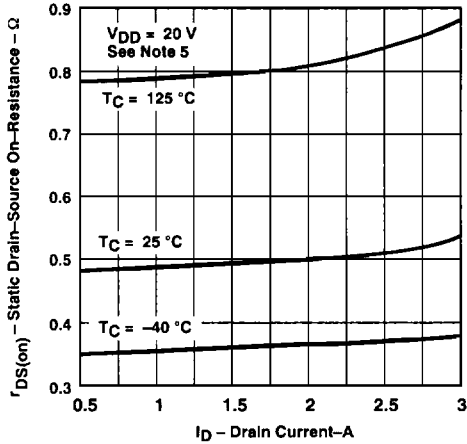


FIGURE 12

STATIC DRAIN-SOURCE
ON-RESISTANCE
vs
POWER MOSFET DRIVER SUPPLY VOLTAGE

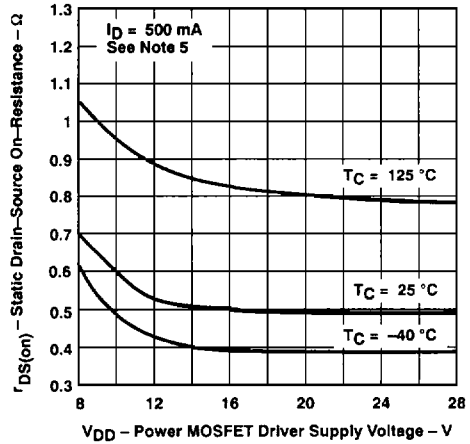


FIGURE 13

NOTE 5: Technique should limit $T_j - T_C$ to 10°C maximum.