

# CD74HC181, CD74HCT181

## High-Speed CMOS Logic 4-Bit Arithmetic Logic Unit

January 1998

**NOT RECOMMENDED FOR NEW DESIGNS**

### Features

- Full Look-Ahead Carry For Speed Operations on Long Words
  - Generates 16 Logic Functions of Two Boolean Variables
  - Generates 16 Arithmetic Functions of Two 4-Bit Binary Words
  - A = B Comparator Output Available (Open Drain)
  - Ripple-Carry Input and Output Available
  - Available in Both Narrow and Wide Body Plastic Packages
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

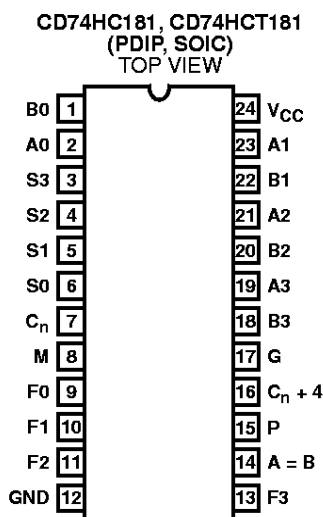
### Description

The Harris CD74HC181 and CD74HCT181 are low power 4-bit parallel arithmetic logic units (ALU) capable of providing 16 binary arithmetic operations on two 4-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and -NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The HC/HCT181 operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs, by using the appropriate truth table.

The CD74HC181 and CD74HCT181 contains logic for full look-ahead carry operation for fast-carry generation using the carry-generate and carry-propagate outputs G and P for the four bits of the CD74HC181 and CD74HCT181. Use of the HC/HCT182 look-ahead carry generator in conjunction with multiple CD74HC181 and CD74HCT181s, permits high-speed arithmetic operations on long words. A ripple-carry output  $C_{n+4}$  is available for use in systems where speed is not of primary importance.

Also included in these devices is a comparator output A = B, which assumes a high level whenever the two 4-bit input words A and B are equal and the device is in the subtract mode. A = B is an open-drain output that can be wire-AND connected to give a comparison for more than four bits. In addition, relative magnitude information may be derived from the carry-in input  $C_n$  and ripple carry-out output  $C_{n+4}$  by placing the unit in the subtract mode and externally decoding using the information in the Magnitude Comparison table.

### Pinout



### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC181E	-55 to 125	24 Ld PDIP	E24.3
CD74HCT181E	-55 to 125	24 Ld PDIP	E24.3
CD74HC181M	-55 to 125	24 Ld SOIC	M24.3
CD74HCT181M	-55 to 125	24 Ld SOIC	M24.3

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

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Functional Diagram

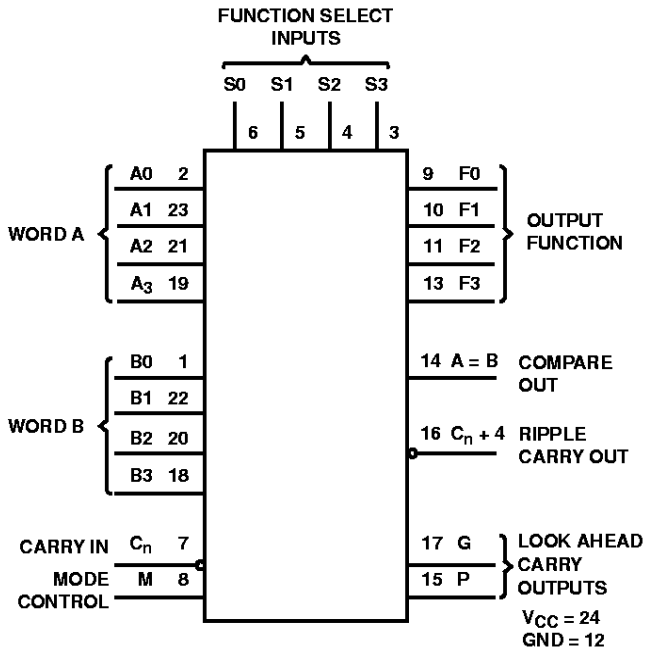


FIGURE 1. ACTIVE-HIGH DATA

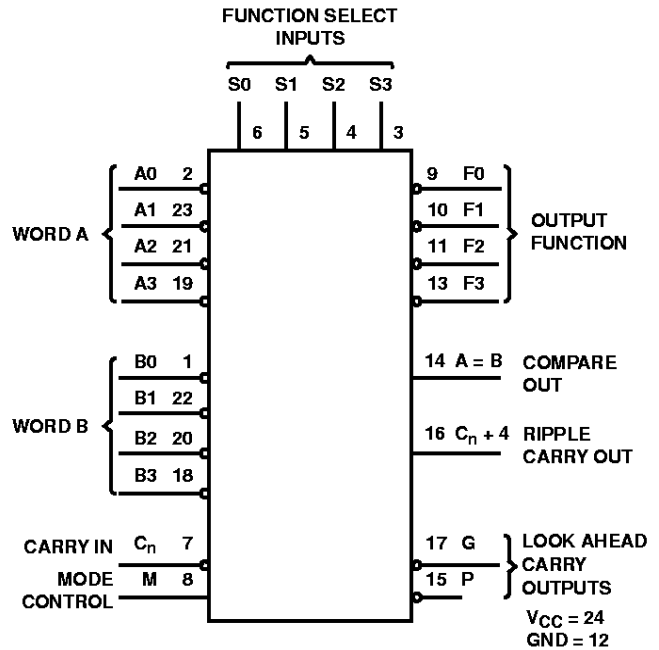


FIGURE 2. ACTIVE-LOW DATA

TRUTH TABLE

FUNCTION SELECT				LOGIC FUNCTION M = H	ARITHMETIC FUNCTION M = L	
S3	S2	S1	S0		C <sub>n</sub> = H (NO CARRY)	C <sub>n</sub> = L (WITH CARRY)
INPUTS/OUTPUTS ACTIVE HIGH						
L	L	L	L	$\bar{A}$	A	A Plus 1
L	L	L	H	$\overline{A + B}$	A + B	(A + B) Plus 1
L	L	H	L	$\bar{A}\bar{B}$	A + $\bar{B}$	(A + $\bar{B}$ ) Plus 1
L	L	H	H	Logic 0	Minus 1 (2's Compl.)	Zero
L	H	L	L	$\bar{A}\bar{B}$	A Plus $\bar{A}\bar{B}$	A Plus $\bar{A}\bar{B}$ Plus 1
L	H	L	H	$\bar{B}$	(A + B) Plus $\bar{A}\bar{B}$	(A + B) Plus $\bar{A}\bar{B}$ Plus 1
L	H	H	L	A $\oplus$ B	A Minus B Minus 1	A Minus B
L	H	H	H	$A\bar{B}$	$A\bar{B}$ Minus 1	$A\bar{B}$
H	L	L	L	$\bar{A} + B$	A Plus AB	A Plus AB Plus 1
H	L	L	H	$\bar{A} \oplus \bar{B}$	A Plus B	A Plus B Plus 1
H	L	H	L	B	(A + $\bar{B}$ ) Plus AB	(A + $\bar{B}$ ) Plus AB Plus 1
H	L	H	H	AB	AB Minus 1	AB
H	H	L	L	Logic 1	A Plus A (Note 4)	A Plus A Plus 1
H	H	L	H	A + $\bar{B}$	(A + B) Plus A	(A + B) Plus A Plus 1
H	H	H	L	A + B	(A + $\bar{B}$ ) Plus A	(A + $\bar{B}$ ) Plus A Plus 1
H	H	H	H	A	A Minus 1	A

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TRUTH TABLE (Continued)

FUNCTION SELECT				LOGIC FUNCTION M = H	ARITHMETIC FUNCTION M = L	
S3	S2	S1	S0		C <sub>n</sub> = H (NO CARRY)	C <sub>n</sub> = L (WITH CARRY)
<b>INPUTS/OUTPUTS ACTIVE LOW</b>						
L	L	L	L	$\bar{A}$	A Minus 1	A
L	L	L	H	$\bar{AB}$	AB Minus 1	AB
L	L	H	L	$\bar{A} + B$	$\bar{AB}$ Minus 1	$\bar{AB}$
L	L	H	H	Logic 1	Minus 1 (2's Compl.)	Zero
L	H	L	L	$\overline{A + B}$	A Plus (A + $\bar{B}$ )	A Plus (A + $\bar{B}$ ) Plus 1
L	H	L	H	$\bar{B}$	AB Plus (A + B)	AB Plus (A + $\bar{B}$ ) Plus 1
L	H	H	L	$\overline{A \oplus B}$	A Minus B Minus 1	A Minus B
L	H	H	H	A + $\bar{B}$	A + $\bar{B}$	(A + $\bar{B}$ ) Plus 1
H	L	L	L	$\bar{AB}$	A Plus (A + B)	A Plus (A + B) Plus 1
H	L	L	H	A $\oplus$ B	A Plus B	A Plus B Plus 1
H	L	H	L	B	$\bar{AB}$ Plus (A + B)	$\bar{AB}$ Plus (A + B) Plus 1
H	L	H	H	A + B	A + B	(A + B) Plus 1
H	H	L	L	Logic 0	A Plus A (Note 4)	A Plus A Plus 1
H	H	L	H	$\bar{AB}$	AB Plus A	AB Plus A Plus 1
H	H	H	L	AB	$\bar{AB}$ Plus A	$\bar{AB}$ Plus A Plus 1
H	H	H	H	A	A	A Plus 1

NOTE:

3. 1 = High Level, 0 = Low Level
4. Each Bit is shifted to the next more significant position.

**MAGNITUDE COMPARISON TABLE**

INPUT C <sub>n</sub>	OUTPUT C <sub>n</sub> + 4	MAGNITUDE
<b>ACTIVE HIGH DATA</b>		
1	1	A ≤ B
0	1	A < B
1	0	A > B
0	0	A ≥ B
<b>ACTIVE LOW DATA</b>		
0	0	A ≤ B
1	0	A < B
0	1	A > B
1	1	A ≥ B

NOTE: 1 = High Level, 0 = Low Level

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## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 5)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	55
SOIC Package .....	75
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

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### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ to GND	0	5.5	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	$\mu A$
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	$\Delta I_{CC}$	$V_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	$\mu A$

NOTE:

6. For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
S0-S3	1
All A and B (Data)	0.75
M, $C_n$	0.5

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu A$  max at 25°C.

### AC Test Setup Reference (Active Low Data)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE
	INPUTS	OUTPUTS	TO GND	TO $V_{CC}$	
SUM <sub>IN</sub> to SUM <sub>OUT</sub>	$\overline{B}0$	Any F	$\overline{B}1, \overline{B}2, \overline{B}3, M, C_n$	ALL $\overline{A}$ 's	ADD
SUM <sub>IN</sub> to $\overline{P}$	$\overline{A}0$	$\overline{P}$	$\overline{A}1, \overline{A}2, \overline{A}3, M, C_n$	ALL $\overline{B}$ 's	ADD
SUM <sub>IN</sub> to $\overline{G}$	$\overline{B}0$	$\overline{G}$	All $\overline{A}$ 's, M, $C_n$	$\overline{B}1, \overline{B}2, \overline{B}3$	ADD
SUM <sub>IN</sub> to $C_{n+4}$	$\overline{B}0$	$C_{n+4}$	All $\overline{A}$ 's, M, $C_n$	$\overline{B}1, \overline{B}2, \overline{B}3$	ADD
$C_n$ to SUM <sub>OUT</sub>	$C_n$	Any F	All $\overline{A}$ 's, M	All $\overline{B}$ 's	ADD

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### AC Test Setup Reference (Active Low Data) (Continued)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE
	INPUTS	OUTPUTS	TO GND	TO V <sub>CC</sub>	
C <sub>n</sub> to C <sub>n+4</sub>	C <sub>n</sub>	C <sub>n+4</sub>	All $\bar{A}$ 's, M	All $\bar{B}$ 's	ADD
SUM <sub>IN</sub> to A = B	$\bar{B}0$	A = B	All A's, B1, B2, B3, M	C <sub>n</sub>	SUBTRACT
SUM <sub>IN</sub> to SUM <sub>OUT</sub> (Logic Mode)	All $\bar{B}$ 's	Any $\bar{F}$	All $\bar{A}$ 's C <sub>n</sub>	M	EXCLUSIVE OR

**NOTES:**

7. ADD Mode: S0, S3 = V<sub>CC</sub>; S1, S2 = GND
8. SUBTRACT Mode: S0, S3 = GND; S1, S2 = V<sub>CC</sub>

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C To 85°C	-55°C To 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, SUM Mode A <sub>n</sub> or B <sub>n</sub> to C <sub>n+4</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	225	280	345	ns
			4.5	-	45	56	69	ns
		C <sub>L</sub> = 15pF	5	19	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	38	48	59	ns
A <sub>n</sub> or B <sub>n</sub> to G	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	210	265	315	ns
			4.5	-	42	53	63	ns
		C <sub>L</sub> = 15pF	5	18	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	36	45	54	ns
A <sub>n</sub> or B <sub>n</sub> to P	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	170	215	255	ns
			4.5	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	29	37	43	ns
A <sub>n</sub> or B <sub>n</sub> to F <sub>n</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	230	290	345	ns
			4.5	-	46	58	69	ns
		C <sub>L</sub> = 15pF	5	19	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	39	49	59	ns
Propagation Delay, DIFF. Mode A <sub>n</sub> or B <sub>n</sub> to C <sub>n+4</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	235	285	355	ns
			4.5	-	47	59	71	ns
		C <sub>L</sub> = 15pF	5	20	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	40	50	60	ns
A <sub>n</sub> or B <sub>n</sub> to G	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	215	270	325	ns
			4.5	-	43	54	65	ns
		C <sub>L</sub> = 15pF	5	18	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	37	46	55	ns
A <sub>n</sub> or B <sub>n</sub> to P	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	170	215	255	ns
			4.5	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	29	37	43	ns

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### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C To 85°C	-55°C To 125°C	UNITS
				TYP	MAX	MAX	MAX	
$A_n$ or $B_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	235	295	355	ns
			4.5	-	47	59	71	ns
		$C_L = 15\text{pF}$	5	20	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	40	50	60	ns
$A_n$ or $B_n$ to $A = B$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	245	305	370	ns
			4.5	-	49	61	74	ns
		$C_L = 15\text{pF}$	5	21	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	42	52	63	ns
Propagation Delay, LOGIC Mode $A_n$ or $B_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	230	290	345	ns
			4.5	-	46	58	69	ns
		$C_L = 15\text{pF}$	5	19	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	39	49	59	ns
Propagation Delay, SUM and DIFF. Modes $C_n$ to $C_{n+4}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	28	35	43	ns
$C_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
		6	-	34	43	51	ns	
		$C_L = 15\text{pF}$	5	17	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	10	10	10	pF
Power Dissipation Capacitance	$C_{PD}$	$C_L = 15\text{pF}$	5	120	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, SUM Mode $A_n$ or $B_n$ to $C_{n+4}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	53	66	80	ns
			$C_L = 15\text{pF}$	5	22	-	-	-
$A_n$ or $B_n$ to G	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	54	53	63	ns
			$C_L = 15\text{pF}$	5	23	-	-	-
$A_n$ or $B_n$ to P	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	41	51	62	ns
			$C_L = 15\text{pF}$	5	17	-	-	-
$A_n$ or $B_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	58	58	69	ns
			$C_L = 15\text{pF}$	5	24	-	-	-
Propagation Delay, DIFF. Mode $A_n$ or $B_n$ to $C_{n+4}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	55	69	83	ns
			$C_L = 15\text{pF}$	5	23	-	-	-
$A_n$ or $B_n$ to G	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	54	54	65	ns
			$C_L = 15\text{pF}$	5	23	-	-	-
$A_n$ or $B_n$ to P	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	40	50	60	ns
			$C_L = 15\text{pF}$	5	17	-	-	-

# CD74HC181, CD74HCT181

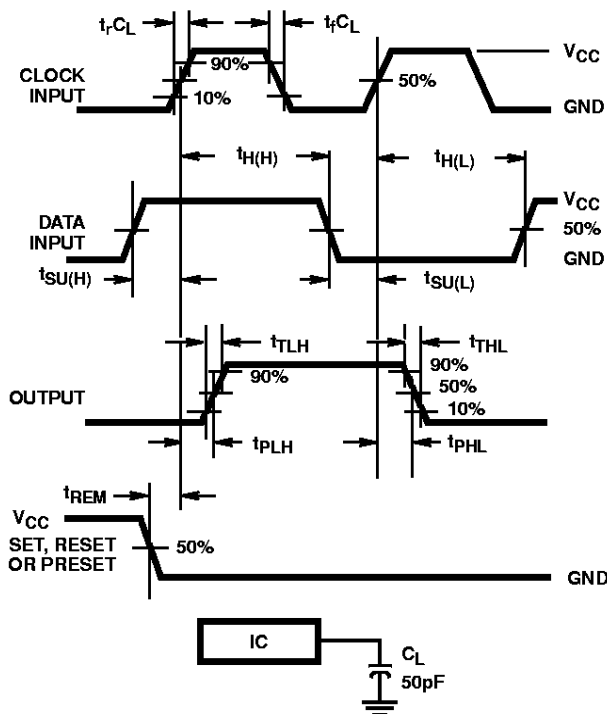
## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C To 85°C	-55°C To 125°C	UNITS
				TYP	MAX	MAX	MAX	
$A_n$ or $B_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	57	71	86	ns
		$C_L = 15\text{pF}$	5	24	-	-	-	ns
$A_n$ or $B_n$ to $A = B$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	60	75	90	ns
		$C_L = 15\text{pF}$	5	25	-	-	-	ns
Propagation Delay, LOGIC Mode $A_n$ or $B_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	54	68	81	ns
		$C_L = 15\text{pF}$	5	23	-	-	-	ns
Propagation Delay, SUM and DIFF. Modes $C_n$ to $C_{n+4}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	42	53	63	ns
		$C_L = 15\text{pF}$	5	18	-	-	-	ns
$C_n$ to $F_n$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	48	56	68	ns
		$C_L = 15\text{pF}$	5	20	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	10	10	10	pF
Power Dissipation Capacitance	$C_{PD}$	$C_L = 15\text{pF}$	5	140	-	-	-	pF

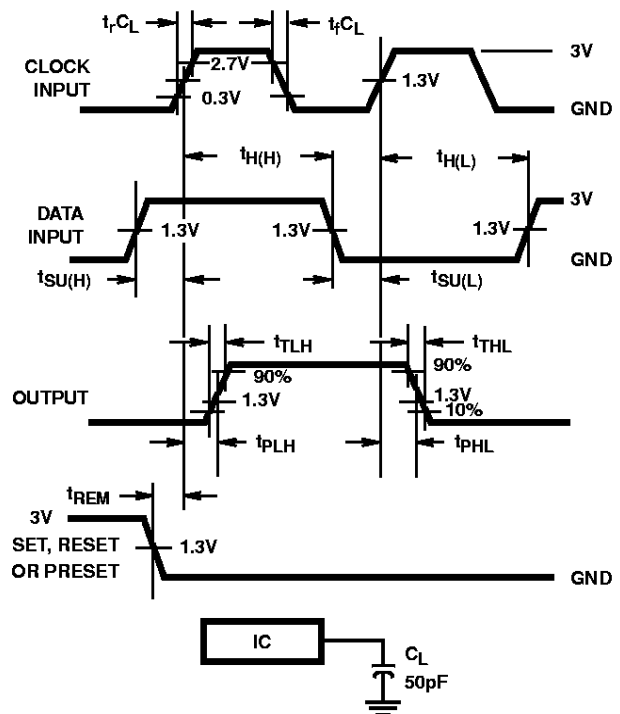
**NOTES:**

9.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
10.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2) f_o$  where  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



**FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**



**FIGURE 4. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**