MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8254	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - Nibble (4 bit) Write
  - Non-Persistent Write-Per-Bit
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low CMOS Standby Current – 10 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8254 VRAM is organized as 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8254 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

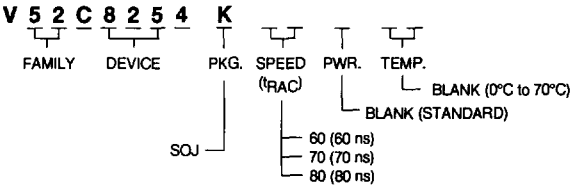
In addition to the conventional multiport video RAM operating modes, the V52C8254 features the nibble write mode, split read/write transfer and block/flash write mode.

The V52C8254 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

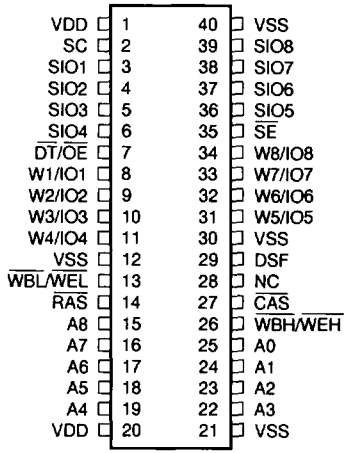
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature Mark
	K	60	70	80	Std	
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WBL/WEL}$	Write per Bit/Write Enable (lower 4 bits)
$\overline{WBH/WEH}$	Write per Bit/Write Enable (higher 4 bits)
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.