Overview

The Direct Rambus™ DRAM (Direct RDRAM™) is a general purpose high-performance memory device suitable for use in a broad range of applications including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The 64/72Mbit Direct Rambus DRAM (Direct RDRAM™) are extremely high-speed CMOS DRAMs organized as 4M words by 16 or 18 bits. The use of Rambus signaling Level (RSL) technology permits 600MHz or 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25ns per two bytes (10ns per sixteen bytes). The architecture of the Direct RDRAMs allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAMís sixteen banks support up to four simultaneous transactions.

System oriented features for mobile, graphics and large memory systems include power management, byte masking, and x18 organization. The two data bits in the x18 organization are general and can be used for additional storage and bandwidth or for error correction.

Features

- Highest sustained bandwidth per DRAM device
  - 1.6GB/s sustained data transfer rate
  - Separate row and column control buses for easy scheduling and highest performance
  - 16 banks: four transactions can take place simultaneously at full bandwidth data rates
- Low latency features
  - Write buffer to reduce read latency
  - 3 precharge mechanisms for controller flexibility
  - Interleaved transactions
- Advanced power management
  - Multiple low power states allows flexibility in power consumption versus time to transition to active state
  - Power-down self-refresh
- Organization: 1Kbyte pages and 16 banks, x16/18
  - x18 organization allows ECC configurations or increased storage/bandwidth
  - x16 organization for low cost applications
- Uses Rambus Signaling Level (RSL) for up to 800MHz operation

Ordering Information

Part Number	Organization [a]	I/O Freq. (MHz)	tRAC (ns)
HYRDU64164M - 60M	256Kx16x16d	600	55
HYRDU64164M - 80M	256Kx16x16d	800	50
HYRDU64164M - 80M	256Kx16x16d	800	45
HYRDU64164M - 80M	256Kx16x16d	800	40
HYRDU72184M - 60M	256Kx18x16d	600	55
HYRDU72184M - 80M	256Kx18x16d	800	50
HYRDU72184M - 80M	256Kx18x16d	600	45
HYRDU72184M - 80M	256Kx18x16d	800	40

a. The "16d" designation indicates that this RDRAM core is composed of 16 banks which use a "double" bank architecture.

Pinouts and Definitions

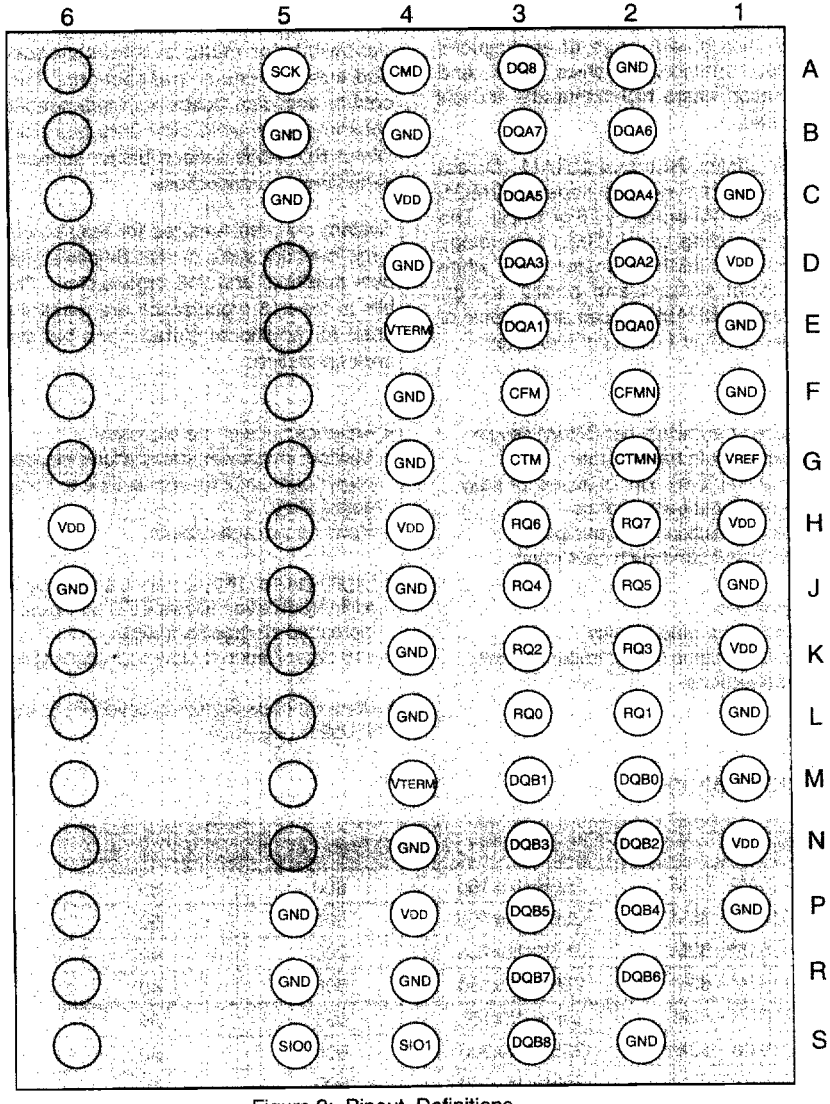


Figure 2: Pinout Definitions

The 64/72Mbit Direct RDRAMs are offered in a uBGA package suitable for desktop as well as low profile add-in card and mobile applications. Direct RDRAMs operate from a 2.5 volt supply.

Pins	Signal	I/O	Type	Description
S4, S5	SIO1, SIO0	I/O		Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
A4	CMD	I	CMOS	Command input. Pins for reading from and writing to the control registers. Also used for power management.
A5	SCK	I	CMOS	Clock input. Clock source used for reading from and writing to the control registers.
C4, D1, H1, H4, H6, K1, N1, P4	V_{DD}			Supply voltage for the RDRAM core and interface logic.
E4, M4	V_{TERM}			Termination voltage for RSL load resistors.
A2, B4, B5, C1, C5, D4, E1, F1, F4, G4, J1, J4, J6, K4, L1, L4, M1, N4, P1, P5, R4, R5, S2,	GND			Ground reference for RDRAM core and interface.
A3, B3, B2, C3, C2, D3, D2, E3, E2	DQA8..DQA0	I/O	RSL	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM.
F3	CFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
F2	CFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
G1	V_{REF}			Logic threshold reference voltage for RSL signals.
G2	CTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
G3	CTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
H2, H3, J2	RQ7..RQ5 or ROW2..ROW0	I	RSL	Row access control. Three pins containing control and address information for row access.
J3, K2, K3, L1, L2, L3	RQ4..RQ0 or COL4..COL0	I	RSL	Column access control. Five pins containing control and address information for column access.
S3, R3, R2, P3, P2, N2, N2, M3, M2	DQB8.. DQB0	I/O	RSL	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM.

Table 1: Pin Descriptions

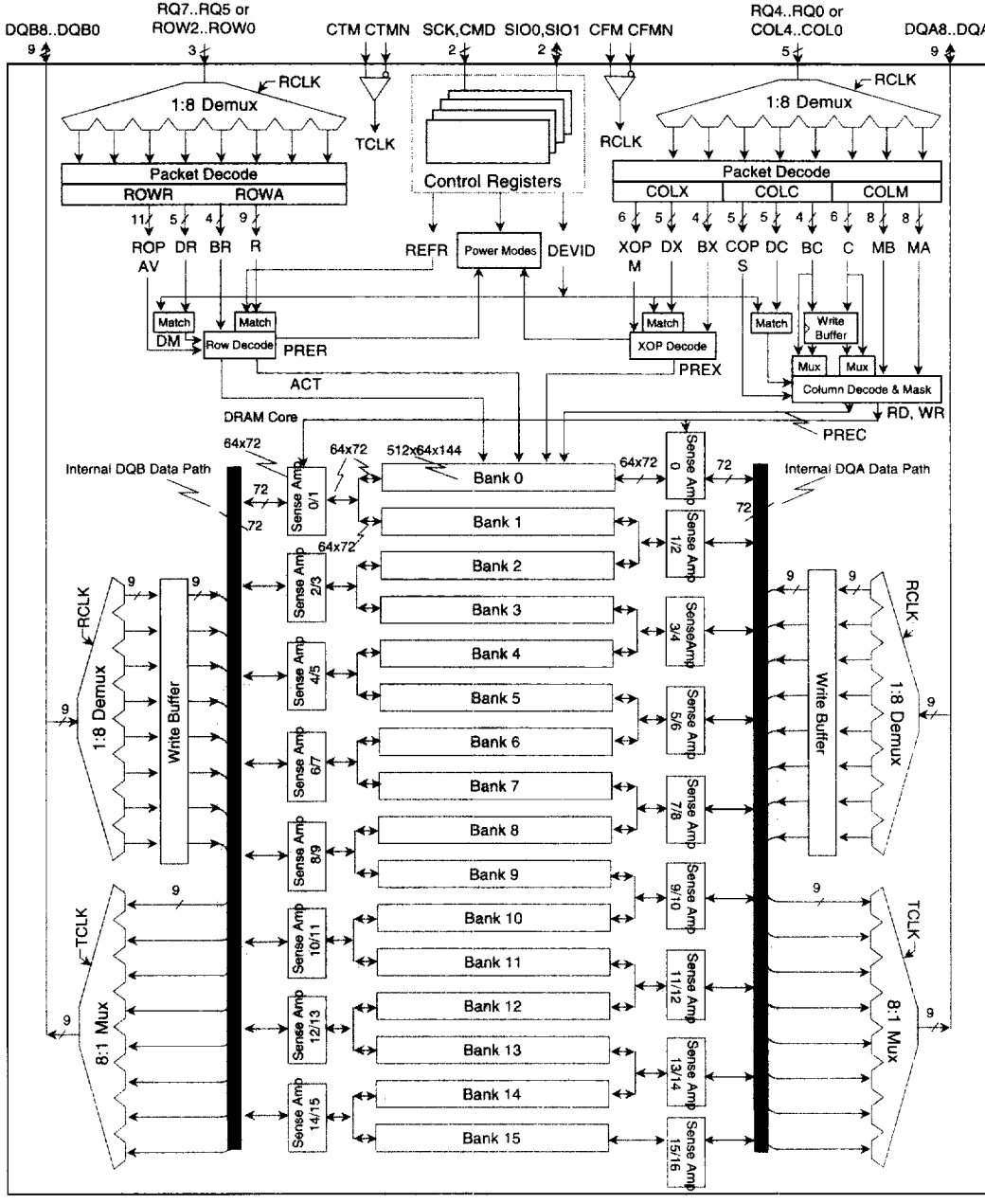


Figure 3: 64/72Mbit Direct RDRAM Block Diagram

General Description

Figure 3 is a block diagram of the 64/72Mbit Direct RDRAM. It consists of two major blocks: a "core" block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus interface block which permits an external controller to access this core at up to 1.6GB/s.

Control Registers: The CMD, SCK, SIO0, and SIO1 pins appear in the upper center of the figure. They are used to write and read a block of control registers.
These registers supply the RDRAM configuration information to a controller and they select the operating modes of the device. The nine bit REFR value is used for tracking the last refreshed row. Most importantly, the five bit DEVID specifies the device address of the RDRAM on the Channel.

Clocking: The CRM and CTMN pins (Clock-To-Master) generate TCLK (Transmit Clock), the internal clock used to transmit read data. The CFM and CFMN pins (Clock-From-Master) generate RCLK (Receive Clock), the internal clock signal used to receive write data and to receive the ROW and COL pins.

DQA, DQB Pins: These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed / de-multiplexed from / to two 72-bit data paths (running at one-eighth the data frequency) inside the RDRAM.

Banks: The 8Mbyte core of the RDRAM is divided into sixteen 0.5Mbyte banks, each organized as 512 rows, with each row containing 64 dualocts, and each dualoct containing 16 bytes. A dualoct is the smallest unit of data that can be addressed.

Sense Amps: The RDRAM contains 17 sense amp arrays. Each sense amp consists of 512 bytes of fast storage and can hold one-half of one row of one bank of the RDRAM. The sense amp may hold any of the 512 half-rows of an associated bank. However, each sense amp is shared between two adjacent banks of the RDRAM (except for number 0 and number 15). This introduces the restriction that adjacent banks may not be simultaneously accessed.

RQ Pins: These pins carry control and address information. They are broken into two groups. RQ7..RQ5 are also called ROW2..ROW0, and are used primarily for controlling row accesses. RQ4..RQ0 are also called COL4..COL0, and are used primarily for controlling column accesses.

ROW Pins: The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM. These pins are de-multiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins: The principle use of these five pins is to manage the transfer of data between the DQA / DQB pins and the sense amps o the RDRAM. These pins are de-multiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17bit COLX (extended-operation) packet.

ACT Command: An ACT (activate) command from an ROWA packet causes one of the 512 rows of the selected bank to be loaded to its two associated sense amps.

PRER Command: A PRER (precharge) command from an ROWR packet causes the selected bank to release its two associated sense amps, permitting a different row to be activated, or permitting adjacent banks to be activated.

RD Command: The RD (read) command causes one of the 64 dualocts of one of the sense amp arrays to be transmitted on the DQA / DQB data pins of the Channel.

WR Command: The WR (write) command causes a dualoct received from the DQA / DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional bytemask) to one of the 64 dualocts of one of the sense amp arrays during a subsequent COP command. A retire can take place during a RD or WR to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD to the same device. The write buffer reduces the delay needed for the internal DQA / DQB data path turn-around.

PREC Precharge: The RDA and WRA commands are similar to RD and WR, except that a precharge operation (PREC) is scheduled at the end of the data transfer. These commands provide a second mechanism for performing precharge.

PREX Precharge: After a RD command, or after a WR command with no byte masking (M=0), a COLX (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

Packet Format

Figure 4 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 2 describes the fields which comprise these packets. DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM.

The AV (ROWA / ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packet provide a five bit device address and a four bit bank address. An ROWA packet uses the remaining bits to specify a nine bit row address, and the ROWR packet uses the remaining bits for an eleven bit opcode field. Note the use of the "RsvX" notation to reserve bits for future address field extension.

Table 2: Field Description for ROWA Packet and ROWR Packet

Field	Description
DR4T,DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR3..DR0	Device address for ROWA or ROWR packet.
BR3..BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits reserved for future address extension.
AV	Selects between ROWA packet (AV=1) and ROWR packet (AV=0).
R8..R0	Row address for ROWA packet. RsvR denotes bits reserved for future row address extension.
ROP10..ROP0	Opcode field for ROWR packet. Specifies precharge, refresh, and power management functions.

Figure 4 also shows the formats of the COLC, COLM, and COLX packets on the COL pins. Table 3 describes the fields which comprise these packets.

The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23 bit COLC packet has a five bit device address, a four bit bank address, a six bit column address, and a four bit opcode. The COLC packet specifies a read or write command, as well as some power management command.

The remaining 17 bits are interpreted as a COLM (M=1) or COLX (M=0) packet.

A COLM packet is used for a COLC write command which needs bytemask control. The COLM packet is linked with the COLC packet from a tRTR earlier. An COLX packet may be used to specify an independent precharge command. It contains a five bit device address, a four bit bank address, and a five bit opcode. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is not linked with a COLC packet except for framing.

Table 3: Field Description for COLC Packet, COLM Packet, and COLX Packet

Field	Description
S	Bits for framing (recognizing) a COLC packet, and independently for framing COLM and COLX packets.
DC4..DC0	Device address for COLC packet.
BC3..BC0	Bank address for COLC packet. RsvB denotes bits reserved for future bank address extension.
C5..C0	Column address for COLC packet. RsvC denotes bits reserved for future column address extension.
COP3..COP0	Opcode field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Selects between COLM packet (M=1) and COLX packet (M=0).
MA7..MA0	Bytemask write control bits. 1=write, 0=no-write. MA0 controls earliest byte on DQA8..0.
MB7..MB0	Bytemask write control bits. 1=write, 0=no-write. MB0 controls earliest byte on DQB8..0.
DX4..DX0	Device address for COLX packet.
BX3..BX0	Bank address for COLX packet. RsvB denotes bits reserved for future bank address extension.
XOP4..XOP0	Opcode field for COLX packet. Specifies precharge, IOL control, and power management functions.

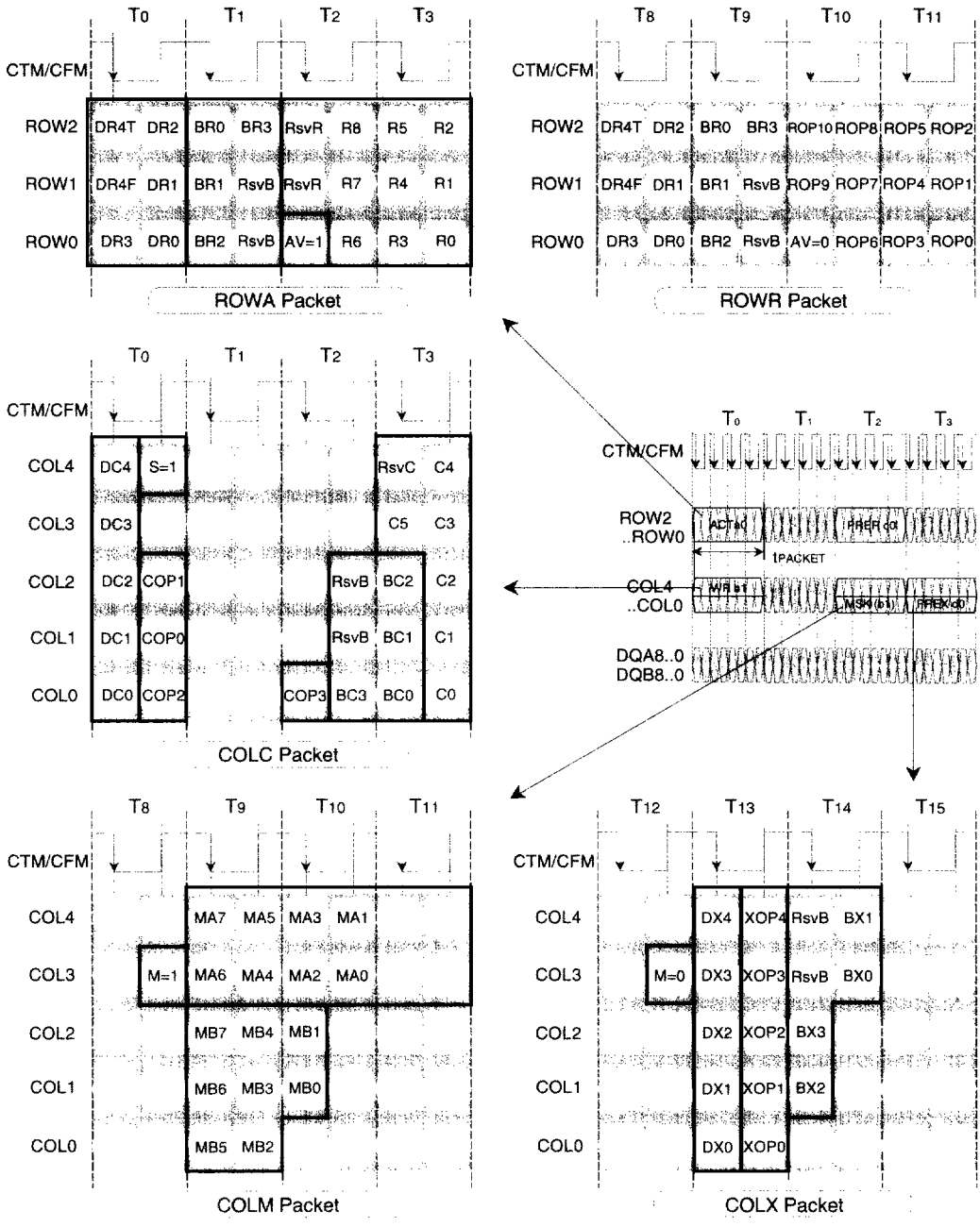


Figure 4: Packet Format

Field Encoding Summary

Table 4 shows how the six device address bits are deocded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (DeviceMatch) signal is asserted and an ACT or ROP command is performed.

Table 4: Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Device Selection	Device Match Signal (DM) [a]
1	1	All devices (broadcast)	DM == 1
0	1	One device selected	DM == 1 if {DEVID4..DEVID0} == {0,DR3..DR0} else DM = 0
1	0	One device selected	DM == 1 if {DEVID4..DEVID0} == {1,DR3..DR0} else DM = 0
0	0	One device selected	DM == 0

a. "/=" means not equal, "==" means equal.

Table 5 shows the encodings of the remaining field of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device (the device with DM asserted) to be loaded into the two associated sense amps.

An ROWR packet is specified when AV is not asserted. An 11 bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its two associated sense amps to precharge, so another row or an adjacent bank may be activated.

The REFA (refresh-activate) command is identical to the ACT command, except the row address comes from an internal register REFR. The REFP (refresh - precharge) command is identical to a PRER command except that REFR is incremented at the largest bank address.

The NAPR, NAPRC, PDNR, and RLXR commands are used for managing the power dissipation of the RDRAM. They are described in more detail in 'Power State Management' on page 34.

Table 5: ROWA Packet and ROWR Packet Field Encodings

DM [a]	DM [a]	ROP10..ROP0 Field									Command Name	Command description
		10	9	8	7	6	5	4	3	2,1,0		
0	x	x	x	x	x	x	x	x	x	xxx	-	-
1	1	x	x	x	x	x	x	x	x	xxx	ACT	Activate row R8..R0 of bank BR3..BR0 or this device.
1	0	1	1	0	0	0	x	x	x	000	PRER	Precharge bank BR3..BR0 of this device.
1	0	0	0	0	1	1	0	0	x	000	REFA	Refresh (activate) row REFR8..REFR0 of bank BR3.. BR0 of this device.
1	0	1	0	1	0	1	0	0	x	000	REFP	Precharge bank BR3..BR0 of this device and increment REFR if BR3..BR0 = 1111.
1	0	x	x	0	0	0	0	1	x	000	PDNR	PowerDown this device
1	0	x	x	0	0	0	1	0	x	000	NAPR	NapDown this device.
1	0	x	x	0	0	0	1	1	x	000	NAPRC	NapDown this device conditionally.
1	0	x	x	x	x	x	x	x	1	000	RLXR	Relax this device.
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

a. The DM (Device Match signal) value is determined by the DR4T,DR4F,DR3..DR0 field of the ROWA and ROWR packets. See Table4.

Table 6 shows the COP field encoding. The COLC packet is used primarily to specify RD (read) and WR (write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See figure 18 for a more detailed description. The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA/WRA commands are equivalent to a RD/WR followed by a PREC. RLXC (relax) performs a power mode transition. See "Power State Management" on page 34.

Table 6: COLC Packet Field Encodings

S	DC4..DC0 (selects one device)	COP 3	COP 2	COP 1	COP 0	Command Name	Command Description
0	xxxxx	x	x	x	x	-	No operation.
1	/=(DEVID4..DEVID0)	x	x	x	x	-	Retire write buffer of this device.
1	==(DEVID4..DEVID0)	x	0	0	0	NOCOP	Retire write buffer of this device.
1	==(DEVID4..DEVID0)	x	0	0	1	WR	Retire write buffer of this device, then write column C5..C0 of bank BC3..BC0 to the write buffer
1	==(DEVID4..DEVID0)	x	0	1	0	RSRV	Reserved, no operation.
1	==(DEVID4..DEVID0)	x	0	1	1	RD	Read column C5..C0 of bank BC3..BC0 of this device.
1	==(DEVID4..DEVID0)	x	1	0	0	PREC	Retire write buffer of this device, then precharge bank BC3..BC0
1	==(DEVID4..DEVID0)	1	1	0	1	WRA	Same as WR, but precharge bank BC3..BC0 after the write buffer (with new data) of this device is retired.
1	==(DEVID4..DEVID0)	x	1	1	0	RSRV	Reserved, no operation.
1	==(DEVID4..DEVID0)	x	1	1	1	RDA	Same as RD, but precharge bank BC3..BC0 afterward.
1	==(DEVID4..DEVID0)	1	x	x	x	RLXA	Relax this device.

Table 7 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two8 bit bytemask fields MA and MB. If the M bit is not asserted, an COLX is specified. It has device and bank address fields, and an opcode field. The primary use of the COLX packet is to permit an independent PREX (precharge) command to be specified without consuming control bandwidth on the ROW pins.

Table 7: COLM packet and COLX Packet Field Encodings

M	DX4..DX0 (selects one device)	XOP 4	XOP 3	XOP 2	XOP 1	XOP 0	Command Name	Command Description
1	xxxxx	x	x	x	x	x	MSK	MB/MA bytemasks used by WR/WRA
0	/=(DEVID4..DEVID0)	x	x	x	x	x	-	No operation.
0	==(DEVID4..DEVID0)	0	0	0	0	0	NOXOP	No operation.
0	==(DEVID4..DEVID0)	1	x	x	x	0	PREX	Precharge bank BX5..BX0 of this device.
0	==(DEVID4..DEVID0)	x	1	x	x	0	rsrv	
0	==(DEVID4..DEVID0)	x	x	1	x	0	rsrv	
0	==(DEVID4..DEVID0)	x	x	x	1	0	RLXX	Relex this device.
0	==(DEVID4..DEVID0)	x	x	x	x	1	RSRV	Reserved, no operation.

DQ Packet Timing

Figure 5 shows the timing relationship of COLC packets with D and Q data packets. This document uses a specific convention for measuring time intervals between packets: all packets on the ROW and COL pins (ROWA, ROWR, COLC, COLM, COLX)use the trailing edge of the packet as a reference point, and all packets on the DQA/DQB pins (D and Q use the leading edge of the packet as a reference point.

An RD or RDA command will transmit a dualoct of read data Q a time tCAC later. This time includes one cycle of round-trip propagation delay on the Channel. A static, programmed delay tRDLY (equal to 0,1, or 2 tCYCLE, depending upon the number of devices on the Channel) is added to tCAC to give the total RD-toQ delay. See Figure 29 for more information.

A WR or WRA command will receive a dualoct of write data D a time tCWD later. This time does not include the round-trip propagation time of the Channel since the COLC and D packets are traveling in the same direction.

When a Q packet follows a D packet (shown on the left side of the figure), a gap must be inserted on the DQA/DQB pins that is equal or greater than the round-trip delay. *The round-trip delay will be 1,2, or 3 cycles*, depending upon the number of devices on the Channel. Because the tCWD value is less than the tCAC+tRDLY value, this will be automatically satisfied. When a WR is immediately followed by a RD on the COL pins, a gap of tCAC+tRDLY-tCWD will appear between the D packet and the Q packet.

When a D packet follows a Q packet (shown on the right side of the figure), no gap on the DQA/DQB pins is *needed. Because the tCWD value is less than the* tCAC+tRDLY value, a gap of tCAC+tRDLY-tCWD or greater must be inserted between the RD command and the WR command on the COL pins.

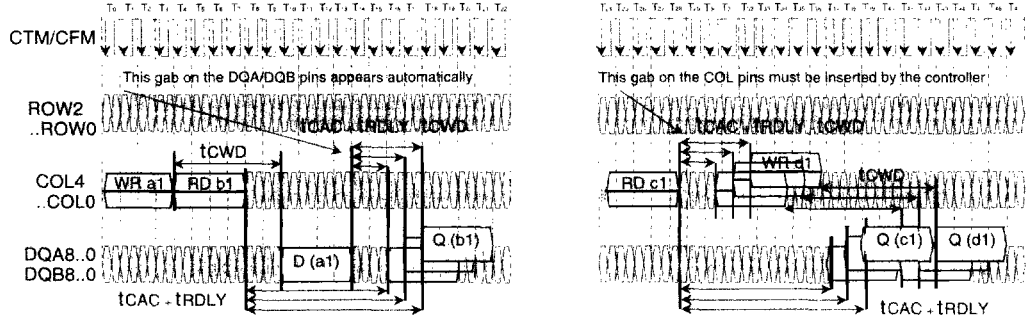


Figure 5: Read (Q) and Write (D) Data Packet - Timing for tRDLY=0,1, or 2 tCYCLE

COLM Packet to D Packet Mapping

Figure 6 shows a write operation initiated by a WR command in a COLC packet. If a subset of the 16 bytes of write data are to be written, then a COLM packet is transmitted on the COL pins a time tRTR after the COLC packet containing the WR command. The M bit of the COLM packet is set to indicate that it contains the MA and MB mask fields. Note that this COLM packet is aligned with the COLC packet which causes the write buffer to be retired. See Figure 18 for more details.

If all 16 bytes of the D data packet are to be written, then no further control information is required. The packet slot that would have been used by the COLM packet (tRTR after the COLC packet) is available to be used as an COLX packet. This could be used for a PREX precharge command or for a housekeeping command (this case is not shown). The M bit is not asserted in an COLX packet and causes all 16 bytes of the previous WR to be written unconditionally. Note that a RD command will never need a COLM packet, and will always be able to use the COLX packet option.

The figure also shows the mapping between the MA and MB fields of the COLM packet and bytes of the D packet on the DQA and DQB pins. Each mask bit controls whether a byte of data is written (=1) or not written (=0).

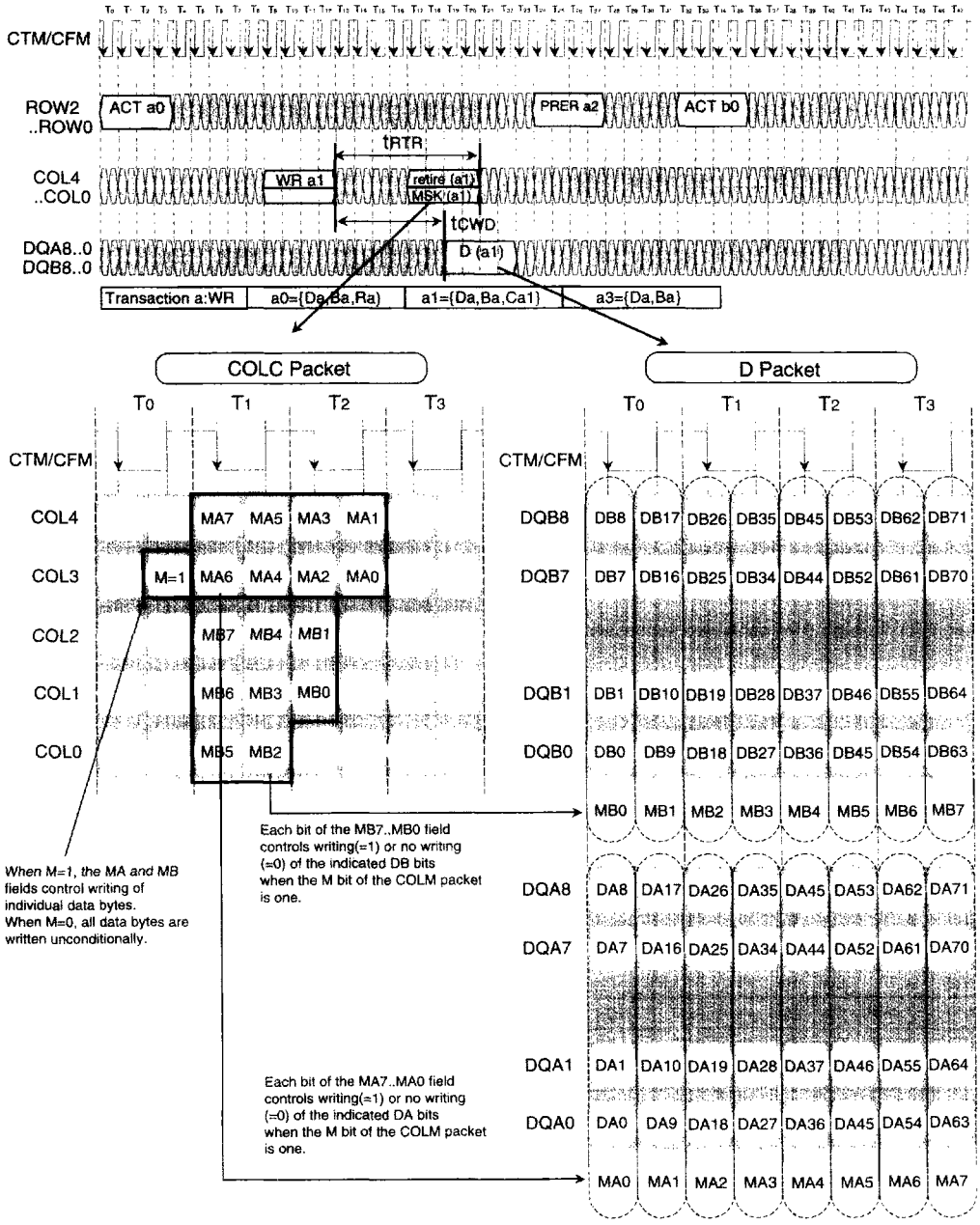


Figure 6: Mapping Between COLM Packet and D Packet for WR Command

ROW-to-ROW Packet Interaction

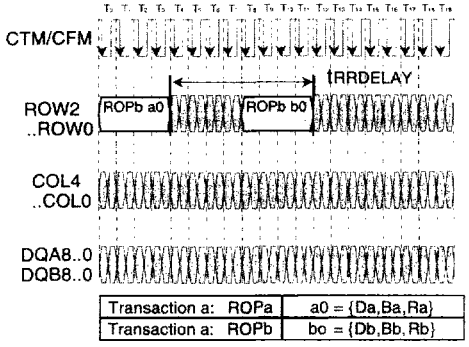


Figure 7: ROW-to-ROW Packet Interaction-Timing

Figure 7 shows two arbitrary packets on the ROW pins separated by an interval tRRDELAY that depends upon the command and addresses in the packets. No other ROW packets are sent to banks {Ba,Ba+1,Ba-1} between packet "a" and packet "b" unless noted otherwise. Table 8 summarizes the tRRDELAY values for all possible cases.

Cases RR1 through RR4 show two successive ACT commands. Figure 11 shows an example of these cases. In case RR1, there is essentially no restriction since the ACT commands are to different devices. In case RR2, the tRR restriction applies to the same device with nonadjacent banks (which do not share sense amps). Cases RR3 and RR4 are illegal unless a PRER Ba command is inserted, in which case the tRRDELAY value is tRC.

Cases RR5 through RR8 show an ACT command followed by a PRER command. In cases RR5 and RR6, there are essentially no restrictions since the commands are to different devices or to non-adjacent banks of the same device. Case RR7 is illegal unless a PRER Ba command is inserted, in which case the tRRDELAY value is tRAS. In case RR8, the tRAS restriction means the activated bank must wait before it can be prechareged. Figure 11 and Figure 12 show these cases.

Cases RR9 through R12 show a PRER command followed by an ACT command. In cases RR9 and RR10, there are essentially no restrictions since the commands are to different devices or to non-adjacent banks of the same device. In case RR11 and RR12, the same and adjacent banks must all wait tRP for the sense amp and bank to precharge before being activated. Figure 11 and Figure 13 show these cases.

Table 8: ROW to ROW Packet interaction - Rules

Case #	ROPa	Da	Ba	Ra	ROPb	Db	Bb	Rb	tRRDELAY
RR1	ACT	Da	Ba	Ra	ACT	/=Da	xxxx	x..x	tPACKET
RR2	ACT	Da	Ba	Ra	ACT	==Da	/={Ba,Ba+1,Ba-1}	x..x	tRR
RR3	ACT	Da	Ba	Ra	ACT	==Da	=={Ba+1,Ba-1}	x..x	tRC - needs PRER Ba first, however
RR4	ACT	Da	Ba	Ra	ACT	==Da	=={Ba}	x..x	tRC - needs PRER Ba first, however
RR5	ACT	Da	Ba	Ra	PRER	/=Da	xxxx	x..x	tPACKET
RR6	ACT	Da	Ba	Ra	PRER	==Da	/={Ba,Ba+1,Ba-1}	x..x	tPACKET
RR7	ACT	Da	Ba	Ra	PRER	==Da	=={Ba+1,Ba-1}	x..x	tRAS - needs PRER Ba first, however
RR8	ACT	Da	Ba	Ra	PRER	==Da	=={Ba}	x..x	tRAS
RR9	PRER	Da	Ba	Ra	ACT	/=Da	xxxx	x..x	tPACKET
RR10	PRER	Da	Ba	Ra	ACT	==Da	/={Ba,Ba+1,Ba-1}	x..x	tPACKET
RR11	PRER	Da	Ba	Ra	ACT	==Da	=={Ba+1,Ba-1}	x..x	tRP
RR12	PRER	Da	Ba	Ra	ACT	==Da	=={Ba}	x..x	tRP
RR13	PRER	Da	Ba	Ra	PRER	/=Da	xxxx	x..x	tPACKET
RR14	PRER	Da	Ba	Ra	PRER	==Da	/={Ba,Ba+1,Ba-1}	x..x	tPP
RR15	PRER	Da	Ba	Ra	PRER	==Da	=={Ba+1,Ba-1}	x..x	tPP
RR16	PRER	Da	Ba	Ra	PRER	==Da	=={Ba}	x..x	tPP

ROW-to-ROW Interaction - continued

Cases RR13 through RR16 summarize the combinations of two successive PRER commands. In case RR13, there is no restriction since two device are addressed. In RR14, tPP applies, since the same device is addressed. In RR15 and RR16, the same bank or an adjacent bank may be given repeated PRER commands with only the tPP restriction. Figure 13 shows RR13 and RR14.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, NAPRC, PNDR, and RLXR commands are discussed in a later section.

ROW-to-COL Packet Interaction

Figure 8 shows two arbitrary packets on the ROW and COL pins. They must be separated by an interval tRCDELAY which depends upon the command and address values in the packets. Table 9 summarizes the tRCDELAY values for all possible cases. Note that if the COL packet is earlier than the ROW packet, it is considered a COL-to-ROW packet interaction.

Cases RC1 through RC5 summarize the rules when the ROW packet has an ACT command. Figure 16 and Figure 17 show examples of RC5 - an activation followed by a read or write. RC4 is an illegal situation, since a read or write of a precharged banks is being attempted (remember that when a bank is activated, Adjacent banks are precharged). In cases RC1,RC2, and RC3, there is no interaction of the ROW and COL packets.

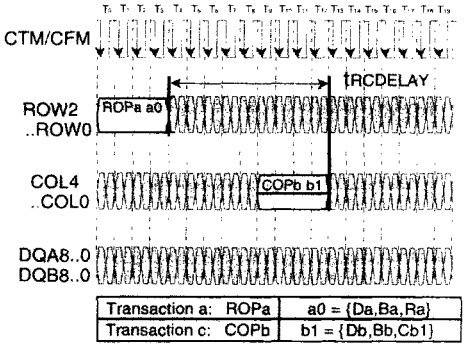


Figure 8: ROW-to-COL Packet Interaction-Timing

Cases RC6 through RC9 summarize the rules when the ROW packet has a PRER command. There is either no interaction (RC6 through RC9) or an illegal situation with a read or write of a precharged bank (RC9).

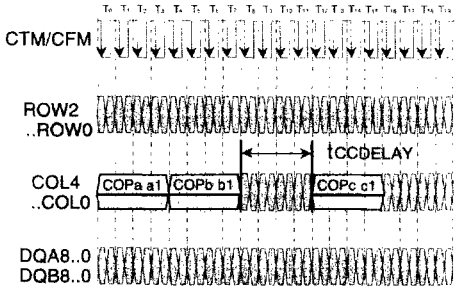
The COL pins can also schedule a precharge operation with a RDA, WRA, or PREC command in a COLC packet or a PREX command in a COLX packet. The constraints of these precharge operations may be converted to equivalent PRER command constraints using the rules summarized in Figure 15.

Table 9: ROW to COL Packet interaction - Rules

Case #	ROPa	Da	Ba	Ra	COPb	Db	Bb	Cb1	tRCDELAY
RC1	ACT	Da	Ba	Ra	NOCOP,RD,WR	/=Da	xxxx	x..x	0
RC2	ACT	Da	Ba	Ra	NOCOP	==Da	xxxx	x..x	0
RC3	ACT	Da	Ba	Ra	RD,WR	==Da	/={Ba,Ba+1,Ba-1}	x..x	0
RC4	ACT	Da	Ba	Ra	RD,WR	==Da	=={Ba+1,Ba-1}	x..x	Illegal
RC5	ACT	Da	Ba	Ra	RD,WR	==Da	=={Ba}	x..x	tRCD
RC6	PRER	Da	Ba	Ra	NOCOP,RD,WR	/=Da	xxx	x..x	0
RC7	PRER	Da	Ba	Ra	NOCOP	==Da	xxx	x..x	0
RC8	PRER	Da	Ba	Ra	RD,WR	==Da	/={Ba}	x..x	0
RC9	PRER	Da	Ba	Ra	RD,WR	==Da	=={Ba}	x..x	Illegal

a. "/=" means not equal; "==" means equal.

COL-to-COL Packet Interaction



Transaction a: COPa	a1 = {Da,Ba,Ca1}
Transaction a: COPb	b1 = {Db,Bb,Cb1}
Transaction a: COPc	c1 = {Dc,Bc,Cc1}

Figure 9: COL-to-COL Packet Interaction-Timing

Figure 9 shows three arbitrary packets on the COL pins. Packets "b" and "c" must be separated by an interval tCCDELAY which depends upon the command and address values in all three packets. Table 10 summarizes the tCCDELAY values for all possible cases.

Cases CC1 through CC5 summarize the rules for every situation other than the case when COPb is a WR command and COPc is a RD command. In CC3, when a RD command is followed by a WR command, a gap of tCAC+tRDLY-tCWD must be inserted between the two COL packets. See Figure 5 for more explanation of why this gap is needed. For cases CC1, CC2, CC4, and CC5, there is no restriction (tCCDELAY is tCC).

In cases CC6 through CC10, COPb is a WR command and COPc is a RD command. The tCCDELAY value needed between these two packets depends upon the command and address in the packet with COPa. In particular, in case CC6 when there is WR-WR-RD command sequence directed to the same device, a gap will be needed between the packets with COPb and COPc. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place. Figure 19 (right) provides a more detailed explanation of this case.

In case CC10, there is a RD-WR-RD sequence directed to the same device. If a prior write to the same device is unretired when COPa is issued, then a gap will be needed between the packets with COPb and COPc as in case CC6. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place.

Cases CC7,CC8, and CC9 have no restriction (tCCDELAY is tCC).

For the purpose of analyzing COL-to-ROW interaction, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation PREC to take place. This precharge may be converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 15.

Table 10: COL-to-COL Packet interaction - Rules

Case #	COPa	Da	Ba	Ca1	COPb	Db	Bb	Cb1	COPc	Dc[a]	Bc	Cc1	tCCDELAY
CC1	xxxx	xxxxx	x..x	x..x	NOCOP	Db	Bb	Cb1	xxxx	xxxxx	x..x	x..x	tCC
CC2	xxxx	xxxxx	x..x	x..x	RD,WR	Db	Bb	Cb1	NOCOP	xxxxx	x..x	x..x	tCC
CC3	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	c
CC4	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	RD	xxxxx	x..x	x..x	tCC
CC5	xxxx	xxxxx	x..x	x..x	WR	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	tCC
CC6	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	tRTR
CC7	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	/= Db	x..x	x..x	tCC
CC8	WR	/=Db	x	x..x	WR	Db	Bb	Cb1	RD	==Db	x..x	x..x	tCC
CC9	NOCOP	==Db	x	x..x	WR	Db	Bb	Cb1	RD	==Db	x..x	x..x	tCC
CC9	RD	==Db	x	x..x	WR	Db	Bb	Cb1	RD	==Db	x..x	x..x	tCC or tRTR[b]

a. "/=" means not equal "==" means equal.
b. If the write buffer was full from an earlier WR command, and had not been retired when COPa=RD is executed, tCCDELAY will be tRTR
c. tCC+tCAC+tRDLY-tCWD

COL-to-ROW Packet Interaction

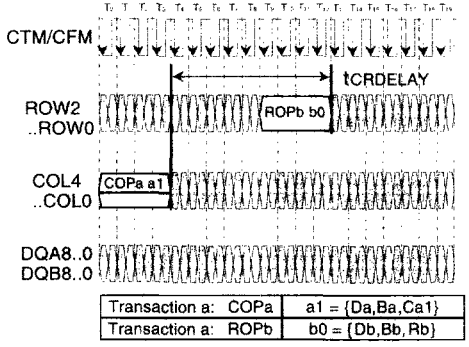


Figure 10: COL-to-ROW Packet Interaction-Timing

Figure 10 shows arbitrary packets on the COL and ROW pins. They must be separated by an interval tCRDELAY which depends upon the command and address values in the packet. Table 11 summarizes the tCRDELAY value for all possible cases.

Case CR1, CR2, CR3, and CR9 show no interaction between the COL and ROW packets, either because one of the command is a NOP or because the packets are directed to different devices or to non-adjacent banks.

Case CR4 is illegal because an already-activated bank is to be re-activated without being precharged.

Case CR5 is illegal because an adjacent bank can't be activated or precharged until bank Ra is precharged first.

In case CR6, the COLC packet contains a RD command, and the ROW packet contains a PRER command for the same bank. The tOFFP parameter specifies the required spacing.

Likewise, in case CR7, the COLC packet causes an automatic retire to take place, and the ROW packet contains a PRER command for the same bank. The tOFFP parameter specifies the required spacing.

Case CR8 is labeled "Hazardous" because a WR command should always be followed by an automatic retire before a precharge is scheduled. Figure 20 shows an example of what can happen when the retire is not able to happen before the precharge.

For the purpose of analyzing COL-to-ROW interactions, the PREC,WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation to take place. This precharge may converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 15.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, PDNR, and RLXR commands are discussed in a later section.

Table 11: COL-to-ROW Packet interaction - Rules

Case #	COPa	Da	Ba	Ca1	ROPb	Db[a]	Bb	Bb	tCCDELAY
CR1	NOCOP	Da	Ba	Ca1	x..x	xxxxx	xxxxx	x..x	0
CR2	RD/WR	Da	Ba	Ca1	x..x	/= Da	xxxxx	x..x	0
CR3	RD/WR	Da	Ba	Ca1	x..x	== Da	/= {Ba,Ba+1,Ba-1}	x..x	0
CR4	RD/WR	Da	Ba	Ca1	ACT	== Da	= {Ba}	x..x	Illegal
CR5	RD/WR	Da	Ba	Ca1	x..x	== Da	= {Ba+1,Ba-1}	x..x	Illegal
CR6	RD	Da	Ba	Ca1	PRER	== Da	= {Ba}	x..x	tOFFP
CR7	retire[a]	Da	Ba	Ca1	PRER	== Da	= {Ba}	x..x	tOFFP
CR8	WR	Da	Ba	Ca1	PRER	== Da	= {Ba}	x..x	Harzardous[b]
CR9	xxxx	Da	Ba	Ca1	NOROP	xxxxx	xxxxx	x..x	0

a. This is any command which permits the write buffer of device Da to retire. Here "Ba" is the bank address in the write buffer.
b. This situation is hazardous because the write buffer will be left unretired while the targeted bank is precharged.

ROW-to-ROW Examples

Figure 11 shows examples of some of the ROW-to-ROW packet spacings from Table 8. A complete sequence of activate and precharge commands is directed to a bank. The RR8 and RR12 rules apply to this sequence. In addition to satisfying the tRAS and tRP timing parameters, the separation between ACT

Commands to the same bank must also satisfy the tRC timing parameter (RR4).

When a bank is activated, it is necessary for adjacent banks to remain precharged. As a result, the adjacent banks will also satisfy parallel timing constraints; in example, the RR11 and RR3 rules are analogous to the RR12 and RR4 rules.

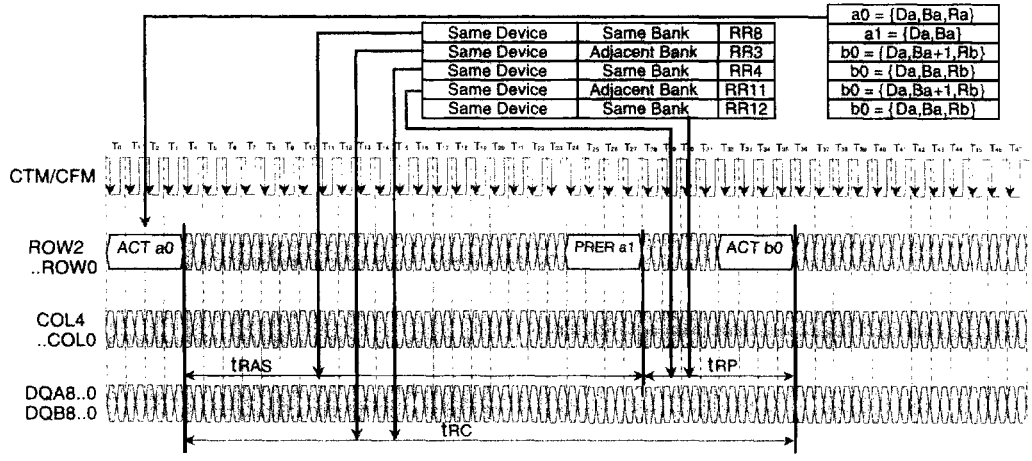


Figure 11: Row Packet Example

Figure 12 shows examples of the ACT-to-ACT (RRO, RR1) and ACT-to-PRER (RR5, RR6) command spacings from table 8. In general, the command in ROW packets may be spaced an interval tPACKET unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.

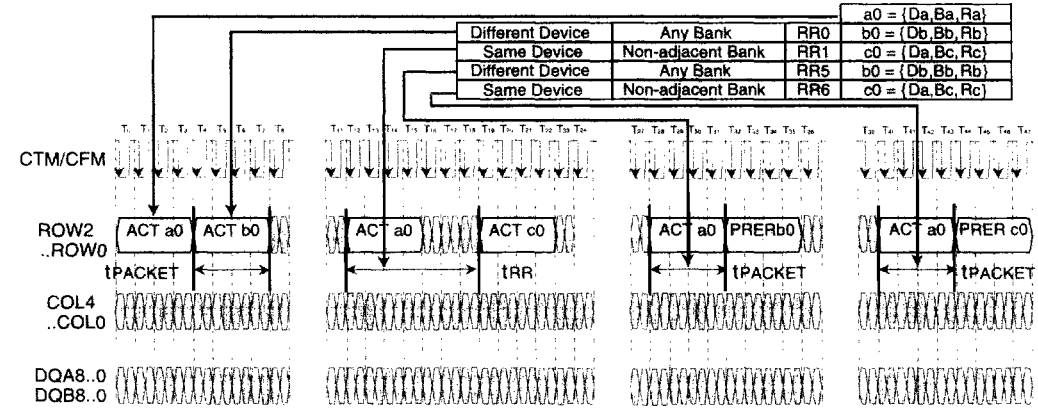


Figure 12: Row Packet Example

Figure 13 shows examples of the PRER-to-PRER (RR13, RR14) and PRER-to-ACT (RR9, RR10) command spacings from Table 8. The RR15 and RR16 cases (PRER-to-PRER to same or adjacent banks) are not shown, but are similar to RR14.

In general, the commands in ROW packets may be spaced an interval tPACKET apart unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.

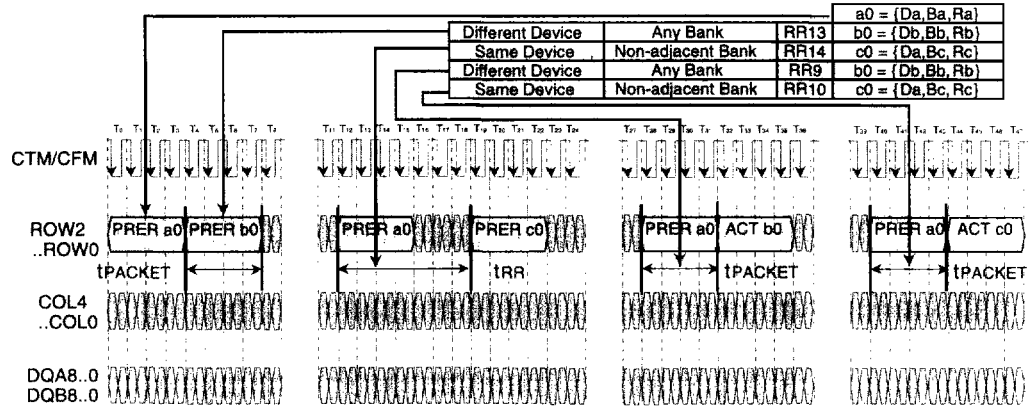


Figure 13: Row Packet Example

Row Cycle Description

Activate: A row cycle begins with the activate (ACT) operation. The activation process is destructive; the act of sensing the value of a bit in a bank's storage cell transfers the bit to the sense amp, but leaves the original bit in the storage cell with an incorrect value.

Restore: Because the activation process is destructive, a hidden operation called restore is automatically performed. The restore operation rewrites the bits in the sense amp back into the storage cells of the activated row of the bank.

Read/Write: While the restore operation takes place, the sense amp may be read (RD) and written (WR) using column operations. If new data is written into the sense amp, it is automatically forwarded to the storage cells of the bank so the data in the activated row and the data in the sense amp remain identical.

Precharge : When both the restore operation and the column operations are completed, the sense amp and bank are precharged (PRE). This leaves them in the proper state to begin another activate operation.

Intervals: The activate operation requires the interval tRCD,MIN to complete. The hidden restore operation requires the interval tRAS,MIN-tRCD,MIN to complete. Column read and write operations are also performed during the tRAS,MIN-tRCD,MIN interval (if more than about four column operations are performed, this interval must be increased). The precharge operation requires the interval tRP,MIN to complete.

Adjacent Banks: An RDRAM with a "d" designation (256Kx16dx16 / 18) indicates it contains "doubled banks". This means the sense amps are shared between two adjacent banks. The only exception is that sense amp 0 and sense amp15 are not shared. When a row in a bank is activated, the two adjacent sense amps are connected to (associated wit) that bank and are not available for use by the two adjacent banks. These two adjacent banks must remain precharged while the selected bank goes through its activate, restore, read/write, and precharge operations.

For example (referring to the block diagram of Figure 3), if bank 5 is accessed, sense amp 4/5 and sense amp 5/6 will both be loaded with one of the 512 rows (with 512 bytes loaded into each sense amp form the 1Kbyte row). While this row from bank 5 is being accessed, no rows may be accessed in banks 4 or 6 because of the sense amp sharing.

Precharge Mechanisms

Figure 14 shows an example of precharge with the ROWR packet mechanism. The PRER command must occur a time tRAS after the ACT command, and a time tRP before the next ACT command. This timing will serve as a baseline against which the other precharge mechanisms can be compared.

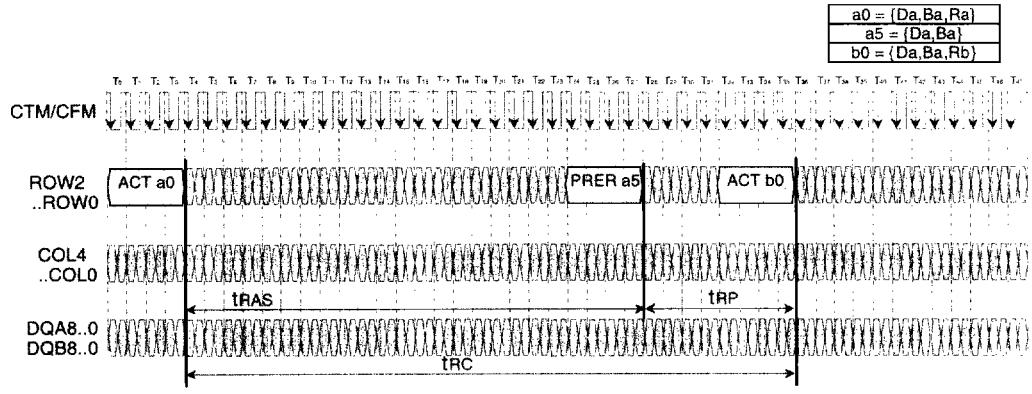


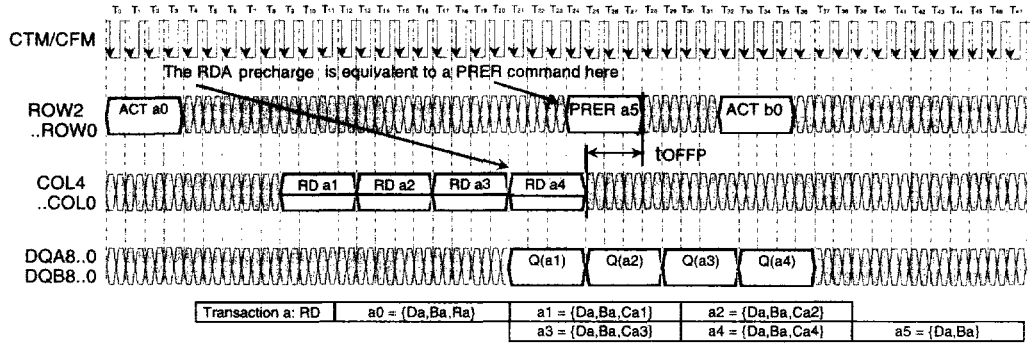
Figure 14: Precharge via PRER Command in ROWR Packet

Figure 15 (top) shows an example of precharge with a RDA command. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these commands is a RDA, which causes the bank to automatically precharge when the final read has finished. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time tOFFP from the COLC packet with the RDA command. The RDA command should be treated as a RD command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets.

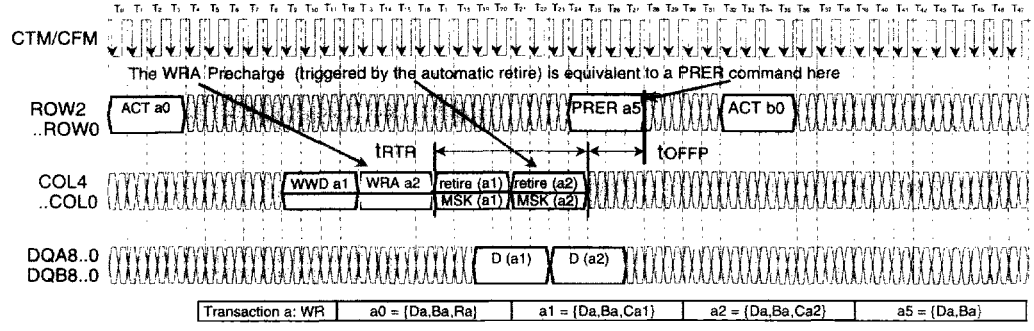
Figure 15 (middle) shows an example of precharge with a WRA command. As in the RDA example, a bank is activated with an ROWA packet on the ROW pins. Then, two dualocts are written with WR commands in COLC packets on the COL pins. The second of these commands is a WRA, which causes the bank to automatically precharge when the final write has been retired. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time tOFFP from the COLC packet that causes the automatic retire. The WRA command should be treated as a WR command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets. Note that the automatic retire is triggered by a COLC packet a time tRTR after the COLC packet with the WR command unless the second COLC contains a RD command to the same device. This is described in more detail in Figure 18.

Figure 15 (bottom) shows an example of precharge with a PREX command in an COLX packet. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COLC pins. The fourth of these COLC packets includes an COLX packet with a PREC command. This causes the bank to precharge with timing equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time tOFFP form the COLX packet with the PREX command.

COLC Packet: RDA Precharge Offset



COLC Packet: WDA Precharge Offset



COLX Packet: PREX Precharge Offset

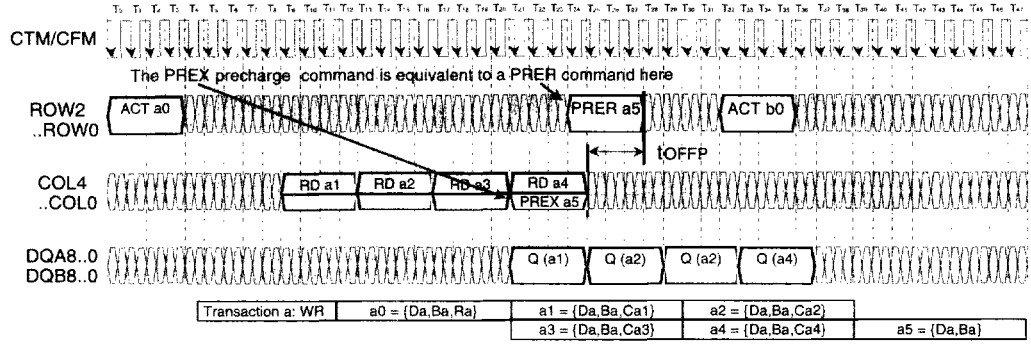


Figure 15: Offsets for Alternate Precharge Mechanisms

Read Transaction - Example

Figure 16 shows an example of a read transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time tRCD later a RD a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the RD command includes device, bank, and column address (abbreviated as a1). A time tCAC after the RD command the read data dualoct Q(a1) is returned by the device (the tRDLY value is assumed to be programmed to zero). Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time tCC after the first COLC packet on the COL pins a second COLC packet is issued. It contains a RD a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time tCAC after the second RD command a second read data dualoct Q(a2) is returned by the device.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated.

The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time tRAS or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the tRAS interval). The PRER command must also occur a time tOFFP or more after the last RD command. Note that the tOFFP value shown is greater than the tOFFP,MIN specification in Table 17. This transaction example reads two dualocts, but there is actually enough time to read up to four dualocts before tOFFP becomes the limiting parameter rather than tRAS.

Finally, an ACTb0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time tRC or more after the first ACT command and a time tRP or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.

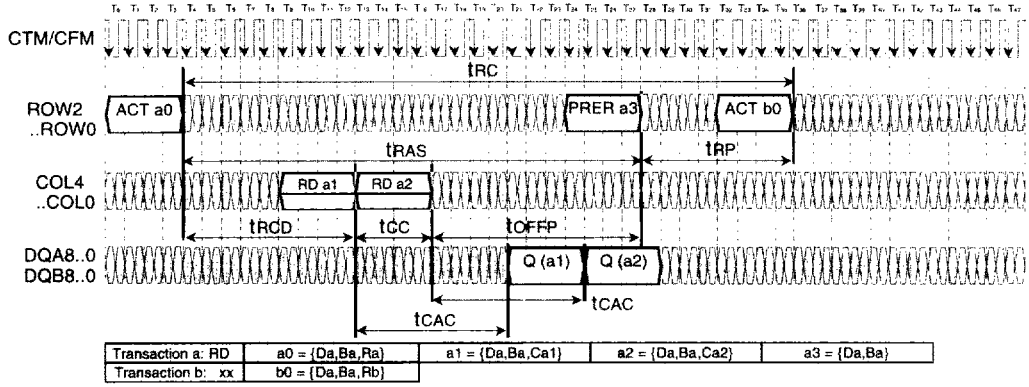


Figure 16: Read Transaction Example

Write Transaction - Example

Figure 17 shows an example of a write transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time tRCD later a WR a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the WR command includes device, bank, and column address (abbreviated as a1). A time tCWD after the WR command the write data dualoct D(a1) is issued. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time tCC after the first COLC packet on the COL pins a second COLC packet is issued. It contains a WR a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time tCWD after the second WR command a second write data dualoct D(a2) is issued.

A time tRTR after each WR command an optional COLM packet MSK (a1) is issued, and at the same time a COLC packet will cause the write buffer to automatically retire. See Figure 18 for more detail on the write / retire mechanism. If a COLM packet is not used, all data bytes are unconditionally written. If the COLC packet which causes the write buffer to retire is delayed, then the COLM packet (if used) must also be delayed.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time tRAS or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the tRAS interval).

A PRER a3 command is issued in an ROWR packet on the ROW pins. The PRER command must occur a time tOFFP or more after the last COLC which causes an automatic retire.

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time tRC or more after the first ACT command and a time tRP or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.

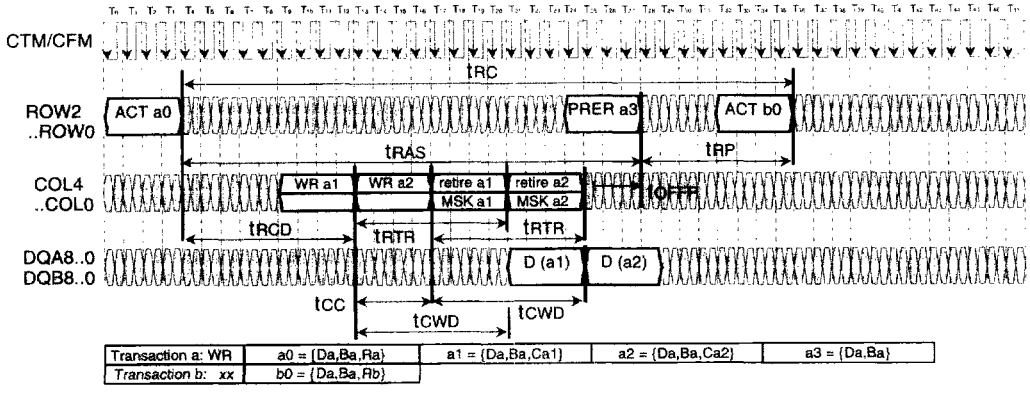


Figure 17: Write Transaction Example

Write / Retire - Examples

The process of writing a dualoct into a sense amp of an RDRAM bank occurs in two steps. The first step consists of transporting the write command, write address, and write data into the write buffer. The second step happens when of the RDRAM automatically retires the write buffer (with an optional byte-mask) into the sense amp. This two-step write process reduces the natural turn-around delay due to the internal bidirectional data pins.

Figure 18 (left) shows an example of this two step process. The first COLC packet contains the WR command and an address specifying device, bank and column. The write data dualoct follows a time tCWD later. This information is loaded into the write buffer of the specified device.

The COLC packet which follows a time tRTR later will retire the write buffer. The retire will happen automatically unless (1) a COLC packet is not framed (the S bit is zero), or (2) the COLC packet contains a RD command to the same device. If the retire does not take place at time tRTR after the original WR command, then the device continues to frame COLC packets, looking for the first that is not a RD directed to itself. A bytemask MSK (a1) may be supplied in a COLM packet aligned with the COLC that retires the write buffer at time tRTR after the WR command.

The memory controller must be aware of this two-step write/retire process. Controller performance can be improved, but only if the controller design accounts for several side effects.

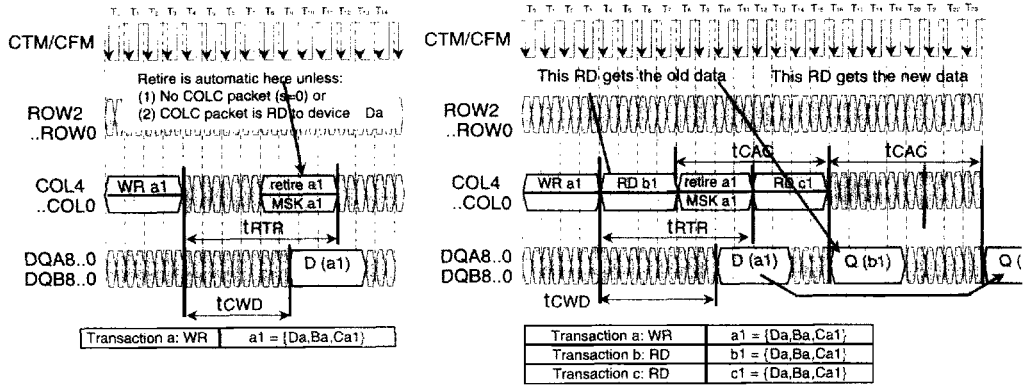


Figure 18: Normal Retire (left) and Retire/Read Ordering (right)

Figure 18 (right) shows the first of these side effects. The first COLC packet has a WR command which loads the address and data into the write buffer. The third COLC causes an automatic retire of the write buffer to the sense amp. The second and fourth COLC packets (which bracket the retire packet) contain RD commands with the same device, bank and column address as the original WR command. In other words, the same dualoct address that is written is read both before and after it is actually retired. The first RD returns the old dualoct value from the sense amp before it is overwritten. The second RD returns the new dualoct value that was just written.

Figure 19 (left) shows the result of performing a RD command to the same device in the same COLC packet slot that would normally be used for the retire Operation.

The read may be to any bank and column address; all that matters is that it is to the same device as the WR command. The retire operation and MSK(a1) will be delayed by a time tPACKET as a result. If the RD command used the same bank and column address as the WR command, the old data from the sense amp would be returned. If many RD commands to the same device were issued instead of the single one that is shown, then the retire operation would be held off an arbitrarily long time. However, once a RD to another device or a WR or NOCOP to any device is issued, the retire will take place. Figure 19 (right) illustrates a situation in which the controller wants to issue a WR-WR-RD COLC packet sequence, with all commands addressed to the same device, but addressed to any combination of banks and columns.

Write / Retire - Examples - continued

The RD will prevent a retire of the first WR from automatically happening. But the first dualoct D(a1) in the write buffer will be overwritten by the second WR dualoct D(b1) if the RD command is issued in the third COLC packet.

Therefore, it is required that for this situation that the controller issue a NOCOP command in the third COLC packet, delaying the RD command by a time of tPACKET. This situation is explicitly shown in Table 10 for the cases in which tCCDELAY is equal to tRTR.

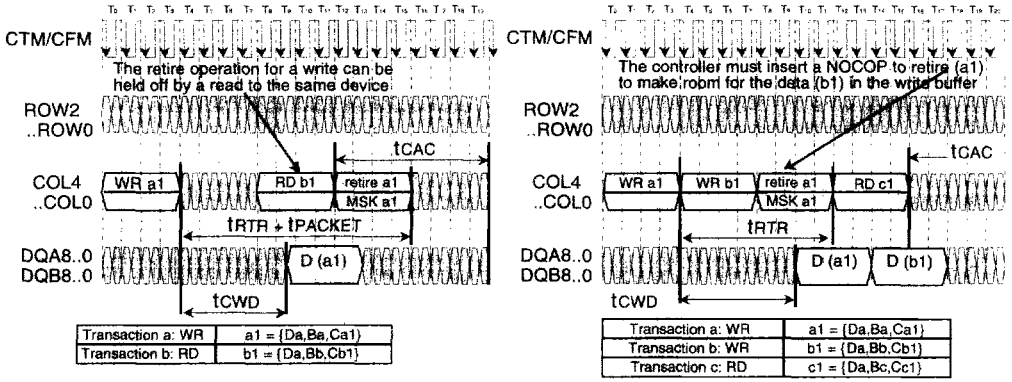


Figure 18: Normal Retire (left) and Retire/Read Ordering (right)

Figure 20 shows a possible result when a retire is held off for a long time (an extended version of Figure 19 left). After a WR command, a series of six RD commands are issued to the same device (but to any combination of bank and column addresses). In the meantime, the bank Ba to which the WR command was originally directed is precharged, and a different row Rc is activated. When the retire is automatically performed, it it made to this new row, since the write buffer only contains the bank and column address, not the row address. The controller can insure that this doesnít happen by never precharging a bank with an unretired write buffer. Note that in a system with more than one RDRAM, there will never be more than two RDRAMs with unretired write buffers. This is because a WR command issued to one device automatically retires the write buffer of all other devices written a time tRTR before or earlier.

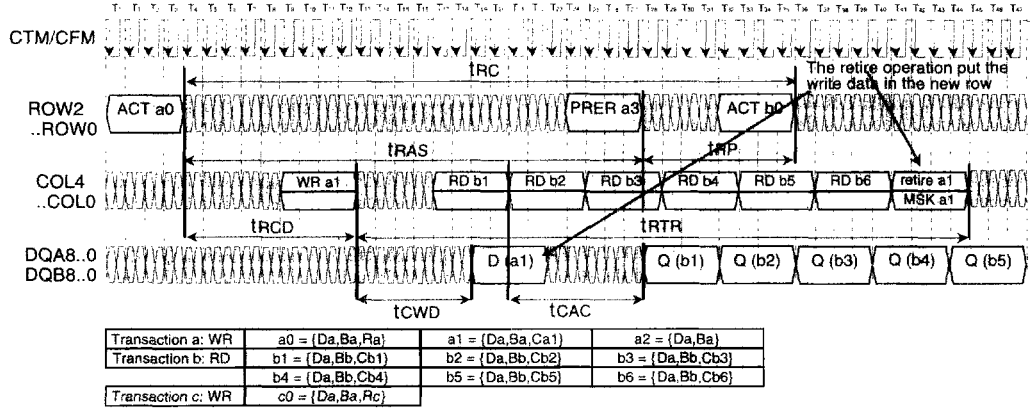


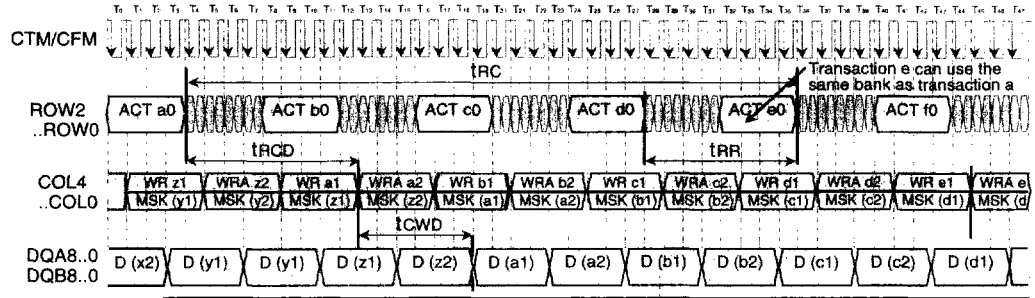
Figure 20: Retire Held Off by Reads to Same Device, Write Buffer Retired to New Row

Interleaved Write - Example

Figure 21 shows an example of an interleaved write transaction. Transactions similar to the one presented in Figure 17 are directed to non-adjacent banks of a single RDRAM. This allows a new transaction to be issued once every tRR interval rather than once every tRC interval (four times more often). The DQ data pin efficiency is 100% with this sequence.

With two dualocts of data written per transaction, the COL, DQA, and DQB pins are fully utilized. Banks are precharged using the WRA autoprecharge option rather than the PRER Rather than the PRER command in an ROWR packet on the ROW pins.

In this example, the first transaction is directed to device Da and bank Ba. The next three transactions are directed to the same device Da, but need to use different, non-adjacent banks Bb, Bc, Bd so there is no bank conflict. The fifth transaction could be redirected bank to bank Ba without interference, since the first transaction would have completed by then (tRC has elapsed). Each transaction may use any value of row address (Ra, Rb, ..) and column address (Ca1, Ca2, Cb1, Cb2,..).



Transaction y: WR	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2 = {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: WR	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2 = {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2 = {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2 = {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: WR	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2 = {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: WR	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2 = {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	c0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2 = {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 21: Interleaved Write Transaction with Two Dualoct Data Length

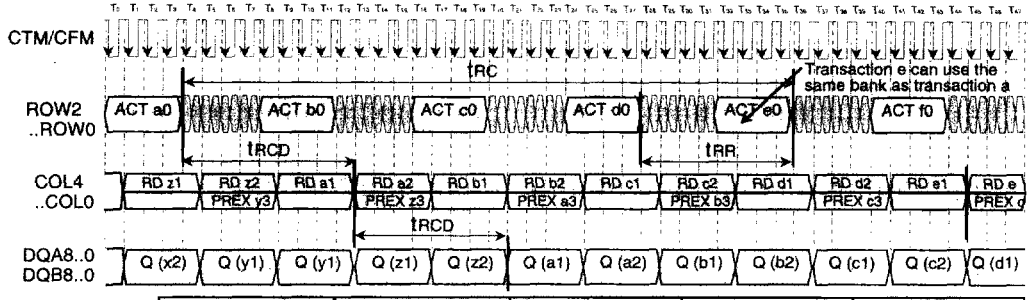
Interleaved Write - Example

Figure 22 shows an example of interleaved read transactions. Transactions similar to the one presented in figure 16 are directed to non-adjacent banks of a single RDRAM. The address sequence is identical to the one used in the previous write example. The DQ data pins efficiency is also 100%. The only difference with the write example (aside from the use of the RD command rather than the WR command) is the use of the PREX command in a COLX packet to precharge the banks rather than the WRA command. This is done because the PREX is not available for a masked write transaction.

Interleaved RRWW - Example

Figure 23 shows a steady-state sequence of 2-dualoct RD / RD / WR / WR..transactions directed to non-adjacent banks of a single RDRAM. This is similar to the interleaved write and read examples in Figure 21 and Figure 22 except that bubble cycles need to be inserted by the controller at read/write boundaries. The DA data pin efficiency for the example in Figure 23 is 32 / 38 or 84%. If there were more RDRAMs on the Channel, the DQ pin efficiency would approach 32 / 34 or 94% for the two-dualoct RRWW sequence (this case is not shown).

In Figure 23, the first bubble type tCBUB1 is inserted by the controller between a RD and WR command on the COL pins. This bubble accounts for the round-trip propagation delay that is seen by read data, and is explained in detail in Figure 5. This bubble appears on the DQA and DQB pins as tDBUB1 between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as tRBUB1.

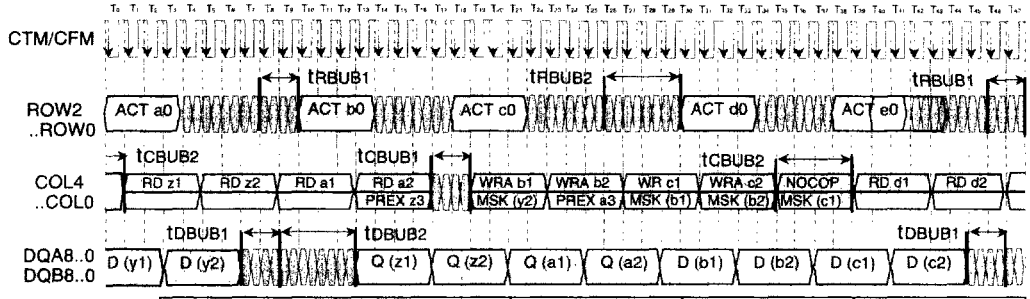


Transaction y: RD	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2 = {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: RD	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2 = {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: RD	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2 = {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: RD	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2 = {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2 = {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2 = {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: RD	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2 = {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

Figure 22: Interleaved Read Transaction with Two Dualoct Data Length

The second bubble type tCBUB2 is inserted (as a NOCOP command) by the controller between a WR and RD command on the COL pins when there is a WR-WR-RD sequence to the same device. This bubble enables write data to be retired from the write buffer without being lost, and is explained in detail in Figure 19.

There would be no bubble if address c0 and address d0 were directed to different devices. This bubble appears on the DQA and DQB pins as the DBUB2 between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as tRBUB2.



Transaction y: WR	y0 = {Da,Ba+6,Ry}	y1 = {Da,Ba+6,Cy1}	y2 = {Da,Ba+6,Cy2}	y3 = {Da,Ba+6}
Transaction z: RD	z0 = {Da,Ba+8,Rz}	z1 = {Da,Ba+8,Cz1}	z2 = {Da,Ba+8,Cz2}	z3 = {Da,Ba+8}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2 = {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2 = {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2 = {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba+8,Re}	e1 = {Da,Ba+8,Ce1}	e2 = {Da,Ba+8,Ce2}	e3 = {Da,Ba+8}
Transaction f: WR	c0 = {Da,Ba,Rf}	f1 = {Da,Ba,Cf1}	f2 = {Da,Ba,Cf2}	f3 = {Da,Ba}

Figure 23: Interleaved RRWW Sequence with Two Dualoct Data Length

Control Register Transactions

The RDRAM has two CMOS input pins SCK and CMD and two COMS input / output pins SIO0 and SIO1. These provide serial access to a set of control registers in the RDRAM. These control registers provide configuration information to the controller during the initialization process. They also allow an application to select the appropriate operating mode of the RDRAM.

SCK (serial clock) and CMD (command) are driven by the controller to all RDRAMs in parallel. SIO0 and SIO1 are connected (in a daisy chain fashion) from one RDRAM to the next. These two pins are initially identical and are automatically configured into SIOIN (the pin closer to the controller) and SIOOUT (the pin further from the controller) at initialization. In normal operation, the data on SIOIN is repeated on SIOOUT, which connects to SIOIN of the next RDRAM.

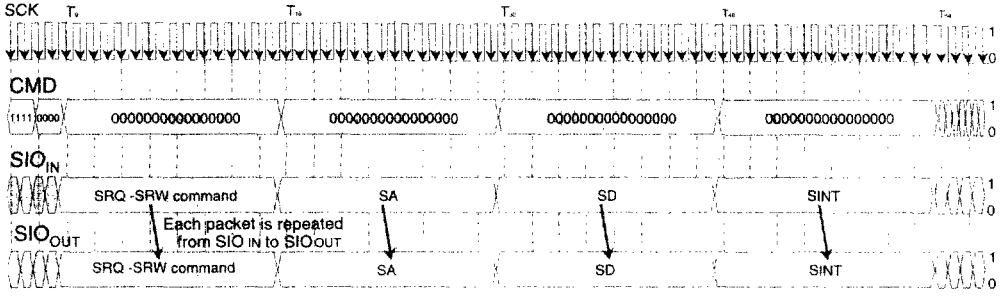


Figure 24: Serial Write (SWR) Transaction to Control Register

Write and read transactions are each composed of four packets, as shown in Figure 24 and Figure 25. Each packet consists of 16 bits, as summarized in Table 12 and Table 13. The packet bits are sampled on the falling edge of SCK. A transaction begins with a SRQ (Serial Request) packet . This packet is framed with a 11110000 pattern on the CMD input (note that the CMD bits are sampled on both the falling edge and the rising edge of SCK). The SRQ packet contains the SOP3..SOP0 (Serial Opcode) field, which selects the transaction type. The SDEV4..SDEV0 (Serial Device address) selects one of the 32 RDRAMs. If SBC (Serial Broadcast) is set, ten all RDRAMs are selected. The Sa (Serial Address) packet contains a 12 bit address for selecting a control register.

A write transaction has a SD (Serial Data) packet next. This contains 16 bits of data that is written into the selected control register. A SNT (Serial Interval) packet is last, providing some delay for any side-effects to take place. A read transaction has a SINT packet, then a SD packet. This provides delay for the selected RDRAM to access the control register. The SD read data packet travels in the opposite direction (towards the controller) as the other packet types. The SCK cycle time can accommodate the total propagation delay.

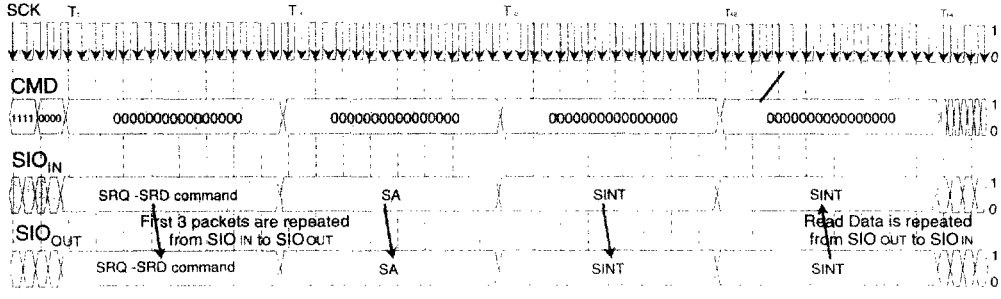


Figure 25: Serial Read (SRD) Transaction to Control Register

Control Register Packet

Table 12 summarizes the formats of the four packet types for control register transactions. Table 13 summarizes the fields that are used within the packets.

Figure 26 shows the transaction format for the SETR, CLRR, and SETF commands. These transactions consist of a single SRQ packet, rather than four packets like the SWR and SRD commands. The same framing sequence on the CMD input is used, however. These commands are used during initialization prior to any control register read or write transaction.

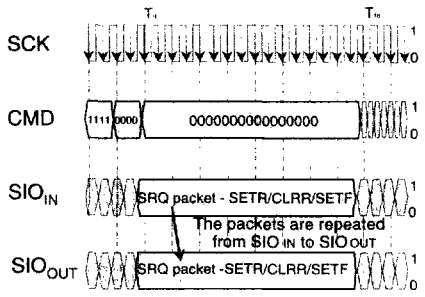


Figure 26: SETR, CLRR, SETF Transaction

Table 12: Control Register Packet Formats

SCK Cycle	SIOIN or SIOOUT for SRQ	SIOIN or SIOOUT for SA	SIOIN or SIOOUT for SINT	SIOIN or SIOOUT for SD	SCK Cycle	SIOIN or SIOOUT for SRQ	SIOIN or SIOOUT for SA	SIOIN or SIOOUT for SINT	SIOIN or SIOOUT for SD
0	rsrv	rsrv	0	SD15	8	SOP1	SA7	0	SD7
1	rsrv	rsrv	0	SD14	9	SOP2	SA6	0	SD6
2	rsrv	rsrv	0	SD13	10	SBC	SA5	0	SD5
3	rsrv	rsrv	0	SD12	11	SDEV4	SA4	0	SD4
4	rsrv	SA11	0	SD11	12	SDEV3	SA3	0	SD3
5	rsrv	SA10	0	SD10	13	SDEV2	SA2	0	SD2
6	rsrv	SA9	0	SD9	14	SDEV1	SA1	0	SD1
7	rsrv	SA8	0	SD8	15	SDEV0	SA0	0	SD0

Table 13: Field Description for Control Register Packets

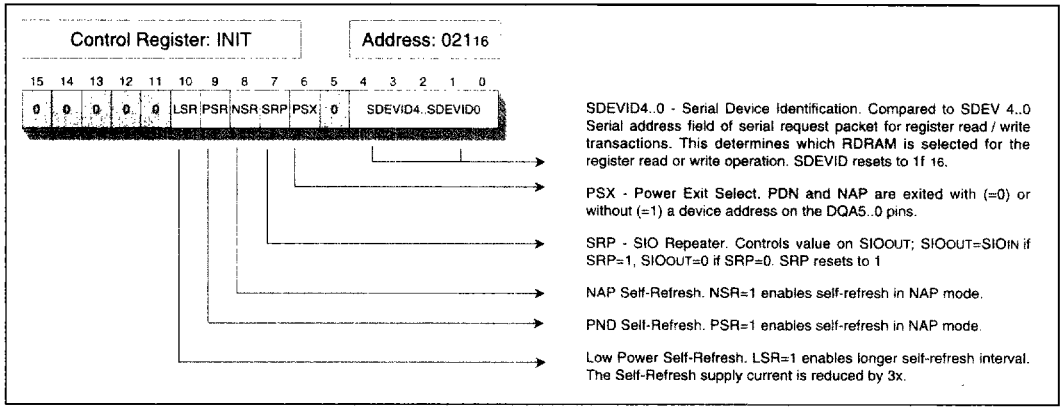
Field	Description
rsrv	Reserved. Should be driven as "0" by controller.
SOP3..SOP0	Serial opcode . Specifies command for control register transaction. Encoding not listed below are reserved.
	0000- SRD. Serial read of control register {SA11..SA0} of RDRAM {SDEV4..SDEV0}.
	0001 - SWR. Serial write of control register {SA11..SA0} of RDRAM {SDEV4..SDEV0}.
	0010 - SETR. Set Reset bit, all control registers assume their reset values.
	0011 - CLRR. Clear Reset bit, all control registers retain their reset values.
	0100 - SETF. Set fast (normal) clock mode.
SDEV4..SDEV0	Serial device. Compared to SDEVID4..SDEVID0 field of INIT control register field to select the RDRAM to which the transaction is directed.
SBC	Serial broadcast. When set, RDRAMs ignore {SDEV4..SDEV0} for RDRAM selection.
SA11..SA0	Serial address. Selects which control register of the selected RDRAM is read or written.
SA11..SA0	Serial data. The 16 bits of data written to or read from the selected control register of the selected RDRAM.

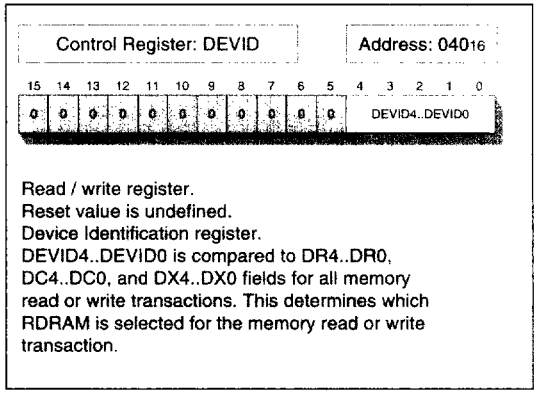
Control Register Summary

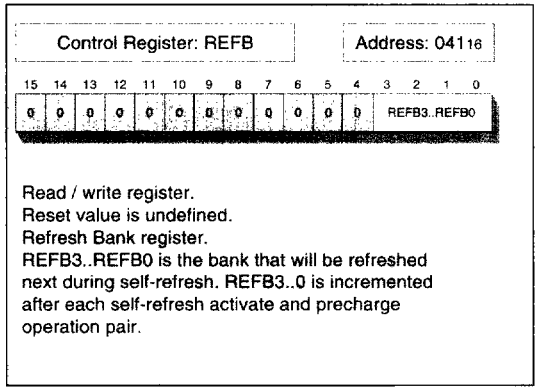
Table 14 summarizes the RDRAM control registers. Detail is provided for each control register in Figure 27 through Figure 31. Read-only bits which are shaded gray are Unused and return zero. Read-write bits which are shaded gray are reserved and should always be written with zero. The RIMM SPD Application Note (DL-0042) describes additional read-only configuration registers which are presented on Direct RIMMs.

Table 14: Control Register Summary

SA11..SA0 Address	Register Name	Field Name	read-write or read-only	Description
021$_{16}$	INIT	SDEVID	read-write, 5 bits	Serial device ID. Device address for control register read/write
		PSX	read-write, 1 bits	Power select exit. PDN/NAP exit with device addr on DQA5..0.
		NSR	read-write, 1 bits	NAP self-refresh. Enables self-refresh in NAP mode.
		PSR	read-write, 1 bits	PDN self-refresh. Enables self-refresh in PDN mode.
		LSR	read-write, 1 bits	Low power self-refresh. Enables low power self-refresh.
040$_{16}$	DEVID	DEVID	read-write, 5 bits	Device ID. Device address for memory read/write
041$_{16}$	REFB	REFB	read-write, 4 bits	Refresh bank. Next bank to be refreshed by self-refresh.
042$_{16}$	REFR	REFR	read-write, 9 bits	Refresh row. Next row to be refreshed by REFA, self-refresh.
043$_{16}$	rsrv			
044$_{16}$	rsrv			
045$_{16}$	NAPX	NAPXA	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A.
		NAPXB	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase B.
		DQS	read-write, 1 bits	DQ select. Selects CMD framing for NAP/PDN exit.
046$_{16}$	PDNXA	PDNXA	read-write, 1 3bits	PDN exit. Specifies length of PDN exit phase A.
047$_{16}$	PDNXB	PDNXB	read-write, 1 3bits	PDN exit. Specifies length of PDN exit phase B.
048$_{16}$	rsrv			
049$_{16}$	TFRM	TFRM	read-write, 4 bits	tFRM core parameter. Determines ROW to COL packet framing interval.
04a$_{16}$	rsrv			
04b$_{16}$	rsrv			
04c$_{16}$	rsrv			
04d$_{16}$	TEST77	TEST77	read-write, 16 bits	Test register. Write with zero.
04e$_{16}$	TEST78	TEST78	read-write, 16 bits	Test register. Write with zero.
096$_{16}$	CNFGA	REFBIT	read-only, 3 bits	Refresh bank bits. Used for multi-bank refresh.
		BBIT	read-only, 3 bits	Bank bits. Number of bank address bits.
		LSR	read-only, 1 bits	Low-power self-refresh. Device supports low-power self-refresh.
097$_{16}$	CNFGB	PVER	read-only, 4 bits	Protocol version. Specifies version of Direct protocol supported.
		BYT	read-only, 1 bits	Byte. Specifies an 8-bit or 9-bit byte size.
		DBL	read-only, 1 bits	Double. Specifies an 8-bit or 9-bit byte size.
		CBIT	read-only, 3 bits	Column bits. Number of column address bits.
		RBIT	read-only, 4 bits	Row bits. Number of row address bits.
098$_{16}$	MVER	MVER	read-write, 6 bits	Manufacturer version. Manufacturer identification number.
099$_{16}$	SVER	SVER	read-write, 16 bits	Stepping version. Mask version number.







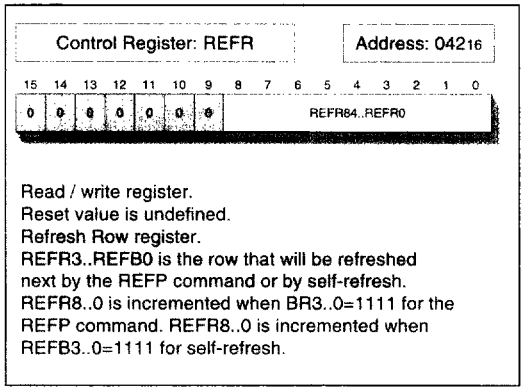


Figure 27: Control Registers

Control Register: rsrv | Address: 044₁₆

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Control Register: rsrv | Address: 044₁₆

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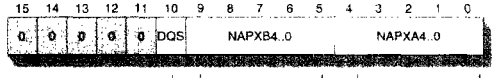
Control Register: NAPX | Address: 045₁₆



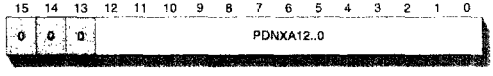
Read / write register.
Reset value is undefined.

NAPXA4..0 - Nap Exit Phase A. This field specifies the number of SCK cycles during the first phase for exiting NAP mode.

NAPXB4..0 - Nap Exit Phase B. This field specifies the number of SCK cycles during the second phase for exiting NAP mode.

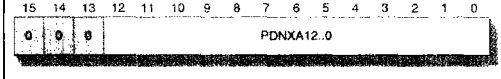
DQS - DQ Select. This field specifies the number of SCK cycles (0 => 0.5 cycles, 1 => 1.5 cycles) between the CMD pin framing sequence and the device selection on DQ5..0.

Control Register: PDNXA | Address: 046₁₆



Read / write register.
Reset value is undefined.
PDNXA4..0 - PDN exit Phase A. This field specifies the number of (64.SCK cycle) units during the first phase for exiting PDN mode.

Control Register: PDBXB | Address: 047₁₆



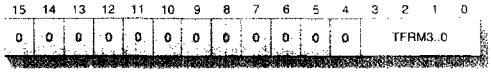
Read / write register.
Reset value is undefined.
PDNXB4..0 - PDN Exit Phase B. This field specifies the number of (256.SCK cycle) units during the second phase for exiting PDN mode.

Figure 28: Control Registers

Control Register: rsrv | Address: 048$_{16}$

(This figure intentionally left blank)

Control Register: TFRM | Address: 049$_{16}$



Read / write register.
Reset value is undefined.
TFRM3..0 - Specifies the value of the tFRM core parameter in tCYCLE units. This is the minimum offset between a ROW packet (which places a device at ATTN) and the first COL packet which must be framed. This should be written with the value i0111i (7.tCYCLE). This should match the tRCD.MIN datasheet parameter.

Control Register: rsrv | Address: 04a$_{16}$

(This figure intentionally left blank)

Control Register: rsrv | Address: 04b$_{16}$

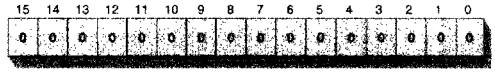
(This figure intentionally left blank)

Control Register: rsrv | Address: 04c$_{16}$

(This figure intentionally left blank)

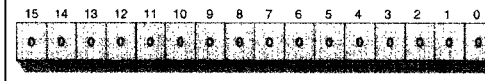
Figure 29: Control Registers

Control Register: TEST77 — Address: 04d16



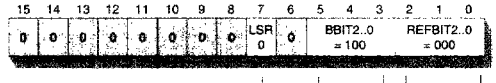
Read / write register.
Reset value is undefined.
This register is used for testing purpose. It should be written with zeros.

Control Register: TEST78 — Address: 04e16



Read / write register.
Reset value is undefined.
This register is used for testing purposes. It should be written with zeros.

Control Register: CNFGA — Address: 09616



Read only register.

REFBIT2..0 - Refresh Bank Bits. Specifies the number of high order bank address bits to be ignored during REFA and REFP commands. Permits multi-bank refresh in future RDRAMs.

BBIT2..0 - Bank Bits. Specifies the number of bank address bits used by this device.

LSR - Low Power self-Refresh. When set (=1), indicates that the device supports low-power self-refresh.

Control Register: CNFGB — Address: 09716

Read only register.

PVER3..0 - Protocol Version. Specifies the Direct Protocol version used by this device.

BYT - Byte width. B=1 means the device reads and writes 9-bit memory bytes. B=0 means 8 bits.

DBL - Doubled-Bank. DBL=1 means the device uses a doubled-bank architecture with adjacent bank dependency. DBL=0 means no dependency.

CBIT2..0 - Column Bits. Specifies the number of column address bits used by this device.

RBIT3..0 - Row Bits. Specifies the number of row bank address bits used by this device.

Figure 30: Control Registers

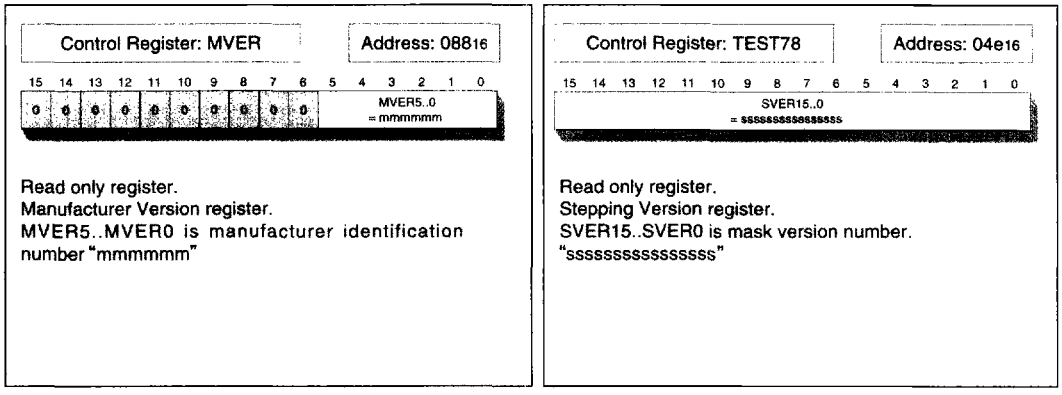


Figure 31: Control Registers

Power State Management

Table 15 summarizes the power states available to a Direct RDRAM. In general, the lowest power states have the longest operational latencies. For example, the relative power levels of PDN state and STBY state have a ratio of about 1:110, and the relative access latencies to get read data have a ratio of about 250:1.

PDN state is the lowest power state available. The information in the RDRAM core is maintained with self-refresh; an internal timer automatically refreshes all rows *of all banks. PDN has a relatively long exit latency (tPXB)* because the TCLK/RCLK block must resynchronize itself to the external clock signal.

NAP state is another low-power state in which either self-refresh or REFA-refresh are used to maintain the core. See "Refresh" on page 38 for a description of the two refresh mechanisms. NAP has a shorter exit latency (tNXB) than PDN because the TCLK/RCLK block maintains its synchronization state relative to the external clock signal. This imposes a limit (tNLIMIT) on how long an RDRAM may remain in NAP state before briefly returning to STBY or ATTN to update this synchro*nization state.*

Table 15: Power State Summary

Power State	Description	Blocks consuming power	Power State	Description	Blocks consuming power
PDN	Powerdown state.	Self-refresh	NAP	Nap state. Similar to PDN except lower wake-up latency.	Self-refresh or REFA-refresh TCLK/RCLK-Nap
STBY	Standby state. Ready for ROW packets.	REFA-refresh TCLK/RCLK ROW demux receiver	ATTN	Attention state. Ready for ROW and COL packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver
ATTNR	Attention read state. Ready for ROW and COL packets. Sending Q(read data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ mux transmitter Core power	ATTNW	Attention write state. Ready for ROW and COL packets. Ready for D (write data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ demux receiver Core power

The NAPRC command causes a napdown operation if the RDRAM's NCBIT is set. The NCBIT is not directly visible. It is undefined on reset. It is set by a NAP or NAPRC command to the RDRAM, and it is cleared by an ACT command to the RDRAM. It permits a controller to manage a set of RDRAMs in a mixture of power states.

Table 16 summarizes representative values for the IDD components used by the various power states. The components are totaled under "IDD - S ··· Profile" on Page 40.

Each component corresponds to a block in the RDRAM. In addition to the interface blocks (TCLK/RCLK, ROW demux, COL demux, D demux, and Q mux), the core is divided into two blocks: the sense amps, which can be performing either a RD or WR command, and the banks, which can be performing up to four (4 = tRC/tRR) simultaneous row access operations (ACT and PRER commands).

Table 16: Representative I_{DD} Components

I_{DD} Component	Block	Representative $I_{DD,MAX}$ value
I_{REF}	Self-refresh, INIT.LSR=1[a]	TBD
	Self-refresh, INIT.LSR=0	TBD
	REFA-refresh	TBD
I_{NAP}	TCLK/ RCLK-Nap	TBD
I_{FAST}	TCLK/ RCLK	TBD
I_{ROW}	ROW demux receiver	TBD
I_{COL}	COL demux receiver	TBD
I_D	DQ demux receiver	TBD
I_Q	DQ mux receiver	TBD[b]
$I_{RD/WR}$	Core - RD/ WR sense amp	TBD
I_{ACT}	Core - ACT bank	TBD[c]

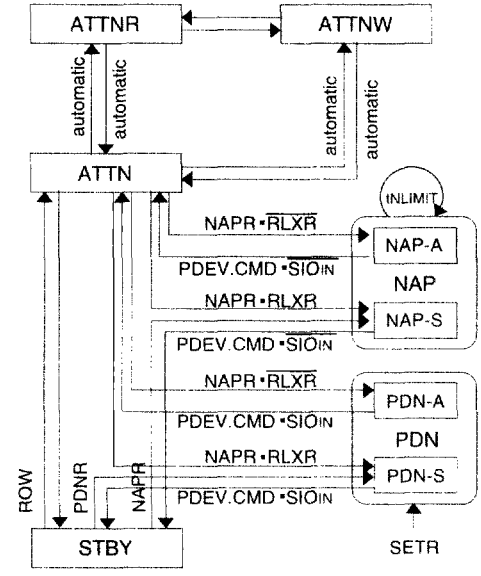
a. The LSR bit in the INIT control register sets self-refresh rate.
b. This does not include the IOL sink current. The RDRAM dissipate IOL*VOL in the output driver when a logic one is driven.
c. Up to four banks can be performing ACT/ PRER operations.

Figure 32 summarizes the transition conditions needed for moving between the various power states. Note that NAP and PDN have been divided into two substates (NAP-A/ NAP-S and PDN-A/ PDN-S) to account for the fact that a NAP or PDN exit may be made to either ATTN or STBY states.

At initialization, the SETR command in an SRQ packet will put the RDRAM into RDN-S state. The PDN exit sequence involves an optional PDEV specification and bits on the CMD and SIO_{IN} pins.

Once the RDRAM is in STBY, it will move to the ATTN/ ATTNR/ ATTNW states when it receives a non-broadcast ROW packet. The RDRAM returns to STBY from these three states when it receives a RLX command. Alternatively, it may enter NAP or PDN state from ATTN or STBY states with a NAPR or PDNR command in an ROWR packet. The PDN or NAP exit sequence involves an optional PDEV specification and bits on the CMD and SIO_{IN} pins. The RDRAM returns to the ATTN or STBY state it was originally in when it first entered NAP or PDN.

An RDRAM may only remain in NAP state for a time tNLIMIT. It must periodically return to ATTN or STBY.

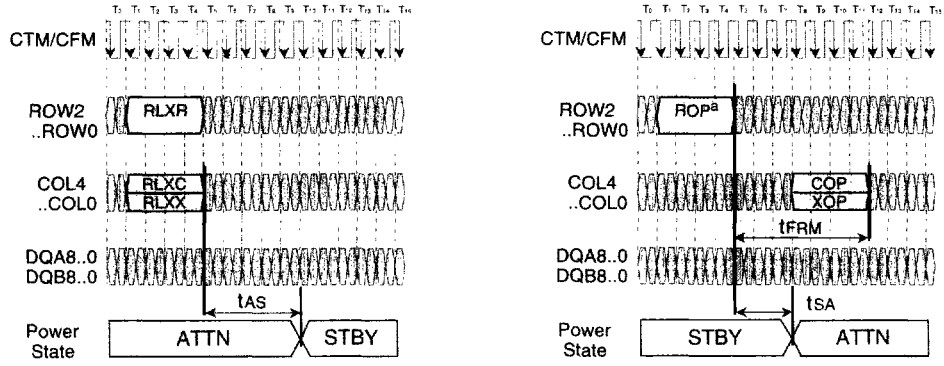


Notation:
SETR - SETR command in SRQ packet
PDNR - PDNR command in ROWR packet
NAPR - NAPR command in ROWR packet
RLXR - RLX command in ROWR packet
RLX - RLX command in ROWR,COLC,COLX packets
ROW - ROWA packet or ROWR packet (non-broadcast)
RDEV.CMD - (PDEV=DEVID)•(CMD=01)
SIO_{IN} - SIO_{IN} input value

Figure 32: Power State Transition Diagram

STBY state is the normal idle state of the RDRAM. In this state all banks and sense amps have usually been left precharged and ROWA and ROWR packets on the ROW pins are being monitored. When a non-broadcast ROW packet addressed to the RDRAM is seen, the RDRAM enters ATTN state (see the right side of Figure 33). This requires a time tSA during which the RDRAM activates the specified row of the specified bank. A time tFRM after the ROW packet, the RDRAM will be able to frame COL packets (this framing parameter is less than or equal to the tRCD,MIN of the RDRAM). Once in ATTN state, the RDRAM will automatically transition to the ATTNW and ATTNR states as it receives WR and RD commands.

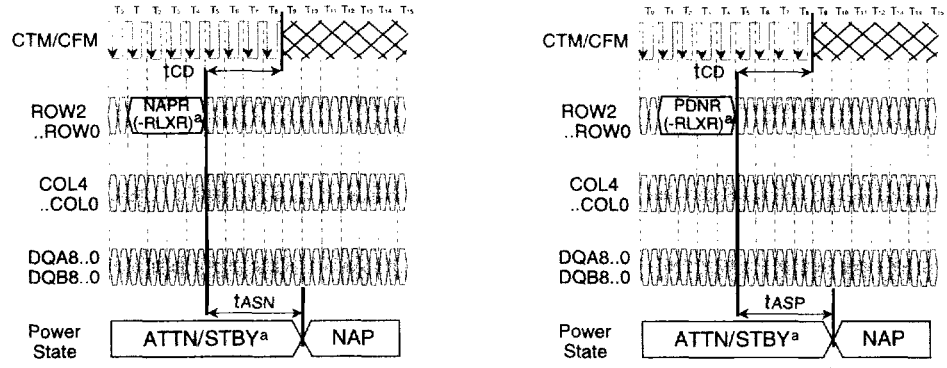
Once the RDRAM is in ATTN, ATTNW, or ATTNR states, it will remain there until it is explicitly returned to the STBY state with a RLX command. A RLX command may be given in an ROWR, COLC, or COLX packet (see the left side of Figure 33). It is usually given after all banks of the RDRAM have been precharged; if other bank are still activated, then the RLX command would not be given.



a Any non-broadcast ROWR or ROWA packet command will cause STBY exit.

Figure 33: STBY Entry (left) and STBY Exit (right)

Figure 34 shows the NAP entry sequence (left). NAP state is entered by sending a NAPR command in a ROW packet. A time tASN is required to enter NAP state (this specification is provided for power calculation purpose). The clock on CTM/ CFM must remain stable for a time tCD after the NAPR command.



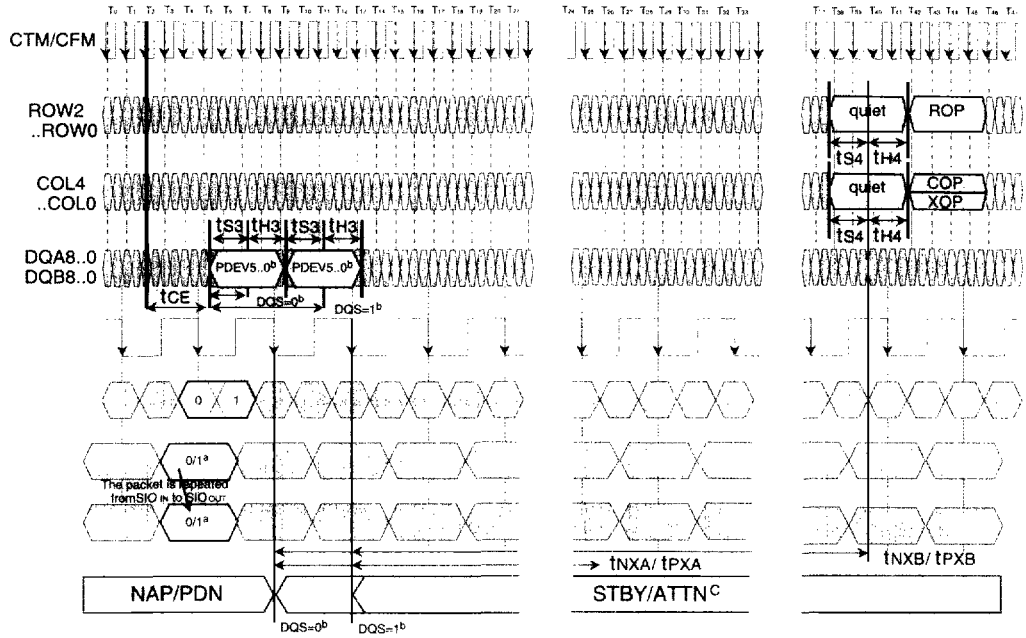
a If optional RLXR command is specified, used, the (eventual) NAP/PDN exit will be to STBY state. otherwise it will be to ATTN state

Figure 34: NAP Entry (left) and PDN Entry (right)

The RDRAM may be in ATTN or STBY state when the NAPR command is issued. When NAP state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with NAPR, then the RDRAM will return to STBY state when NAP is exited.

Figure 34 also shows the PDN entry sequence (right). PDN state is entered by sending a PDNR command in a ROW packet. A time tASP is required to enter PDN state (this specification is provided for power calculation purpose). The clock on CTM/CFM must remain stable for a time tCD after the PDNR command.

The RDRAM may be in ATTN or STBY state when the PDNR command is issued. When PDN state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with PDNR, then the RDRAM will return to STBY state when PDN is exited.



a Use 0 for NAP exit, 1 for PDN exit
b Device selection timing slot is selected by DQS field of NAPX register

c Exit to STBY or ATTN depends upon whether RLXR was asserted at NAP or PDN entry time

Figure 35: NAP and PDN Exit

Figure 35 also shows the NAP and PDN exit sequences. These sequences are virtually identical; the minor differences will be highlighted in the following description.

Before NAP or PDN exit, the CTM/CFM clock must be stable for a time tCE. Then, on a falling and rising edge of SCK, if there is a "01" on the CMD input, NAP or PDN state will be exited. Also, on the falling SCK edge the SIOCD input must be at a 0 for NAP exit and 1 for PDN exit.

If the PSX bit of the INIT register is 0, then a device PDEV5..0 is specified for NAP or PDN exit on the DQA5..0 pins. This value is driven on the rising SCK edge 0.5 or 1.5 SCK cycles after the original falling edge, depending upon the value of the DQS bit of the NAPX register.

The ROW and COL pins must be quiet at a time tNXB or tPXB after the indicated falling SCK edge. After that, ROW and COL packets may be directed to the RDRAM which is now in ATTN or STBY state.

Refresh

RDRAMs, like any other DRAM technology, use volatile storage cells which must be periodically refreshed. This is accomplished with the REFA command. Figure 36 shows an example of this.

The REFA command in the transaction is a broad-cast command (DR4T and DR4F are both set in the ROWR packet), so that in all devices bank number Ba is activated with row number REFR, where REFR is a control register. The controller increments the bank address Ba for the next REFA command. When Ba is equal to its maximum value, the RDRAM automatically increments REFR for the next REFA command.

On average, these REFA commands are sent once every $tREF/2^{BBIT+RBIT}$ (where BBIT and RBIT are control register) so that each row of each bank is refreshed once every tREF interval.

The REFA command is equivalent to an ACT command, in terms of the way that it interacts with other packets. In the example, an ACT command is sent after tRR to address b0, a different (non-adjacent) bank than the REFA command.

A second ACT command can be sent after a time tRC to address c0, the same bank (or an adjacent bank)a the REFA command.

Note that a broadcast REFP command is required a time tRAS after the initial REFA command in order to precharege the refreshed bank in all RDRAMs.

It is also possible to interleave refresh transactions (not shown). In the figure, the ACT b0 command would be replaced by a REFA b0 command. The b0 address would be broadcast to all devices, and would be {Broadcast, Ba+2, REFR}. Note that the bank address must skip by two to avoid adjacent bank interference. The bank incrementing pattern would be : {0,2, 4, 6, 1, 3, 5, 7, 8, 10, 12, 14, 9, 11, 13, 15}. When bank 15 is reached, the REFP command would automatically increment the REFR register.

A second refresh mechanism is available for use in PDN and NAP power states. This mechanism is called self-refresh mode. When the PDN power state is entered with the NPRF0 control register bit set, then self-refresh is automatically started for the RDRAM.

Self-refresh uses an internal time base reference in the RDRAM. This causes an activate and precharge to be carried out once in every $tREF/2^{BBIT+RBIT}$ interval. The REFB and REFR control registers are used to keep track of the bank and row being refreshed.

Before a controller places an RDRAM into self-refresh mode, it should perform REF refreshes until the bank address is equal to the maximum value. This ensures that no rows are skipped. Likewise, when a controller returns an RDRAM to REF refresh, it should start with the minimum bank address value (zero).

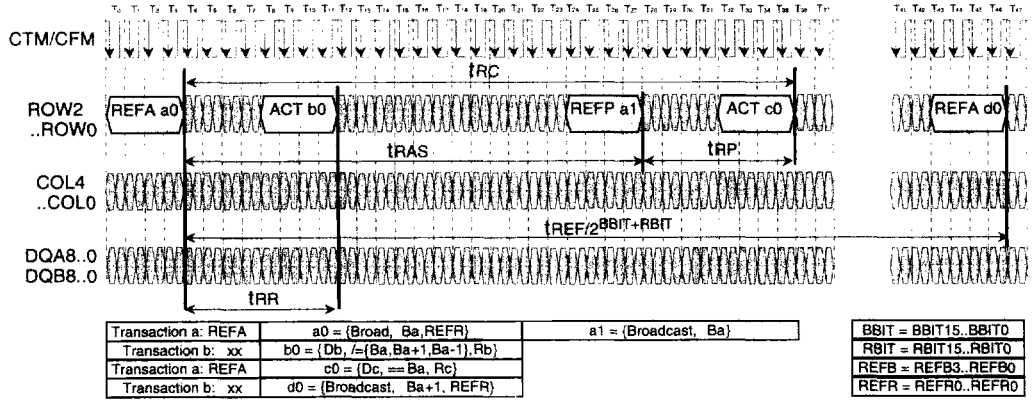


Figure 36: REFA/REFP Refresh Transaction Example

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL pin with respect to Gnd.	- 0.3	$V_{DD,MAX+0.3}$	V
$V_{I,CMOS,ABS}$	Voltage applied to any CMOS pin with respect to Gnd	- 0.3	$V_{DD+0.3}$	V
$V_{I,ABS}$	Voltage on VDD with respect to Gnd	- 0.3	$V_{DD,MAX+1.0}$	V
$T_{J,ABS}$	Junction temperature under bias	- 55	125	°C
T_{STORE}	Storage temperature.	- 55	125	°C

Thermal Parameters

Symbol	Parameter and conditions	Min	Max	Unit
T_J	*Junction operating temperature*	0	100	°C
θJC	Junction- to- Case thermal resistance		TBD	°C/Watt

I_{DD} - Supply Current Profile

Power State	RDRAM blocks consuming power	- 600 Max [a]	- 800 Max [a]	Unit
PDN	Self - refresh only (INIT.LSR=0/1)	TBD	TBD	mA
NAP	Refresh, T/ RCLK- Nap	TBD	TBD	mA
STBY	Refresh , T/ RCLK - Fast, ROW - demux	TBD	TBD	mA
ATTN	Refresh, T / RCLK - Fast Row - demux, COL - demux	TBD	TBD	mA
ATTNW	Refresh, T / RCLK - Fast Row - demux, COL - demux DQ-demux,1·WR- senseAmp, 4·ACT-Bank	TBD	TBD	mA
ATTNR	Refresh, T / RCLK - Fast Row - demux, COL - demux DQ-demux,1·RD- senseAmp, 4·ACT-Bank	TBD[b]	TBD[b]	mA

a. These I_{DD} numbers are manufacturer- dependent ; the numbers shown are representative maximum current levels at 1600MB/s

b. this does not include the I_{OL} sink current.The RDRAM dissipates $I_{OL} \cdot V_{OL}$ in each output driver when a logic one is driven.

Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}, V_{DDA}	Supply voltage	2.50 - 0.125	2.50+ 0.125	V
V_{TERM}	Termination Voltage	1.80 - 0.09	1.80 + 0.09	V
V_{REF}	Reference voltage	1.40 - 0.07	1.40 + 0.07	V
V_{IL}	RSL input low voltage	$V_{REF-0.5}$	$V_{REF-0.2}$	V
V_{IH}	RSL input high voltage.	$V_{REF+0.2}$	$V_{REF+0.5}$	V
$V_{IL,CMOS}$	CMOS input low voltage.	- 0.5	0.8	V
$V_{IH,CMOS}$	CMOS input high voltage.	1.8	$V_{DD+0.5}$	V

Electrical Characteristics

Symbol	Parameter and Conditions	Min	Max	Unit
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10	10	μA
I_{OH}	RSL output high current @(0°≤V_{OUT}°≤VDD)	-10	10	μA
$I_{O(auto)}$	RSL I_{OL} current @V_{OUT}=1.7V @Z_{OUT}= large [a]	0.0	4.0	mA
$I_{20(auto)}$	RSL I_{OL} current @V_{OUT}= 1.7V @ Z_{OUT}= 40Ω	18.0	22.0	mA
$I_{40(auto)}$	RSL I_{OL} current @V_{OUT} = 1.7V @Z_{OUT}= 20Ω	36	44	mA
ΔI_{OL}	RSL I_{OL} current resolution step	-	2.8	mA
r_{OUT}	Dynamics output impedance.	30	-	Ohm
$I_{I,CMOS}$	CMOS input leakage current @(0°≤$V_{I,CMOS}$°≤VDD)	-10.0	10.0	μA
$V_{OL,CMOS}$	CMOS output voltage @ $I_{OL,CMOS}$=1.0mA	0.0	0.4	V
$V_{OH,CMOS}$	CMOS output high voltage @$I_{OH,CMOS}$= -0.25mA	2.0	VDD	V

a. ZOUT is the load on the output used for CAL/SAM calibration ; output pin under test is unloaded.VTERM= 1.8 V and VREF=1.4V

Capacitance and Inductance

Symbol	Parameter and Conditions	Min	Max	Unit
C_I	RSL input parasitic capacitance	TBD	TBD	pF
L_I	RSL input parasitic inductance		TBD	nH
$C_{I,CMOS}$	CMOS input parasitic capacitance		TBD	pF

Timing Characteristics

Symbol	Parameter and Conditions	600 Min	600 Max	800 Min	800 Max	Unit
t_Q	CTM-to- DQA / DQB output time	-0.4	+0.4	-0.3	+0.3	ns
t_{QR},t_{QF}	DQA/DQB output rise and fall times	0.3	0.5	0.3	0.5	ns
t_{Q1}	SCK- to - SIO_{OUT} delay @ C_{LOAD} = 40pF	-	TBD	-	TBD	ns
t_{QR1},t_{QF1}	SIOOUT rise / fall @CLOAD =40pF	-	10	-	10	ns
t_{PROP1}	SIO IN-to- SIOOUT delay@ CLOAD= 40pF	-	4	-	4	ns
t_{NXB}	NDN exit delay - phase B	-	100	-	100	ns
t_{PXB}	PDN exit delay - phase B	-	10	-	10	μs
t_{AS}	ATTN - to - STBY power state delay	1	4	1	4	t_{CYCLE}
t_{SA}	STBY- to- ATTN power state delay	-	TBD	-	3	t_{CYCLE}
t_{ASN}	ATTN / STBY -to-NAP power state delay	-	TBD	-	TBD	t_{CYCLE}
t_{ASP}	ATTN / STBY -to-PDN power state delay	-	TBD	-	TBD	t_{CYCLE}

a. SIO_{OUT} refers to the SIO0 or SIO1 pin when used as an output.

Timing Characteristics

Symbol	Parameter and Conditions	600 Min	600 Max	800 Min	800 Max	Unit
t_{CR}, t_{CF}	CTM and CFM input and fall times	0.3	0.8	0.25	0.6	ns
t_{CYCLE}	CTM and CFM cycle times	3.33	4.0	2.50	3.33	ns
t_{CH}, t_{CL}	CTM and CFM high and low times	45%	55%	40%	60%	t_{CYCLE}
t_{TR}	CTM- CFM differential	0	3.0	0	3.0	t_{CYCLE}
t_{DR} t_{DF}	DQA/DQB/ROW/COL input rise / fall time	0.3	0.6	0.25	0.6	ns
t_s	DQA/DQB/ROW/COL-to-CFM setup time	0.35	-	0.2	-	ns
t_H	CFM-to-DQM/DQB/ROW/COL hold time	0.35	-	0.2	-	ns
t_{DR1}, t_{DF1}	SIO_{IN} [a], CMD ,SCK input rise and fall times	-	TBD	-	TBD	ns
t_{CYCLE1}	SCK cycle time-Serial control register transactions	1000	-	1000	-	ns
	SCK cycle time - power transitions	10	-	10	-	ns
t_{CH1}, t_{CL1}	SCK high and low times	40%	60%	40%	60%	t_{CYCLE1}
t_{S1}	CMD setup time	1	-	1	-	ns
t_{H1}	CMD hold time	1	-	1	-	ns
t_{S2}	SIO_{IN} setup time	5	-	5	-	ns
t_{H2}	SIO_{IN} hold time	5	-	5	-	ns
t_{S3}	PDEV setup time on DQA5..0	4.5	-	4.5	-	ns
t_{H3}	PDEV hold time on DQA5..0	1	-	1	-	ns
t_{S4}	ROW2..0, COL4..0 setup time for quiet window	-1	-	-1	-	t_{CYCLE}
t_{H4}	ROW2..0, COL4..0 hold time for quiet window	5	-	5	-	t_{CYCLE}
t_{CE}	CTM/CFM stable before NAP/PDN exit	2	-	2	-	t_{CYCLE}
t_{CD}	CTM/CFM stable after NAP/PDN exit	4	-	4	-	t_{CYCLE}
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	-	7	-	t_{CYCLE}
t_{NLIMIT}	Maximum time in NAP mode		10.0		10.0	•ïs
t_{REF}	Refresh interval		32		32	ms
t_{RAS}	RAS interval (time a row may stay activated)		64		64	•ïs
t_{PAUSE}	RDRAM substrate bias generator delay		200.0		200.0	•ïs

a. SIO_{IN} refers to the SIO0 or SIO1 pin when used as an input.

Timing Parameters

Parameter	Description	Min -40	Min -45	Min -50	Min -55[a]	Max	Units
t_{RC}	Row Cycle time of RDRAM banks- the interval between ROWA packets with ACT commands to the same bank. Figure 16 and Figure 17.	28	28	32	28	-	t_{CYCLE}
t_{RAS}	RAS-asserted time of RDRAM bank- the interval between ROWA packet with ACT command and next ROWR packet with PERE command to the same bank. See Figure 16 and Figure 17.	20	20	24	20	-	t_{CYCLE}
t_{RP}	Row Precharge time of RDRAM banks- the interval between ROWR packet with PRER command and next ROWA packet with ACT command to the same bank. See Figure 16 and Figure 17.	8	8	8	8	-	t_{CYCLE}
t_{PP}	Precharge-to-precharge time of RDRAM device- the interval between successive ROWR packets with PRER commands to different banks of the same device. See Figure 13.	8	8	8	8	-	t_{CYCLE}
t_{RR}	RAS-to-RAS time of RDRAM device- the interval between successive ROWA packets with ACT commands to different banks of the same device. See Figure 14.	8	8	8	8	-	t_{CYCLE}
t_{RCD}	RAS-to-CAS Delay- the interval from ROWA packet with ACT command to COLC packet with RD or WR command). See Figure 16 and Figure 17. Note- the RAS-to-CAS delay seen by the RDRAM core (tRCD,CORE) is equal to tRCD,CORE = 1 + tRCD because of differences in the row and column paths through the RDRAM interface.	7	9	11	7	-	t_{CYCLE}
t_{RAC}	RAS Access delay- effective interval from ROWA packet with ACT command to Q read data. This is equal to: tRAC = 1 + tRCD + tCAC.	16	18	20	16	-	t_{CYCLE}
t_{CAC}	CAS Access delay- the minimum interval from RD command to Q read data. See Figure 5.	8	8	8	8	8	t_{CYCLE}
t_{CWD}	CAS Write delay (interval from WR command to D write data. See Figure 5.	6	6	6	6	6	t_{CYCLE}
t_{CC}	CAS-to-CAS time of RDRAM bank- the interval between successive COLC commands). See Figure 16 and Figure 17.	4	4	4	4	-	t_{CYCLE}
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet. See Figure 4.	4	4	4	4	4	t_{CYCLE}
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to optional COLM packet with bytemask. See Figure 18.	8	8	8	8	-	t_{CYCLE}
t_{RCD}	Interval from last COLC packet with RD or automatic retire command to ROWR packet with PRER. See Figure 16 and Figure 17. Also, the interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLX packet with PREX command to the equivalent ROWR packet with PRER. See Figure 15	3	3	3	3	3	t_{CYCLE}

a. The tCYCLE,MIN is 3.3ns, not 2.5ns.

RSL Clocking and Bit Transport

Figure 38 shows the timing required to receive or transmit a pair of RSL bits. A single clock cycle T2 from the central figure is expanded to show the details associated with a falling edge and rising edge of the CFM and CTM clock inputs (the CTFN and CTMN inputs will always be at the Opposite signal level). Note that RSL signals are low-true; a high voltage logic zero.

Figure 38a shows the rise/ fall requirements of RSL input signals, and the rise/ fall characteristics of RSL output signals.

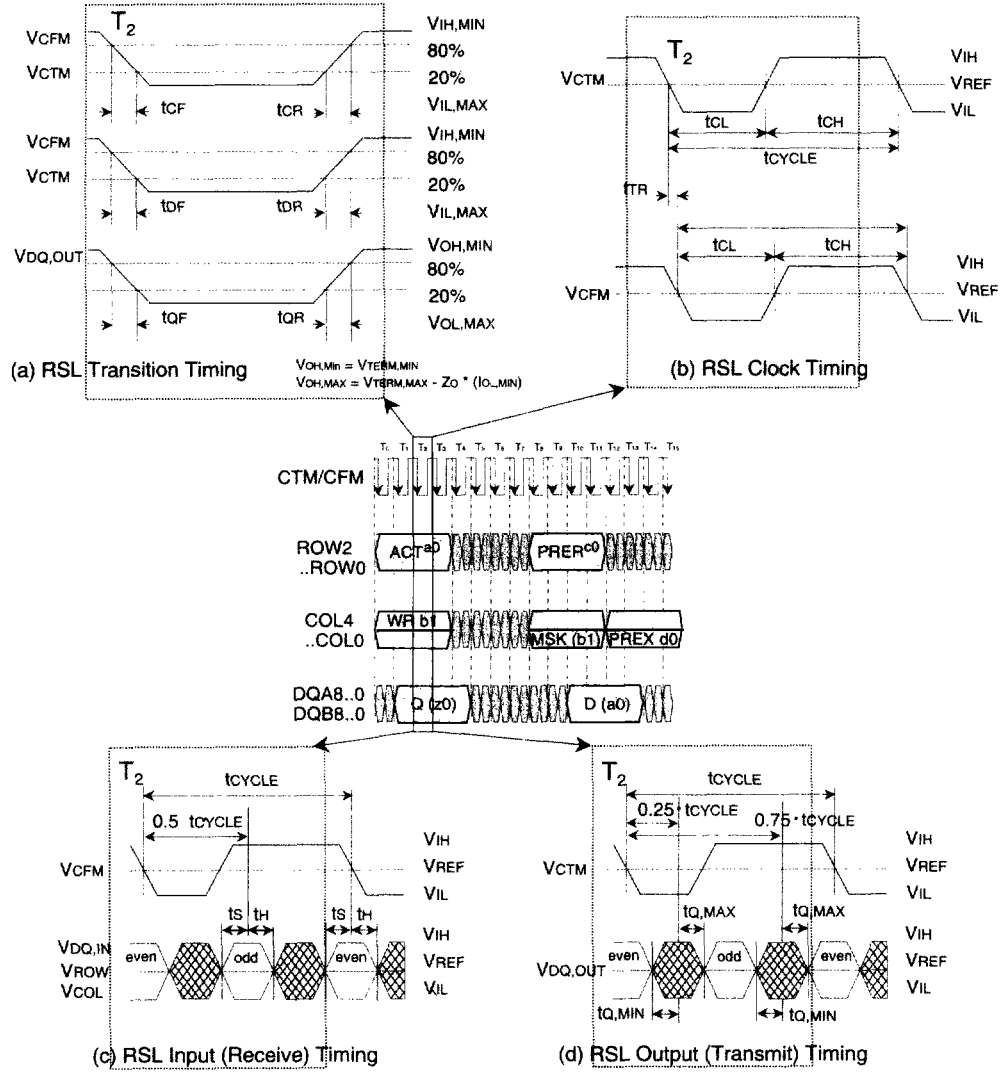


Figure 38: RSL Timing - Clocking and Bit Transport

Figure 38b show the duty cycle requirements of the RSL clock inputs. It also shows the tTR skew parameter (the amount of time by which CTM may lead CFM).

Figure 38c shows the setup and hold requirements of RSL inputs. Even bits are sampled on the falling edge of CFM and odd bits are sampled on the half-cycle (50%) point. The RDRAM synthesizes the 25%, 50%, and 75% timing points so that two bits may be received or transmitted per clock cycle per signal wire.

Figure 38d shows the valid window of RSL outputs. Even bits are driven from the 75% point and odd bits from the 25% point.

RSL Clocking and Bit Transport

Figure 39 shows the timing required to receive or transmit a CMOS bit. A single clock cycle is expanded to show the details associated with a falling edge of the SCK clock input. Note that all CMOS signals are low-true; a high voltage is logic zero.

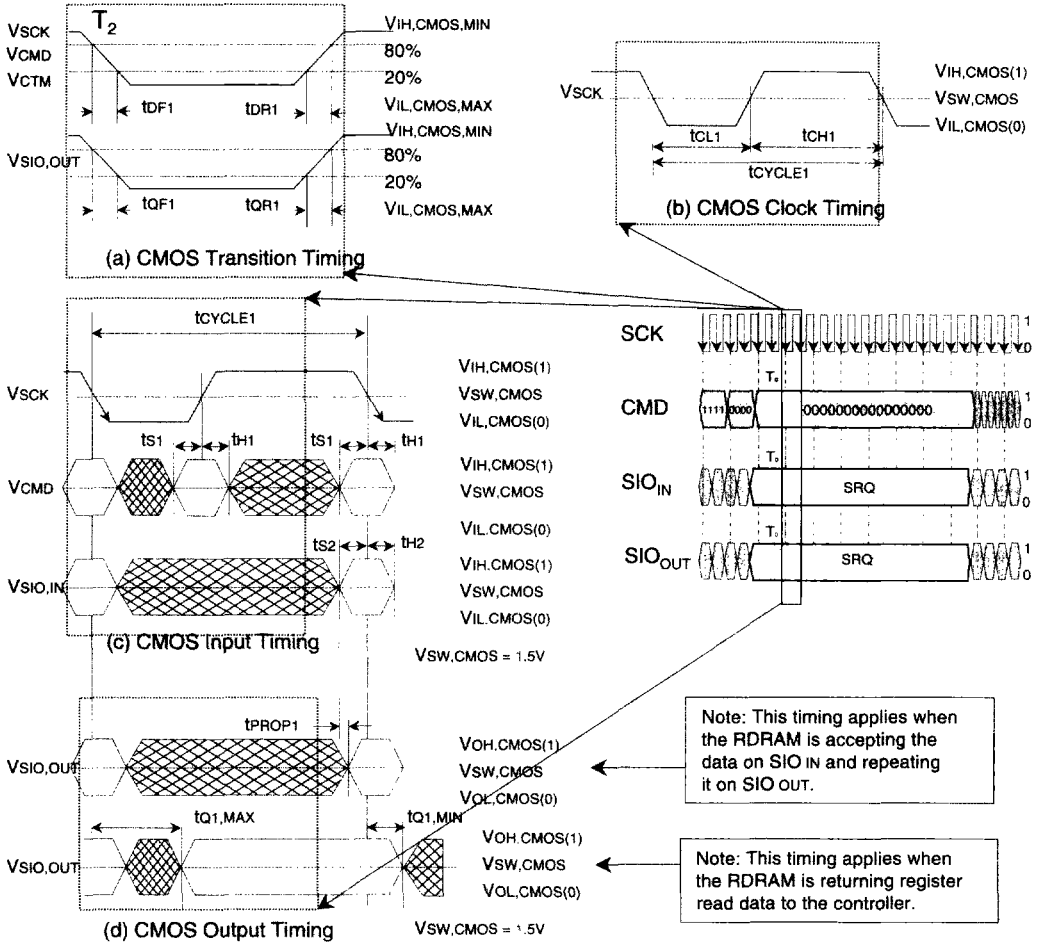


Figure 39: CMOS Timing - Clocking and Bit Transport

Glossary of Terms

ACT	Activate command from AV field.
activate	To access a row and place in sense amp.
adjacent	Two RDRAM banks which share sense amps (also called doubled banks).
ASYM	CCA register field for RSL VOL/VOH.
ATTN	Power state - ready for ROW/COL packets.
ATTNR	Power state - transmitting Q packets.
ATTNW	Power state - receiving D packets.
AV	Opcode field in ROW packets.
bank	A block of $2^{RBT}*2^{CBIT}$ storage cells in the core of the RDRAM.
BC	Bank address field in COLC packet.
BBIT	CNFGA register field - # bank address bits.
broadcast	An operation executed by all RDRAMs.
BR	Bank address field in ROW packets.
bubble	Idle cycle(s) on RDRAM pins needed because of a resource constraint.
BYT	CNFGB register field - 8/9 bits per byte.
BX	Bank address field in COLX packet.
C	Column address field in COLC packet.
CAL	Calibrate (IOL) command in XOP field.
CBIT	CNFGB register field - # column address bits.
CCA	Control register - current control A.
CCB	Control register - current control B.
CFM,CFMN	Clock pins for receiving packets.
Channel	ROW/COL/DQ pins and external wires.
CLRR	Clear reset command from SOP field.
CMD	CMOS pin for initialization/power control.
CNFGA	Control register with configuration fields.
CNFGB	Control register with configuration fields.
COL	Pins for column-access control.
COL	COLC,COLM,COLX packet on COL pins.
COLC	Column operation packet on COL pins.
COLM	Write mask packet on COL pins.
column	Rows in a bank or activated row in sense amps have 2^{CBIT} dualocts column storage.
command	A decoded bit-combination from a field.
COLX	Extended operation packet on COL pins.
controller	A logic-device which drives the ROW/COL /DQ wires for a Channel of RDRAMs.
COP	Column opcode field in COLC packet.
core	The banks and sense amps of an RDRAM.
CTM,CTMN	Clock pins for transmitting packets.
Current control	Periodic operations to update the proper IOL value of RSL output drivers.
D	Write data packet on DQ pins.
DBL	CNFGB register field - doubled-bank.
DC	Device address field in COLC packet.
device	An RDRAM on a Channel.
DEVID	Control register with device address that is matched against DR, DC, and DX fields.
DM	Device match for ROW packet decode.
Doubled-bank	RDRAM with shared sense amp.
DQ	DQA and DQB pins
DQA	Pins for data byte A.
DQB	Pins for data byte B.
DQS	NAPX register field - PDN/NAP exit.
DR,DR4T,DR4F	Device address field and packet framing fields in ROWA and ROWR packets.
dualoct	16 bytes - the smallest addressable datum.
DX	Device address field in COLX packet.
field	A collection of bits in a packet.
INIT	Control register with initialization fields.
initialization	configuring a Channel of RDRAMs so they are ready to respond to transactions.
LSR	CNFGA register field - low-power self-refresh.
M	Mask opcode field (COLM/COLX packet).
MA	Field in COLM packet for masking byte A.
MB	Field in COLM packet for masking byte B.
MSK	Mask command in M field.
MVER	Control register - manufacturer ID.
NAP	Power state - needs SCK/CMD wakeup.
NAPR	Nap command in ROP field.
NAPRC	Conditional nap command in ROP field.
NAPXA	NAPX register field -NAP exit delay A.
NAPXB	NAPX register field - NAP exit delay B.
NOCOP	No-operation command in COP field.
NOROP	No-operation command in ROP field.
NOXOP	No-operation command in XOP field.

NSR	INIT register field- NAP self- refresh.
Packet	A collection of bits carried on the Channel
PDN	Power state - needs SCK.CMD wakeup
PDNR	Power down command in ROP field
PDNXA	Control register - PDN exit delay A.
PDNXB	Control register - PDN exit delay B.
pin efficiency	The fraction of non-idle cycles on a pin
PRE	PREC,PER,PREX,precharge commands
PREC	Precharge command in COP field
precharge	Prepares sense amp and bank for activate.
PRER	Precharge command in ROP field
PREX	Precharge command in XOP field
PSX	INIT register field - PDN/NAP exit
PSR	INIT register - PDN self- refresh
PVER	CNFGB register field-protocol version
Q	Read data packet on DQ pins
R	Row address field of ROWA packet
RBIT	CNFGB register field -# row address bits
RD/RDA	Read(/prechage) command in COP field
read	Operation of accessing sense amp data
receive	Moving information form the Channel into the RDRAM (a serial stream is demuxed)
REFA	Refresh-activate command in ROP field
REFB	Control register - next bank (self-refresh)
REFBIT	CNFGA register field-ignore bank bits (for REFA and self-refresh)
REFP	Refresh -precharge command in ROP field
REFR	Control register- next row for REFA
refresh	Periodic operations to restore storage cells
retire	The automatic operation that stores write buffer into sense amp after WR command
RLX	RLXC,RLXR,RLXX relax commands
RLXC	Relax command in COP field
RLXR	Relax command in ROP field
RLXX	Relax command in XOP field
ROP	Row - opcode field in ROWR packet
row	2^{CBIT} dualocts of cells (bank/sense amp)
ROW	Pins for row access control
ROW	ROWA or ROWR packets on ROW pins
ROWA	Activate packet on ROW pins
ROWR	Row operation packet on ROW pins
RQ	Alternate name for ROW /COL pins
RSL	Rambus Signaling Levels
SAM	Sample (IOL) command in XOP field
SA	Serial address packet for control register transactions w / SA address field
SBC	Serial broadcast field in SRQ
SCK	CMOS clock pin
SD	Serial data packet for control register transactions w / SD data field
SDEV	Serial device address in SQR packet
SDEVID	INIT register field - Serial device ID
self-refresh	Refresh mode for PDN and NAP
sense amp	Fast storage that holds copy of bankís row
SETF	Set fast clock command from SOP field
SETR	Set reset command from SOP field
SINT	Serial interval packet for control register read / write TRANSACTIONS
SIO0,SIO1	CMOS serial pins for control registers
SOP	Serial opcode field in SRQ
SRD	Serial read opcode command from SOP
SRP	INIT register field-Serial repeat bit
SRQ	Serial request packet for control register read / write transactions
STBY	Power state - ready for ROW packets
SVER	control register - stepping version
SWR	serial write opcode command from SOP
TCAS	TCALCAS register field - t_{CAS} core delay
TCAL	TCLSCAS register field -t_{CLS} core delay
TCLSCAS	Control register - t_{CAS} and t_{CLS} delay
TCYCLE	Control register - t_{CYCLE} delay
TDAC	Control register - t_{DAC} delay
TEST 77	Control register - for test purpose
TEST 78	Control register - for test purpose
TRDLY	Control register - t_{RDLY} delay
transaction	ROW ,COL,DQ packets for memory access
transmit	Moving information from RDRAM onto the Channel(parallel word is muxed)
WR/WRA	Write (/precharge)command in COP field
write	Operation of modifying sense amp data
XOP	Extended opcode field in COLX packet