SPM2864C25/30

NMOS 64K-BIT ELECTRICALLY ERASABLE PROM

- **Access Time 250ns/300ns**
- **8,192 Words×8 Bits**
- **Single 5V Supply**

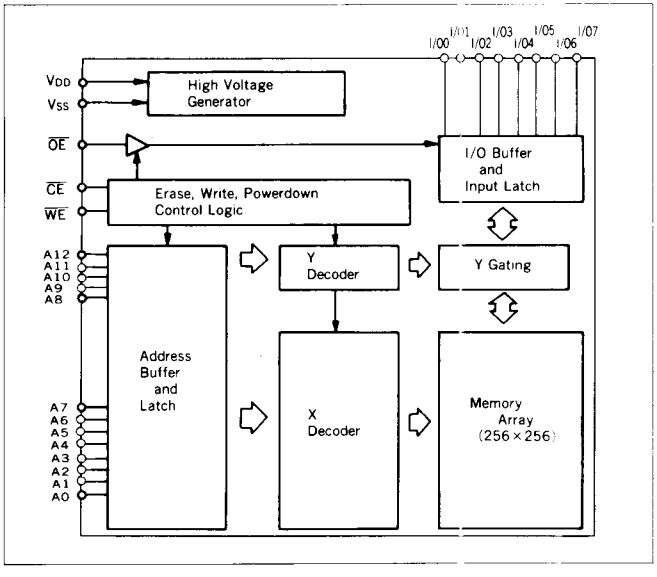
■DESCRIPTION

The SPM2864C25/30 is an 8,192 words × 8bits electrically erasable programmable read-only memory (E^2PROM). The SPM2864C25/30 can be easily erased and reprogrammed on a byte basis with a TTL-low level signal on $\overline{WE}$. The SPM2864C25/30 operates from a single 5V supply. External programming voltage and write pulse shaping are not required because they are generated by on-chip circuitry.

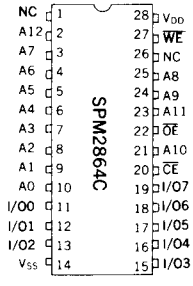
■FEATURES

- Fast access time ····· SPM2864C25 250ns (Max)
  SPM2864C30 300ns (Max)
- Low supply current ····· Standby : 40mA (Max)
  Operation : 100mA (Max)
- Single power supply ····· 5V ± 10%
- Address, Data, $\overline{CE}$, $\overline{OE}$ Latches
- Byte erase / Byte write time ····· 10ms (Typ)
- Chip erase time ····· 20ms (Typ)
- Conforms to JEDEC byte-wide standard
- Reliable N-channel NMOS technology
- 10,000 erase/write cycles
- Package ····· 28-pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A12	Address Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 to I/O7	Data I/O
V_{DD}	Power Supply (5V)
V_{SS}	Power Supply (0V)
NC	No connection

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{DD}	−0.6 to 7.0	V
Input voltage*	V_I	−0.6 to 7.0	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C

* With respect to V_{SS}

■RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		—	0	—	V
Input voltage	V_{IH}		2.0	—	V_{DD}+1	V
	V_{IL}		−0.1	—	0.8	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.0	—	V_{DD}+1	V
Low level input voltage	V_{IL}		−0.1	—	0.8	V
Input leakage current	I_{LI}	V_{DD}=5.5V, V_I=5.5V	—	—	10	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{IH}$	—	—	40	mA
Operating supply current	I_{DDO}	$\overline{CE}=V_{IL}$	—	—	100	mA
Output leakage current	I_{LO}	V_{DD}=5.5V, V_O=5.5V/0.4V	—	—	10	μA
High level output voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V

●Terminal Capacitance

(f=1.0MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	—	6	pF
Output capacitance	C_O	V_O=0V	—	—	12	pF

Read Mode

●AC Electrical Characteristics

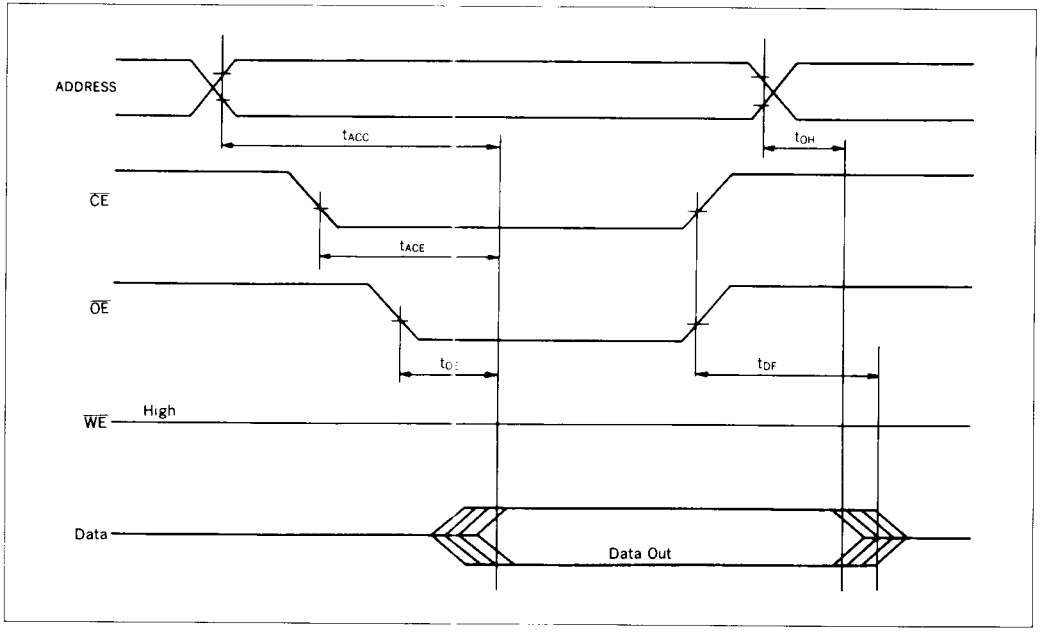
(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol		Conditions	SPM2864C$_{25}$		SPM2864C$_{30}$		Unit
				Min	Max	Min	Max	
Address access time	t_{ACC}	*1	$\overline{WE} = V_{IH}$	—	250	—	300	ns
Chip enable access time	t_{ACE}		$\overline{WE} = V_{IH}$	—	250	—	300	ns
Output enable access time	t_{OE}		$\overline{WE} = V_{IH}$	—	100	—	150	ns
Output floating	t_{DF} *2		$\overline{WE} = V_{IH}$	0	90	0	130	ns
Output hold time	t_{OH}		$\overline{WE} = V_{IH}$	0	—	0	—	ns

*1 Input pulse levels 0.4V to 2.4V, Input rise and fall times ≦ 20 ns, Output load 1 TTL + 100pF
Reference level for measuring timing 0.8V and 2.0V

*2 t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●Timing Chart

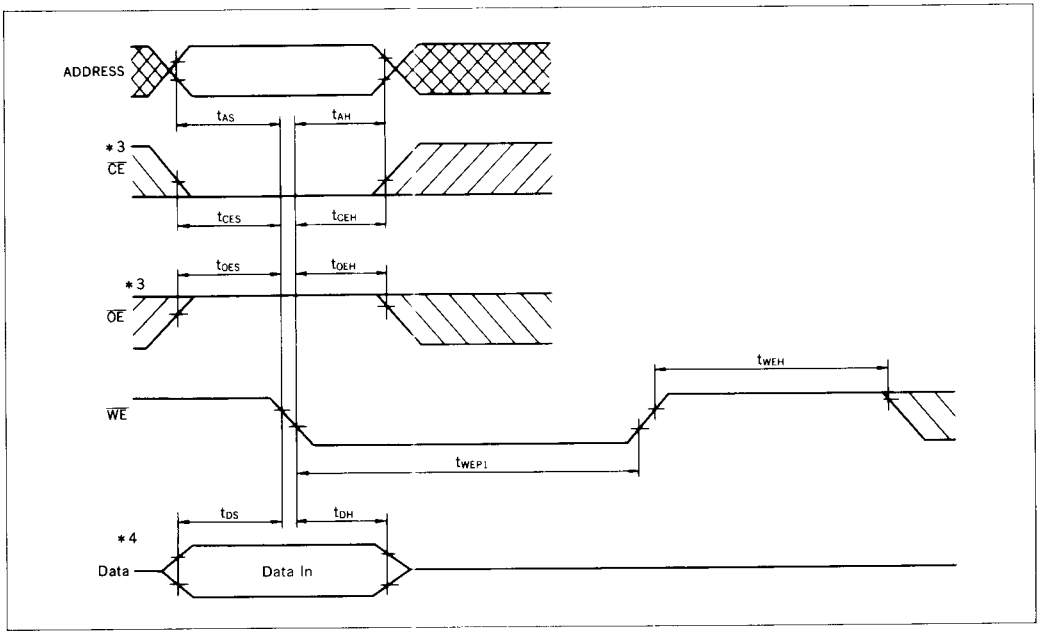


Byte Erase and Byte Write Mode

●AC Electrical Characteristics (V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address setup time	t_{AS}	Input pulse levels: 0.4V to 2.4V Input rise and fall times: ≦20ns Output load: 1 TTL + 100pF Reference level for measuring timing: 0.8V and 2.0V	0	—	—	ns
Chip enable setup time	t_{CES}		0	—	—	ns
Output enable setup time	t_{OES}		0	—	—	ns
Data setup time	t_{DS}		0	—	—	ns
Address hold time	t_{AH}		100	—	—	ns
Data hold time	t_{DH}		100	—	—	ns
Chip enable hold time	t_{CEH}		100	—	—	ns
Output enable hold time	t_{OEH}		100	—	—	ns
$\overline{WE}$ pulse width	t_{WEP1}		8	—	15	ms
$\overline{WE}$ high time	t_{WEH}		1,000	—	—	ns

●Timing Chart



*3 $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Write/Erase operation.
*4 I/O0 to I/O7 must be "1" in Byte Erase.

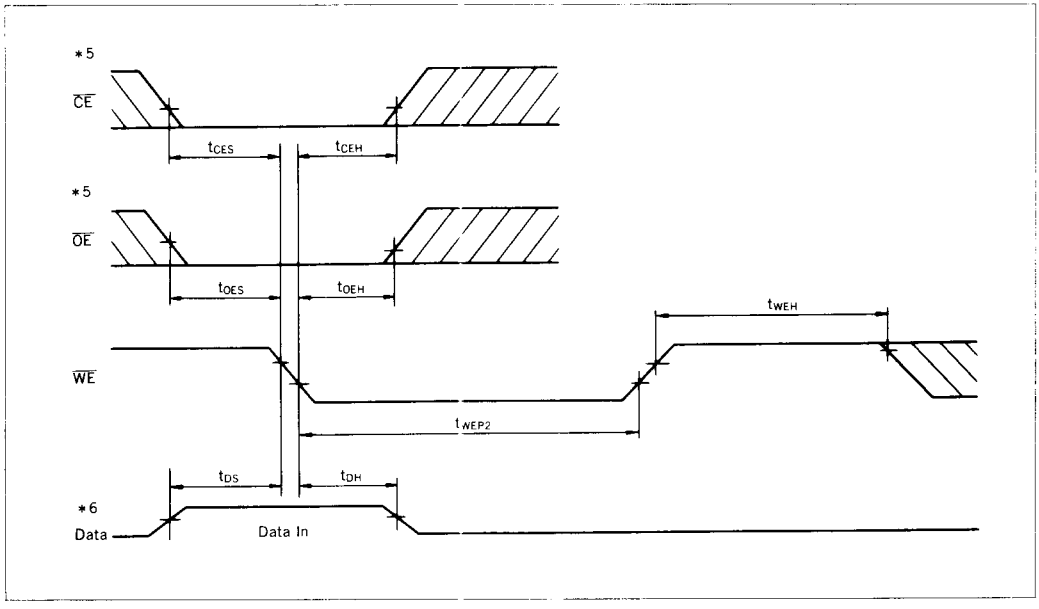
Chip Erase Mode I

●AC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Chip enable setup time	t_{CES}	Input pulse levels: 0.4V to 2.4V Input rise and fall times: ≦20ns Output load: 1 TTL + 100pF Reference level for measuring timing: 0.8V and 2.0V	0	—	—	ns
Output enable setup time	t_{OES}		0	—	50	ns
Data setup time	t_{DS}		0	—	—	ns
Data hold time	t_{DH}		100	—	—	ns
Chip enable hold time	t_{CEH}		100	—	—	ns
Output enable hold time	t_{OEH}		100	—	—	ns
$\overline{WE}$ pulse width	t_{WEP2}		15	—	25	ms
$\overline{WE}$ high time	t_{WEH}		1,000	—	—	ns

●Timing Chart



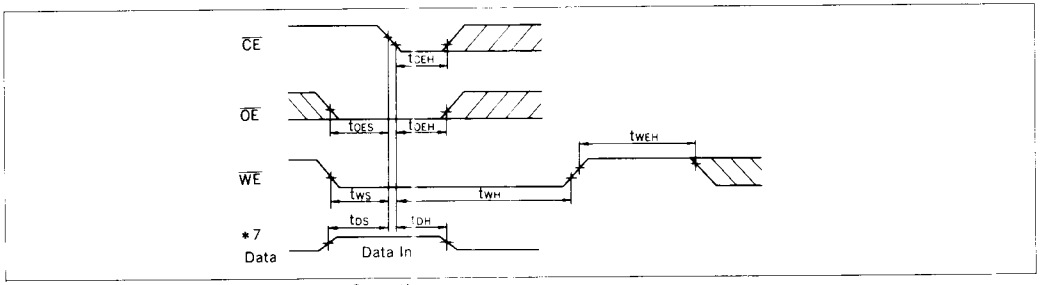
*5 $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Chip Erase operation.
*6 I/O0 to I/O7 must be "1" in Chip Erase operation.
"H" or "L" about Address.

Chip Erase Mode II

●AC Electrical Characteristics ($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output enable setup time	t_{OES}	Input pulse levels:0.4V to 2.4V Input rise and fall times:≦20ns Output load: 1 TTL + 100pF Reference level for measuring timing:0.8V and 2.0V	0	—	—	ns
$\overline{WE}$ setup time	t_{WS}		0	—	—	ns
Data setup time	t_{DS}		0	—	—	ns
Data hold time	t_{DH}		100	—	—	ns
Chip enable hold time	t_{CEH}		100	—	—	ns
Output enable hold time	t_{OEH}		100	—	—	ns
$\overline{WE}$ pulse width	t_{WH}		15	20	25	ms
$\overline{WE}$ high time	t_{WEH}		1,000	—	—	ns

●Timing Chart



*7 I/O1to7 must be "1" in Chip Erase Operation.
"H" or "L" about Address.

■FUNCTIONS

●Truth Table

Mode \ Pin name	Data I/O I/O0 to I/O7	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$
Read	Output data	L	L	H
Standby	Hi-Z	H	X	X
Byte Erase	D_{IN}=H	L	H	L
Byte Write	Input data	L	H	L
Chip Erase	D_{IN}=H	L	L	L
Deselect	Hi-Z	L	H	H

X :"H" or "L"

■PACKAGE DIMENSIONS