

EMIPAK 1B PressFit Power Module

650 V HF Output Rectification, Flexible Configuration, 20 A



EMIPAK 1B
(package example)

FEATURES

- FRED Pt[®] diode technology
- Exposed Al₂O₃ substrate with low thermal resistance
- Ultra soft reverse recovery
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRIMARY CHARACTERISTICS	
D1 - D12	
V _{RRM}	650 V
V _{FM} typical at 20 A	1.70 V
I _O at T _{SINK} = 99 °C	20 A
t _{rr} typical at 20 A	65 ns
Package	EMIPAK 1B
Circuit configuration	6 x independent ultrafast rectifiers legs for output rectification
Type	Modules - diode, FRED Pt [®]

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T _J		175	°C
Storage temperature range	T _{Stg}		-40 to +150	
RMS isolation voltage	V _{ISOL}	T _J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
D1 - D12				
Maximum average forward current (per diode)	I _{F(AV)}	T _{SINK} = 25 °C	31	A
		T _{SINK} = 80 °C	23	
Power dissipation	P _D	T _{SINK} = 25 °C	68	W
		T _{SINK} = 80 °C	43	
Maximum peak one cycle forward non-repetitive surge current	I _{FSM}	10 ms sine or 6 ms rectangular pulse, T _J = 25 °C, no voltage reapplied	160	A
		8.3 ms sine, T _J = 25 °C, no voltage reapplied	167	A
Maximum I ² t capability for fusing	I ² t	No voltage reapplied, t = 10 ms	128	A ² s
		No voltage reapplied, t = 8.3 ms	117	
Maximum I ² √t capability for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied	1281	A ² √s
Repetitive peak reverse voltage	V _{RRM}		650	V
Low level value of threshold voltage	V _{F(TO)1}	(16.7 % × I _{F(AV)}) < I < × I _{F(AV)} , T _J = T _J maximum	1.03	V
High level value of threshold voltage	V _{F(TO)2}	(I > × I _{F(AV)}), T _J = T _J maximum	1.37	
Low level value of forward slope resistance	r _{f1}	(16.7 % × I _{F(AV)}) < I < × I _{F(AV)} , T _J = T _J maximum	39.6	mΩ
High level value of forward slope resistance	r _{f2}	(I > × I _{F(AV)}), T _J = T _J maximum	38.3	

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.



ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
D1 - D12						
Forward voltage drop	V _{FM}	I _F = 20 A	-	1.70	2.10	V
		I _F = 20 A, T _J = 175 °C	-	1.33	-	
Breakdown voltage	V _{BR}	I _R = 100 μA	650	-	-	V
Reverse leakage current	I _{RM}	V _R = 650 V	-	0.3	10	μA
		V _R = 650 V, T _J = 175 °C	-	90	-	

SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
D1 - D12						
Diode reverse recovery time	t _{rr}	V _R = 400 V, I _F = 20 A, di/dt = 500 A/μs	-	65	-	ns
Diode reverse recovery current	I _{rr}		-	8.5	-	A
Diode reverse recovery charge	Q _{rr}		-	275	-	nC
Diode reverse recovery time	t _{rr}	V _R = 400 V, I _F = 20 A, di/dt = 500 A/μs, T _J = 125 °C	-	111	-	ns
Diode reverse recovery current	I _{rr}		-	14.8	-	A
Diode reverse recovery charge	Q _{rr}		-	821	-	nC

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R ₂₅	T _C = 25 °C	5000	Ω
	R ₁₀₀	T _C = 100 °C	493 ± 5 %	
B-value	B _{25/50}	R ₂ = R ₂₅ exp. [B _{25/50} (1/T ₂ - 1/(298.15K))]	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
D1 - D12 - thermal resistance junction to sink (per diode) ⁽¹⁾	R _{thJS}	-	1.83	-	°C/W
Case to sink thermal resistance (per module) ⁽¹⁾		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

⁽¹⁾ Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

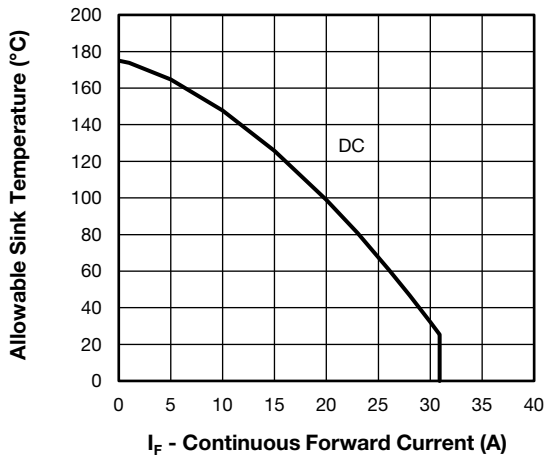


Fig. 1 - Allowable Sink Temperature vs. Continuous Forward Current (Forward Current vs. Sink Temperature)

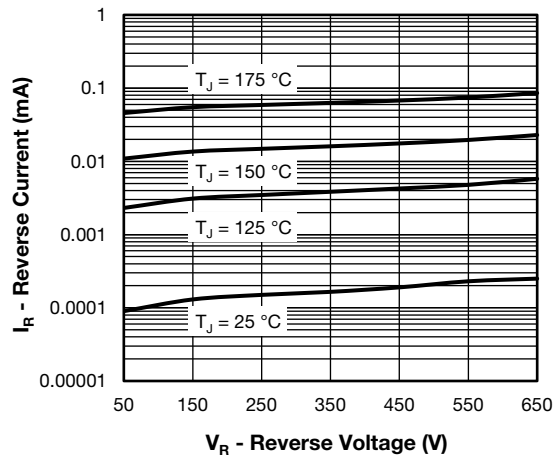


Fig. 4 - Typical Reverse Current vs. Reverse Voltage (Per Diode)

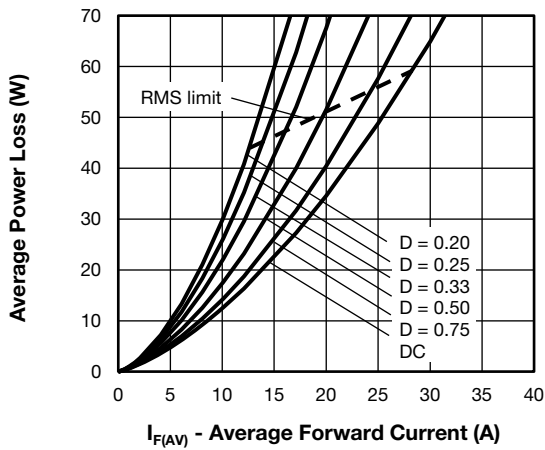


Fig. 2 - Average Power Loss vs. Average Forward Current (Forward Power Loss Characteristics)

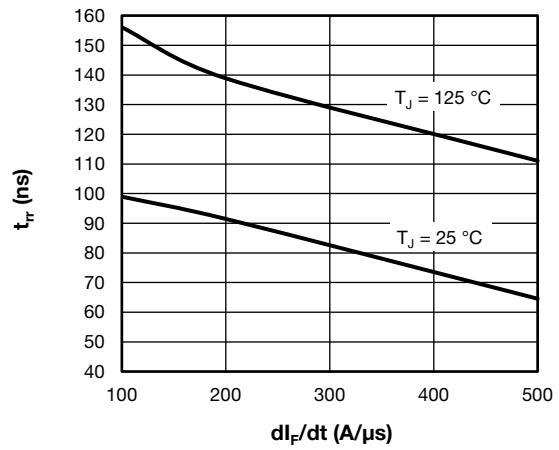


Fig. 5 - Typical Reverse Recovery Time vs. di_F/dt (Per Diode)
 $V_{rr} = 400\text{ V}$, $I_F = 20\text{ A}$

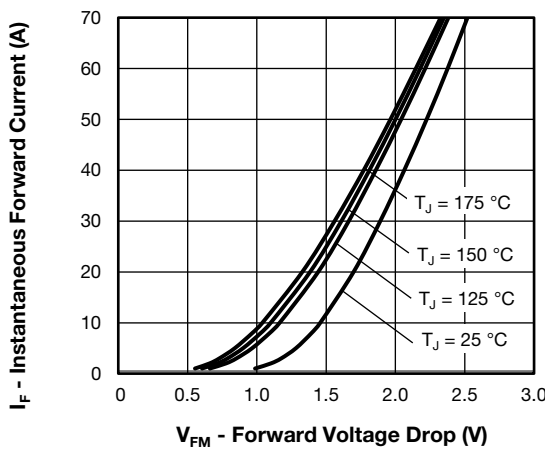


Fig. 3 - Typical Forward Voltage Drop vs. Instantaneous Forward Current (Per Diode)

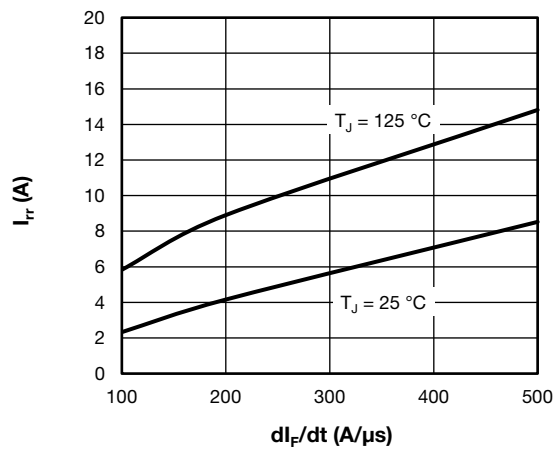


Fig. 6 - Typical Reverse Recovery Current vs. di_F/dt (Per Diode)
 $V_{rr} = 400\text{ V}$, $I_F = 20\text{ A}$

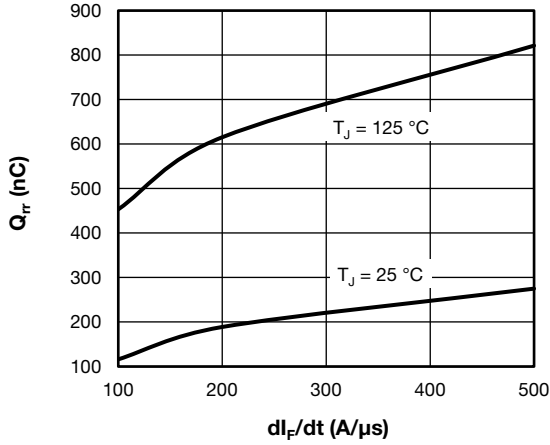


Fig. 7 - Typical Reverse Recovery Charge vs. di_F/dt (Per Diode)
 $V_{rr} = 400\text{ V}$, $I_F = 20\text{ A}$

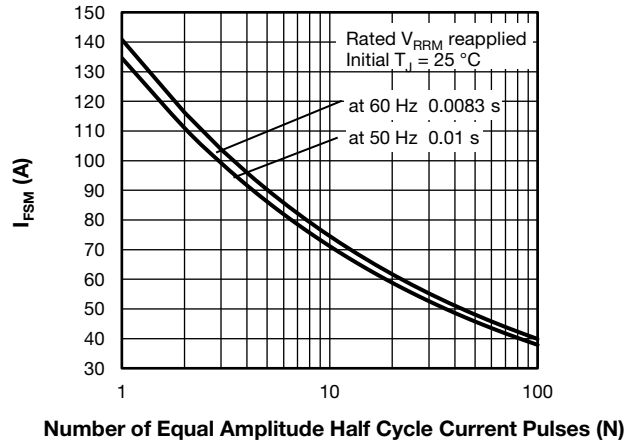


Fig. 8 - I_{FSM} vs. N
(Non-Repetitive Peak Forward Surge Current vs. Number Pulses)

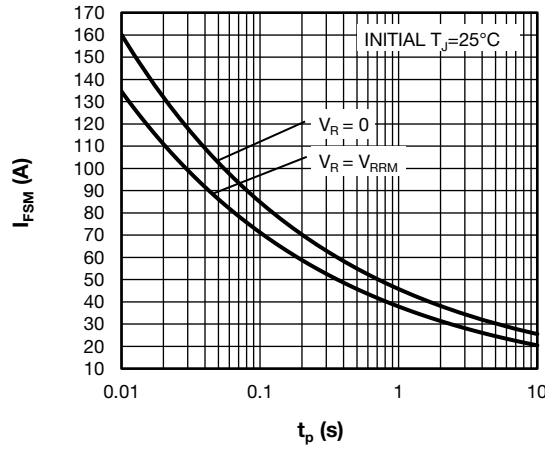


Fig. 9 - I_{FSM} vs. t_p
(Non-Repetitive Peak Forward Surge Current vs. Pulse Duration)

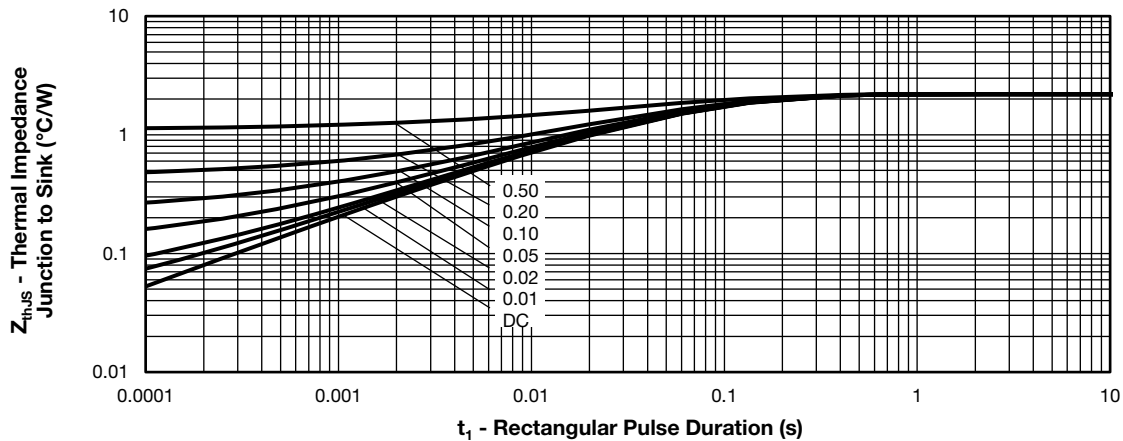
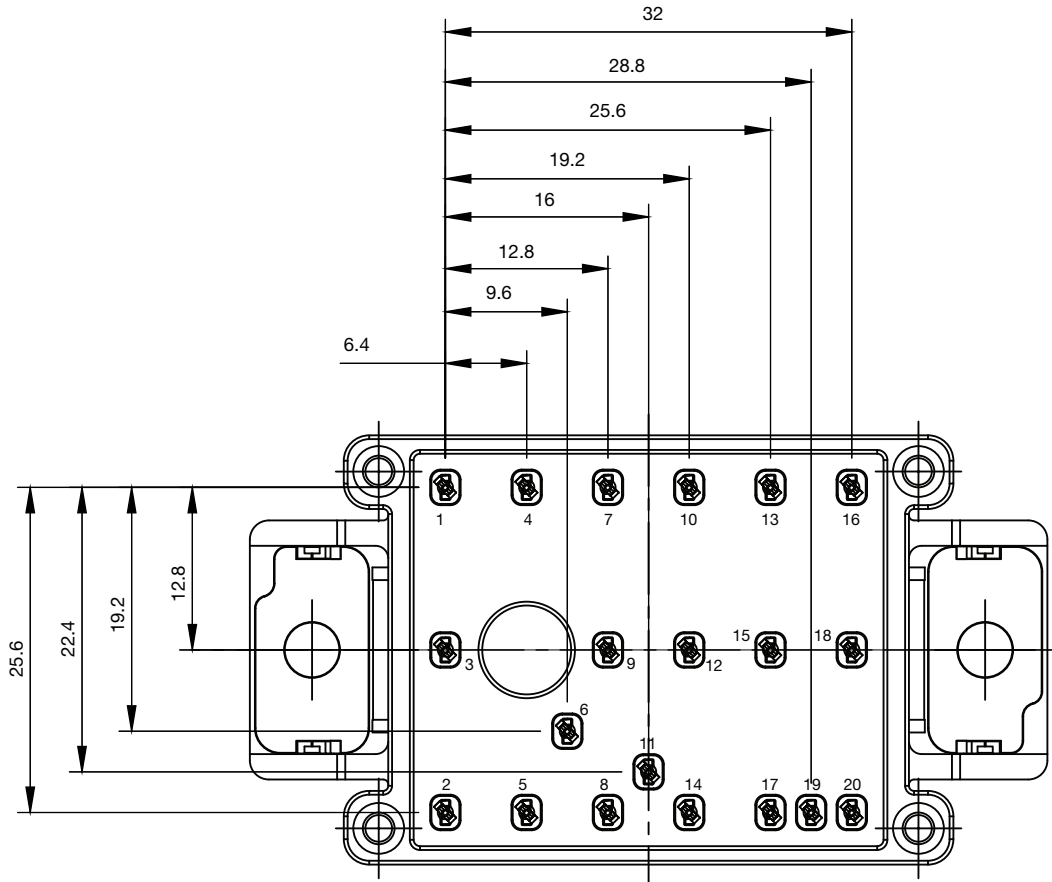


Fig. 10 - Z_{thJS} Thermal Impedance Junction to Sink vs. t_1 Rectangular Pulse Duration
(Maximum Thermal Impedance Z_{thJS} Characteristics Per Diode)

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
6 x independent ultrafast rectifiers legs for output rectification	V	

PACKAGE





ORDERING INFORMATION TABLE

Device code	VS-	EN	V	020	F	65	U
	①	②	③	④	⑤	⑥	⑦

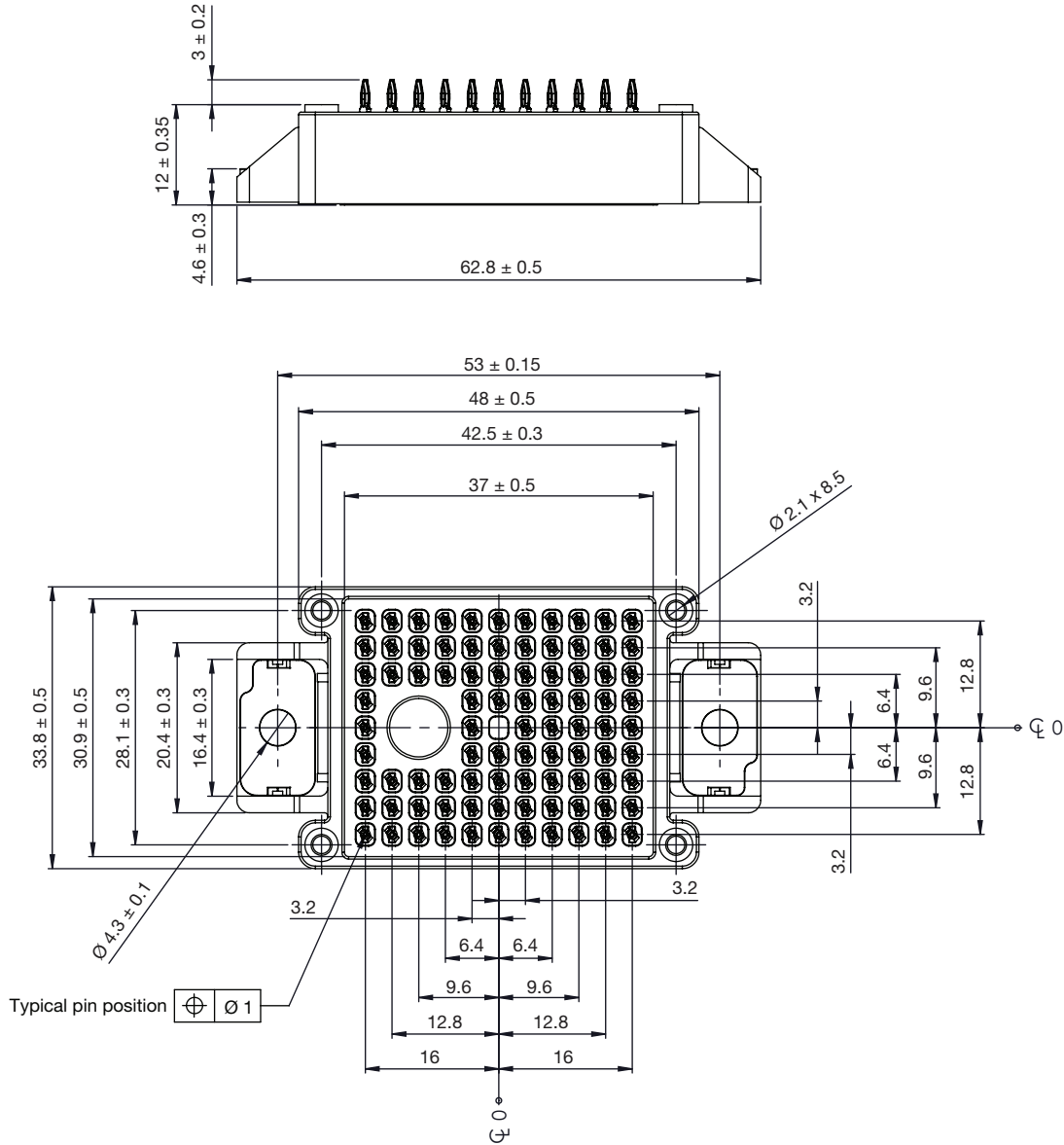
- 1** - Vishay Semiconductors product
- 2** - Package indicator (EN = EMIPAK 1B)
- 3** - Circuit configuration (V = 6 x independent ultrafast rectifiers legs for output rectification)
- 4** - Current rating (020 = 20 A)
- 5** - Switch die technology (F = FRED Pt[®] diode)
- 6** - Voltage rating (65 = 650 V)
- 7** - Diode die technology (U = FRED Pt diode with ultra soft reverse recovery)

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580



EMIPAK-1B PressFit

DIMENSIONS in millimeters





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