PM5307

TBS™ 9953

OC-192 TelecomBus Serializer

Data Sheet

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Issue 6: January 2003

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US patent # 6,316,977B1

Relevant patent applications and other patents may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
6	January 2003	Corrected marketing number on title page from PM5374 to PM5307 Removed pin L8 from VSS pin description section. Added reference to PMC-2021638, Jitter Budget and Pre-Emphasis Setting for the TSE 160 and TBS 9953. Added ELVDS Tx Differential transition time to Table 50
5	September 2002	Removed face powerdown function, changed POWERDOWN bits description. Removed ELVDS powerdown function, changed ELVDS_PWRDNB bits description. Removed ELVDS_PWRDNB and POWERDOWN functions from Powerdown Summary Table. Added ELVDS low power mode to same section. Renamed Section to Low Power Modes Summary Added note about precedence of Connection ID insertion over AIS insertion. Updated Power Sequencing section. Added advisory section incorporating issues from errata: • OSYSCLK Pin Removed • Random Line Code Violation Counts on Unprovisioned 777Mb/s Timeslots • OFAAIS Data Corruption On STS-12 And STS-48 Scrambled Links • Data Recovery On SONET Scrambled Links • Floating 8B/10B Link Frame Alignment Status • Constant OFAV Status At 8B/10B Receiver • Removal From Power-Down Mode on Device Power-Up Added PMC-2010750 to References section Noted RSEF can lose frame in SNRZ mode in min of 3 frames. Added note about unknown default to TIP bit description Added note about unknown default to RSEF_TIP bit description Added note about unknown default to PIPM_TIP bit description Added note about unknown default to RTSI BUSY bit description Updated max operating junction temperature. Updated Power Requirements Section. Changed Serial TX jitter spec from Max to Typical.
4	June 2002	Updated Patent information Updated ELVDS 2.488 Gbit/s Reach to 40” Corrected PIPM synchronization data requirements. Corrected Address range for Port Register Set 1 in Register Memory Map table. Exposed WCIMODE in data sheet. Exposed Connection ID generation/monitoring function in datasheet. (Registers MN21H – MN2DH)Fixed Default value on MCIDI[47:0] bits. Added qualification to MCIDI bits indicating that interrupt not suppressed on changes to PSEL bits or RWSEL_A/B pins. Fixed Default on TTSI Interrupt Enable Register #1 (MN23h) ACTIVE bit

Issue No.	Issue Date	Details of Change
		Changed A1ES default state to X, Added to B1ERR, A1ES bit descriptions Clarification added for meaning of default value X in Register bit description tables. Clarified requirements for power down operation for POWERDOWN and ELVDS_PWRDNB bits. Removed CSUI from list of blocks affected by FACE_RESET and DBLOCK_RESET register bits. Relaxed restriction on REFCLK selection as the source for the core clock in CORE_SRC register bit description. Corrected LCVE description with respect to correct value for SNRZ operation. Added warning about loss of character and frame alignment in downstream devices resulting from LCVP use. Added warning about potential temporary data loss resulting from use of CENTER bit. BUSY_CID default value changed to X. CAP_CIDV bit description clarified. Added recommendation for use of J0INS register bit. Updated instructions for general device initialization in Operations section. Added TBS initialization section to Operations section Added TBS Switch Setting section to Operations section Qualified RWSEL_A/B, CMP_A/B pin descriptions to declare them as essentially 8 kHz signals. Added Power down Summary to Operation Section W/P/A Interface Location section added to Operation Section Added Connection ID Monitoring Section to Operations Section Added Indirect Access Operation Duration Section Added Data Delay diagrams and example table to Transmit Interface Timing section. Added Rev B Device Latency column to Data Transmit Delay table Updated Power Requirements table from validation results Updated hold times on SYSCLK sampled pins. Added new jitter specs for Reference clock, and ELVDS I/O Created new section with new information for ELVDS DC Specs
3	February 2002	Added Boundary Scan Register Table Added FBDIV setting for REFCLK = 77.76 kHz Added requirement for connecting all REFCLK pins Replaced STS-52 core timeslot mode with 48 core timeslot mode Removed STS-51 2.643 Gbit/s link rate feature Renamed TXMUX_EN bit to SLAVE bit. Changed SLAVE bit description. Corrected ACCOUPLE description Remove CSU_TM_TCK from datasheet. Removed requirement that CSU_TM_TCK be set high during power down.

Issue No.	Issue Date	Details of Change
		TM_FBDIVCTRL requirements changed. RTSI J0/Z0 reordering bypass support removed. RTSI J0RORDR bit becomes RESERVED. TTSI J0/Z0 reordering bypass support removed. TTSI J0RORDR bit becomes RESERVED. Added Jitter spec for STS-12 SNRZ operation. Updated jitter specs for other operation modes. Updated power sequencing description. DATA_MONA removed from data sheet. M_RAx, S_RAx bits removed. S_LOCKx bits renamed PLL_LOCKx. PISO_BOOST renamed PREEMPH_EN OSYSCLK pin removed CORE_FP_CENTER description updated. Added note indicating that the control memories do not have a default following reset. to each indirect access data register. Changed default for ETD_SEL[5:0] register. Updated Receive and Transmit Functional Timing Sections Exposed RJ0FPAEA register. Added power requirements section. Relocated power filtering, power up and power consumption information to that section. Updated block diagram
2	May 2001	Register 30H CCK_ACTIVE, REFCLK_ACTIVE activity monitor register added. Registers 30H-31H: Addition PLL lock status visible. Now there are master and slave PLL lock status that are available, with status, enable and indication registers. Indication bits now marked read only. Register 32H. FBDIV now 11 bits. Register 33H: ELVDS_PWRDNB bit added. CSU_RSTB renamed ELVDS_RSTB, default value now 1. CSU_CCKSEL moved to register 33H. Register 33H default value changes. Register 34H CSU_PLLTEST_OE[3:0], CSU_ATP_OE[3:0] added. Register 35H Now all CSU_TM_PLLTSEL bits. Register 36H: All new Face Configuration register. Changed Register Map – registers 34H, 35H, 3CH, 3DH, 44H, 45H, 4CH, 4DH removed. Register MN03 RXLV_HSIN_REDSEL control bit removed. Register MN04H: Removed most of the analog control. Register MN32H: Removed most of the analog control. Added VDDA[20:17] pins, TJ0FPA, and TJ0FPB pulse width changed from 10 to 20 ns. Changed RJ0DLY_A, RJ0DLY_B limits. Updated Core Clock Period table. RAWPRBS description updated to remove reference to PRBS monitoring. Removed WPOFFSET references. Added restriction to CORE_SRC register description. Restrictions on use of LCVI and BIP8I added. I/O power consumption added to power consumption section. Corrected Transmit Interface Timing Section. Qualified the conditions for character insertion for OFAAIS register bit. Addition of CORE_FP_CENTER bit. Restricted valid settings for WPMASK. Added note for Indirect Data registers in SSWE, RTSI and TTSI, that registers must be written to before and indirect write is triggered. K23.7 removed from list of control character line code violation exceptions. FILT[2] register bit becomes FILTB[2]. Added input port replication functionality with SWAP_INPUTB register bit. Added transmit channel muxing feature, with support register bits TXCHAN_SEL, TXMUX_EN. Removed B1/E1 monitoring registers in TTSI registers. Incremented legal value range on RJ0DLY_A/B registers. RJ0DLY_A/B now default to 0x0001. Added TJ0FPA, TJ0FPB Timing section. RXLV_EN

Issue No.	Issue Date	Details of Change
		register bits redocumented as CH_ENB bits. CSU_PLLTEST_OE[0] register bit redocumented as CSU_PLLTEST_OEB[0], defaults to 1. Addition of ACCOUPLE control bits. Added ball diagrams. Added ball locations to pin description table. Added channel enabling to initialization procedures in Operation section. Added J0Z0TPINS register bits to support character insertion in J0/Z0 bytes. Added recommendation to Operation section to set Register MN32H: J0Z0TPINS register and Register MN31H: TP[7:0] during setup for scrambled links.
1	January 2001	Document Created.

Table of Contents

List of Registers

List of Figures

List of Tables

1 Features

- The PM5307 TBS™ 9953 switches timeslots (down to an STS-1 granularity) from/to the line side interface to/from a system side working (W), protection (P), and/or optionally an auxiliary (A) interface.
- 4 sets of 16 port ELVDS serial links:
  - 2 faces of either 16x777.6 Mbit/s links (8B/10B encoded Serial TelecomBus) or 16x622.08 Mbit/s links (SONET/SDH Scrambled).
  - 2 faces of configurable 16x777.6 Mbit/s (8B/10B encoded Serial TelecomBus) or 16x622.08 Mbit/s, 16x2.488 Gbit/s (SONET/SDH scrambled).
- Supports two sets of connection maps (active and standby) and a controlled method of changing settings on STS-1 frame boundaries.
- Typical applications (line to system interfaces):
  - Mode 1: 16x777.6 Mbit/s to 3x16x777.6 Mbit/s (W, P, A).
  - Mode 2: 16x777.6 Mbit/s to 4x4x2.488 Gbit/s (W, P, A1, A2).
  - Mode 3: 2x(16x777.6) Mbit/s to 2x(2x4x2.488) Gbit/s (W, P) - Dual TBS.
  - Mode 4: 4x2.488 Gbit/s to 3x4x2.488 Gbit/s (W, P, A).
  - Mode 5: 2x(16x777.6) Mbit/s to 2x(3x4x2.488) Gbit/s (W, P, A).
- Supports redundant working/protection time-space-time switch fabrics, using the PM5372 TSE, PM5374 TSE 160, or other fabric devices.
- Supports STS-192c/STM-64c, STS-48c/STM-16c, STS-12c/STM-4c, and STS-3c/STM-1 traffic on the interfaces.
- Supports through-traffic, drop-traffic and protection switching in UPSR, 2-fibre BLSR and 4-fibre BLSR applications.
- Provides OC-192 time-slot interchange on the line, working, and protect interfaces to allow arbitrary arrangement of time-slots at STS-1 granularity on each interface.
- Provides per link concatenated SONET PRBS generation/monitoring for outgoing/incoming ELVDS data link for off-line link verification. 622.08 Mbit/s links may optionally carry an STS-12c PRBS stream. 777.6 Mbit/s links may optionally carry an STS-12c PRBS stream. 2.488 Gbit/s links may optionally carry an STS-48c PRBS stream.
- Provides in-service connection verification by optionally checking and/or overwriting the Z2 byte of each constituent STS-1/STM-0 with a software programmable Connection Identifier
- Provides in-service link verification:
  - Line Code Violations (LCVs) are monitored on extended 8B/10B flows.
  - Bit Interleaved Parity (BIP-8) errors are monitored, and the B1 bytes are optionally generated on scrambled flows.

- Provides pins to coordinate updating of the connection map of the time-slot interchange blocks in the local device, peer PM5307 TBS 9953 devices, and companion PM5374 TSE 160 or PM5372 TSE™ devices.
- Provides two independent time planes (A and B) for frame alignment purposes. The time plane for each group of four receive links and four transmit links is independently selectable through the software interface.
- Provides two Receive Working/Protect Selection controls, one for each time plane. These allow independent switchover between working and protect interfaces.
- Driven by a 155.52 or 77.76 MHz reference clock.
- 1.8 V CMOS core and 3.3 V CMOS I/O and 1.8V ELVDS I/O.
- 0.18μm CMOS process.
- Packaged in an 1152 ball Flip Chip Ball Grid Array (FCBGA).
- Requires no external RAMs or logic parts.
- Provides a standard IEEE 1149.1 JTAG port.
- Supports a 16-bit microprocessor interface that is used to initialize the device, to write switch settings into on-chip control tables, and to monitor device performance.

2 Applications

- Sub-wavelength Cross Connects
- Multi-service Provisioning Platforms
- SONET/SDH Digital Cross Connects
- SONET/SDH Add/drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers
- TelecomBus Backplane Driver

3 References

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3. ITU, Recommendation G.707 - "Digital Transmission Systems – Terminal equipments - General", March 1996.

4. IEEE 802.3, "Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications", Section 36.2, 1998.

5. A.X. Widmer and P.A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM Journal of Research and Development, Vol. 27, No 5, September 1983, pp 440-451.

6. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, "Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code," December 4, 1984.

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8. L.R. Ford, D.R. Fulkerson, "Flows in Networks", Maximum Cardinality Matchings in Bipartite Graphs.

9. PMC-2011065, "POWER SUPPLY FILTERING RECOMMENDATIONS FOR 10G CHESS DEVICES", Issue 2.

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12. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions -Junction-to-Board: JESD51-8*. October 1999.

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4 Application Examples

Figure 1 Multi-Service Switch (with 2.488 Gbit/s Backplane)

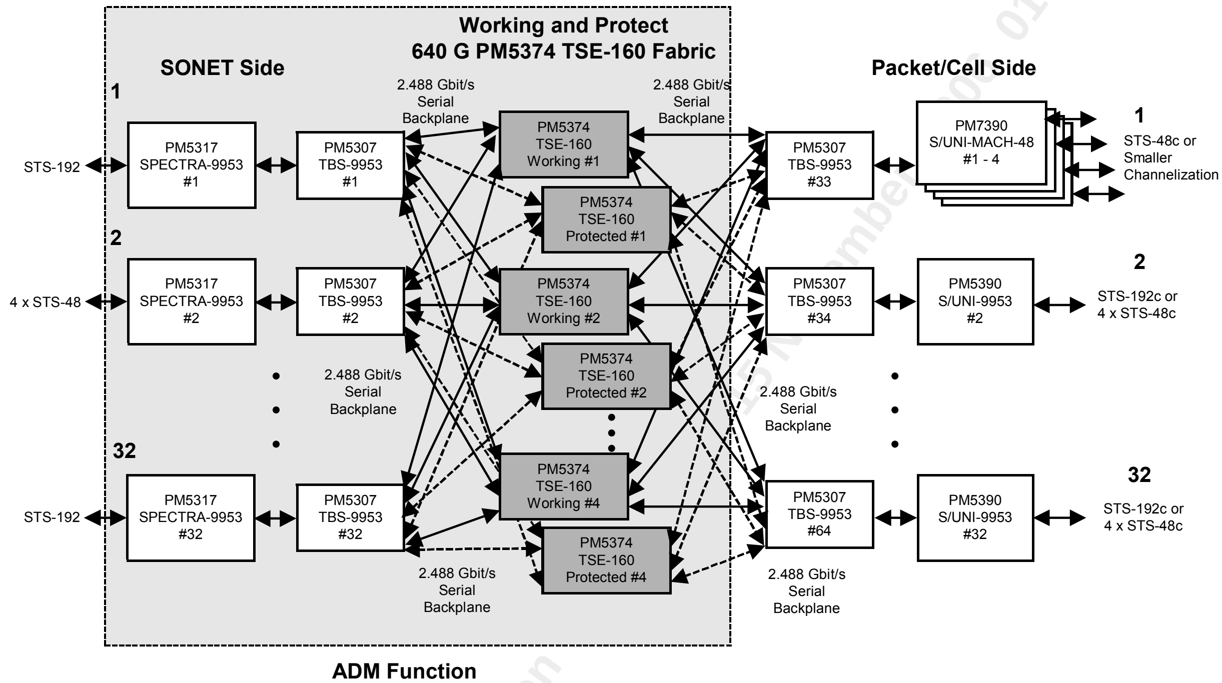


Figure 2 OC-192 Multi-service ADM

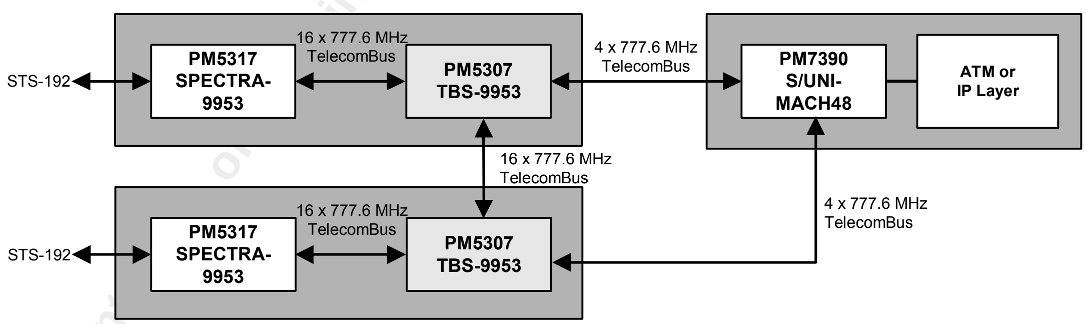


Figure 3 OC-192 Line Cards

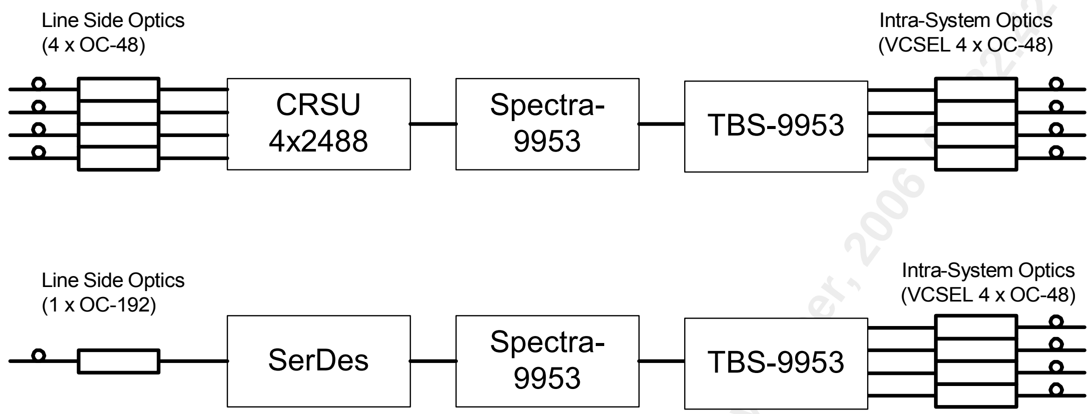
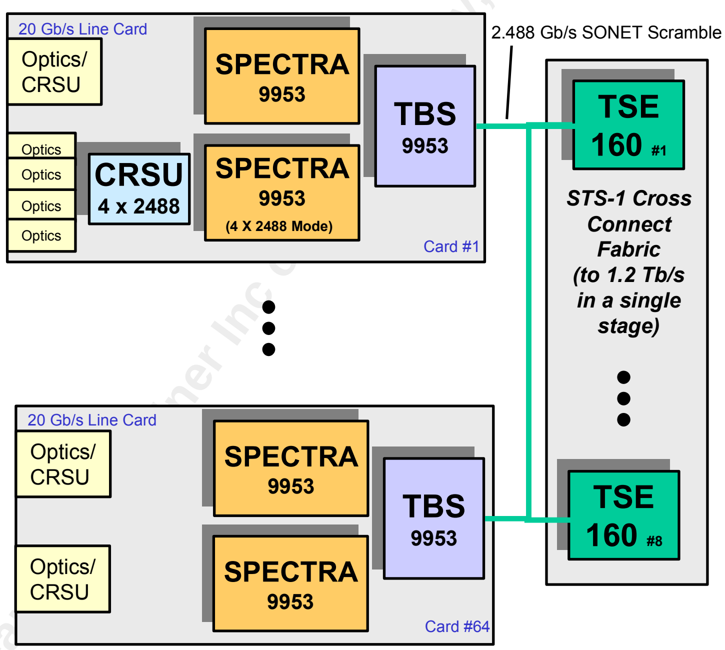
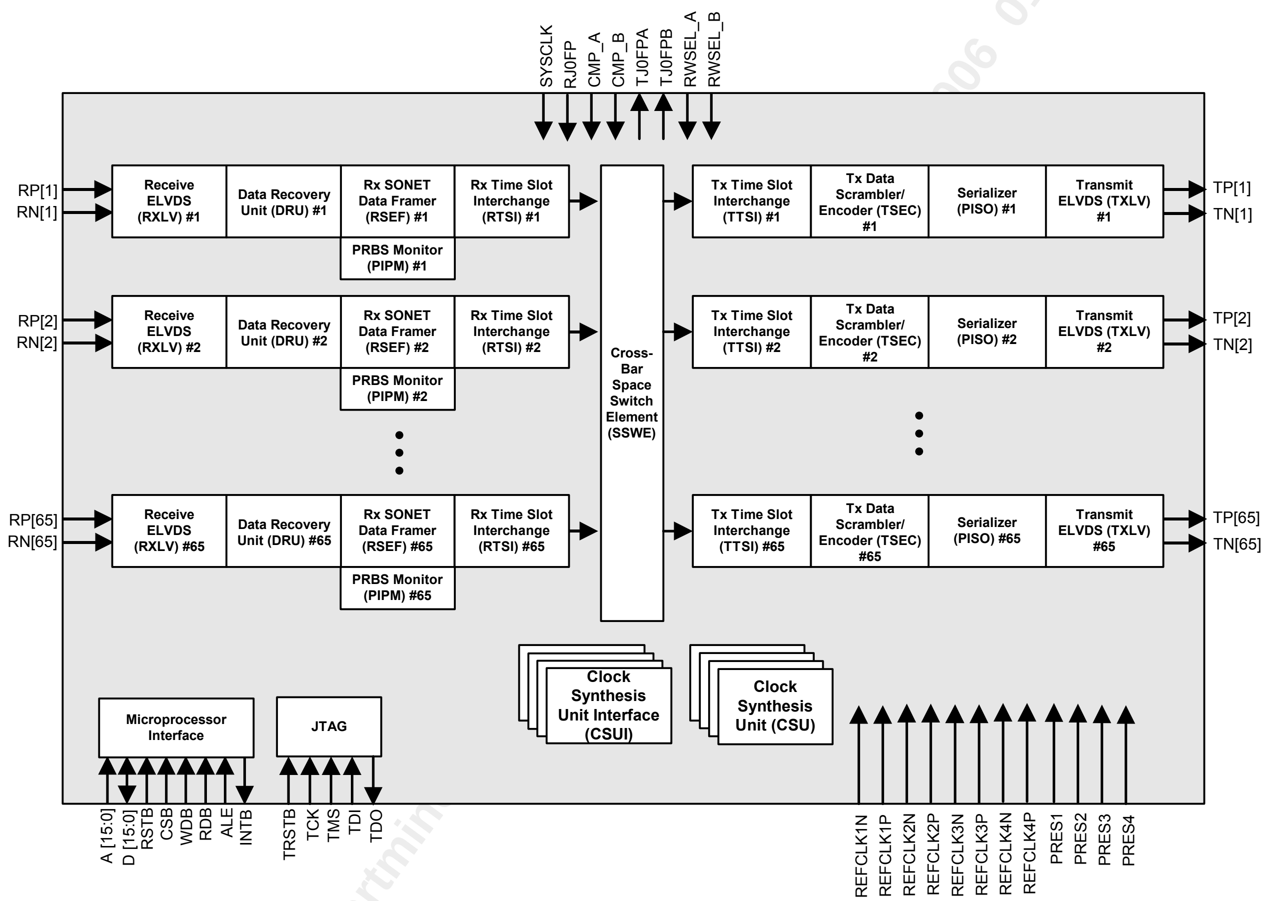


Figure 4 1.28 Terabit STS-1 Cross-connect



5 Block Diagram

Figure 5 TBS 9953 Block Diagram



6 Description

The PM5307 TBS 9953 is a monolithic integrated circuit that implements a multiplexing/demultiplexing/switching function between a high-speed bit-serial ELVDS DataStream on the line side, and working, protect, and auxiliary high-speed bit-serial ELVDS interfaces on the system side. The device has four faces of 16 bidirectional links. Two faces support either 16 x 0.622 or 16 x 0.7776 Gbit/s links, each link carrying an STS-12 equivalent flow. Two faces are configurable to either 16 x 0.622 Gbit/s (STS-12), 16 x 0.7776 Gbit/s (8B/10B encoded STS-12), or 16 x 2.488 Gbit/s (STS-48) links. These four faces can be arbitrarily configured as line, system working, protect and auxiliary interfaces. The TBS 9953 can be used to connect the SONET/SDH framer devices (e.g. PM5317 SPECTRA™ 9953) to ATM/POS processor devices (e.g. PM7390 S/UNI® MACH48 or PM5390 S/UNI 9953) on the line side, or to SONET/SDH cross-connect devices (e.g. PM5372 TSE, PM5374 TSE 160) on the system side.

Data on 777.6 Mbit/s STS-12 configured links is encoded using an extended 8B/10B based Serial TelecomBus format. Transport and payload frame boundaries, pointer justification events and alarm conditions are marked by 8B/10B control characters.

Data on 622 Mbit/s STS-12, and STS-48 configured links is scrambled.

A set of 16 STS-12 links can be aggregated to carry an STS-192c/STM-64c stream, four STS-48c/STM-16c streams, or 16 STS-12c/STM-4c streams. A set of 4 STS-48 links can be aggregated to carry an STS-192c/STM-64c stream, or four STS-48c/STM-16c streams.

Per link pseudo-random bit sequence (PRBS) generation and monitoring can be configured for concatenated SONET/SDH frames with PRBSed payloads. If a link is configured for STS-Nc operation and PRBS is enabled for that link, the PRBS stream that is generated and monitored will be an STS-Nc PRBS stream.

Time-slot interchange and space switching blocks are provided to allow arbitrary mapping of streams between the line side DataStream and the system side working, protect, and auxiliary data streams at STS-1/AU3 granularity. Data on the outgoing line side interface may be sourced from arbitrary time-slots on either of the working, protect and auxiliary interfaces. Multi-cast is supported.

Per STS-1 software programmable Connection Identifiers (CID) can be inserted /monitored in the Z2 byte of each STS-1. The CID includes a 6-bit user defined field that is not monitored, and a 18 bit monitored field.

The TBS 9953 supports a microprocessor interface for startup, test modes, and the setting of the control RAMs.

The TBS 9953 supports JTAG for board testing.

7 Pin Diagram

Figure 6 TBS 9953 Pin Diagram

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
A		VDDI	TP[18]	TP[19]	TP[22]	TP[23]	VSS	VDDO	TP[26]	TP[27]	TP[30]	TP[31]	VSS	VDDI	PRES2	VDDA8	VDDA9
B	VDDI	VDDI	VSS	TN[18]	TN[19]	TN[22]	TN[23]	VDDO	VSS	TN[26]	TN[27]	TN[30]	TN[31]	VDDI	VSS	VDDA11	VDDA7
C	RN[16]	VSS	VSS	VDDO	TP[17]	TP[20]	TP[21]	TP[24]	VSS	VDDO	TP[25]	TP[28]	TP[29]	TP[32]	VSS	VDDI	REFCLK2N
D	RN[13]	RP[16]	VDDO	VDDO	VSS	TN[17]	TN[20]	TN[21]	TN[24]	VDDO	VSS	TN[25]	TN[28]	TN[29]	TN[32]	VDDI	VSS
E	RN[12]	RP[13]	RN[15]	VSS	VSS	VDDI	A3	A5	A15	A13	VSS	VDDO	VDDO	VSS	VSS	VDDA12	VSS
F	RN[9]	RP[12]	RN[14]	RP[15]	VDDI	VDDI	VSS	A2	A4	A14	A12	VDDO	VSS	VSS	VDDO	VDDO	VDDI
G	VSS	RP[9]	RN[11]	RP[14]	VDDI	VSS	VSS	VDDI	A1	A7	A9	A11	VSS	VDDO	VDDO	VSS	VSS
H	VDDO	VDDO	RN[10]	RP[11]	VSS	VSS	VDDI	VDDI	VSS	A0	A6	A8	A10	VDDO	VSS	VSS	VDDO
J	RN[8]	VSS	VSS	RP[10]	VSS	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO
K	RN[5]	RP[8]	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS
L	RN[4]	RP[5]	RN[7]	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS
M	RN[1]	RP[4]	RN[6]	RP[7]	VDDO	VDDO	VDDI	VDDI	VDDO	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO
N	VSS	RP[1]	RN[3]	RP[6]	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO
P	VDDI	VDDI	RN[2]	RP[3]	VSS	VSS	VDDO	VDDO	VSS	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI
R	RESERVED	VSS	VSS	RP[2]	VSS	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS
T	RESERVED	RESERVED	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS
U	VDDA4	RESERVED	REFCLK1P	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS
V	VDDA3	VDDA5	REFCLK1N	VSS	VSS	VDDI	VSS	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS
W	PRES1	VDDA1	VDDI	VDDI	VDDA6	VDDO	VSS	VSS	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS
Y	VDDA2	VSS	VSS	TN[15]	VSS	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS
AA	VDDI	VDDI	TP[15]	TN[14]	VSS	VSS	VDDO	VDDO	VSS	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI
AB	VSS	TN[16]	TP[14]	TN[11]	VDDO	VSS	VSS	D12	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO
AC	TP[16]	TN[13]	TP[11]	TN[10]	VDDO	VDDO	D13	D11	VDDO	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO
AD	TP[13]	TN[12]	TP[10]	VSS	VSS	D14	D10	D4	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS
AE	TP[12]	TN[9]	VDDO	VDDO	D15	D9	D5	D3	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS
AF	TP[9]	VSS	VSS	TN[7]	D8	D6	D2	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO
AG	VDDO	VDDO	TP[7]	TN[6]	D7	D1	VDDI	VDDI	VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	VSS	VDDO
AH	VSS	TN[8]	TP[6]	TN[3]	D0	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI
AJ	TP[8]	TN[5]	TP[3]	TN[2]	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	RESERVED	VDDO	VDDO	VDDA23
AK	TP[5]	TN[4]	TP[2]	VSS	VSS	VDDI	VDDI	VSS	VSS	VDDI	VSS	VDDO	RESERVED	VSS	VDDA20	PRES4	VSS
AL	TP[4]	TN[1]	VDDO	VDDO	VSS	RP[64]	RP[63]	RP[60]	RP[59]	VDDO	VSS	RP[56]	RP[55]	RP[52]	RP[51]	VDDI	VSS
AM	TP[1]	VSS	VSS	VDDO	RN[64]	RN[63]	RN[60]	RN[59]	VSS	VDDO	RN[56]	RN[55]	RN[52]	RN[51]	VSS	VDDI	VDDA22
AN	VDDI	VDDI	VSS	RP[65]	RP[62]	RP[61]	RP[58]	VDDO	VSS	RP[57]	RP[54]	RP[53]	RP[50]	VDDI	VSS	RP[49]	RESERVED
AP		VDDI	RN[65]	RN[62]	RN[61]	RN[58]	VSS	VDDO	RN[57]	RN[54]	RN[53]	RN[50]	VSS	VDDI	RN[49]	RESERVED	VDDA19
	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VDDA10	RESERVED	RESERVED	VDDI	VSS	RN[18]	RN[19]	RN[22]	RN[23]	VDDO	VSS	RN[25]	RN[28]	RN[29]	RN[32]	VDDI		A
RESERVED	RESERVED	VSS	VDDI	RP[18]	RP[19]	RP[22]	RP[23]	VSS	VDDO	RP[25]	RP[28]	RP[29]	RP[32]	VSS	VDDI	VDDI	B
REFCLK2P	VDDI	VSS	RN[17]	RN[20]	RN[21]	RN[24]	VDDO	VSS	RN[26]	RN[27]	RN[30]	RN[31]	VDDO	VSS	VSS	TP[33]	C
VSS	VDDI	RP[17]	RP[20]	RP[21]	RP[24]	VSS	VDDO	RP[26]	RP[27]	RP[30]	RP[31]	VSS	VDDO	VDDO	TN[33]	TP[36]	D
VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	TP[34]	TN[36]	TP[37]	E
VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VDDI	VSS	VDDI	VDDI	TN[34]	TP[35]	TN[37]	TP[40]	F
VDDI	VDDI	VDDO	VDDO	VSS	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	TCK	TN[35]	TP[38]	TN[40]	VSS	G
VDDO	VSS	VSS	VDDO	VSS	VSS	VDDI	VDDI	VSS	VDDI	VDDI	TDO	CMP_A	TN[38]	TP[39]	VDDO	VDDO	H
VDDO	VDDO	VSS	VDDO	VDDO	VSS	VSS	VDDI	VSS	VSS	VSS	CMP_B	RESERVED	TN[39]	VSS	VSS	TP[42]	J
VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	RWSEL_A	RJ0FP	TJ0FPB	VDDO	VDDO	TN[42]	TP[43]	K
VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VSS	RWSEL_B	RSTB	VDDO	VSS	VSS	TP[41]	TN[43]	TP[46]	L
VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VSS	SYSCLK	ALE	VDDO	VDDO	TN[41]	TP[44]	TN[46]	TP[47]	M
VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	INTB	VSS	VSS	VDDO	TN[44]	TP[45]	TN[47]	VSS	N
VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VSS	VDDO	VDDO	VSS	VSS	TN[45]	TP[48]	VDDI	VDDI	P
VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	TN[48]	VSS	VSS	PRES3	R
VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VSS	VDDO	VDDA18	VDDI	VDDI	VDDA17	VDDA14	T
VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VSS	VSS	REFCLK3N	VDDA13	VDDA15	U
VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	REFCLK3P	RESERVED	VDDA16	V
VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VSS	VDDO	VDDI	VDDI	VDDI	RESERVED	RESERVED	W
VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	RP[34]	VSS	VSS	RESERVED	Y
VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VSS	VDDO	VDDO	VSS	VSS	RP[35]	RN[34]	VDDI	VDDI	AA
VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	RP[38]	RN[35]	RP[33]	VSS	AB
VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDO	VSS	VSS	VDDO	VDDO	RP[39]	RN[38]	RP[36]	RN[33]	AC
VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VSS	VDDO	VDDO	VSS	VSS	RN[39]	RP[37]	RN[36]	AD
VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDI	VDDO	VDDO	VDDO	RP[40]	RN[37]	AE
VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	RP[42]	VSS	VSS	RN[40]	AF
VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VSS	VSS	RP[43]	RN[42]	VDDO	VDDO	AG
VDDI	VSS	VDDO	VDDO	VSS	VDDI	VSS	VSS	VDDI	VDDI	VSS	VSS	VDDI	RP[46]	RN[43]	RP[41]	VSS	AH
VDDI	VDDO	VDDO	VSS	VSS	VDDO	RDB	TJ0FPA	VDDI	TDI	VSS	VDDI	VDDI	RP[47]	RN[46]	RP[44]	RN[41]	AJ
VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	WRB	CSB	TRSTB	TMS	VDDI	VSS	VSS	RN[47]	RP[45]	RN[44]	AK
VSS	VDDI	TN[64]	TN[61]	TN[60]	TN[57]	VSS	VDDO	TN[55]	TN[54]	TN[51]	TN[50]	VSS	VDDO	VDDO	RP[48]	RN[45]	AL
VDDA21	VDDI	VSS	TP[64]	TP[61]	TP[60]	TP[57]	VDDO	VSS	TP[55]	TP[54]	TP[51]	TP[50]	VDDO	VSS	VSS	RN[48]	AM
REFCLK4N	TN[65]	VSS	VDDI	TN[63]	TN[62]	TN[59]	TN[58]	VSS	VDDO	TN[56]	TN[53]	TN[52]	TN[49]	VSS	VDDI	VDDI	AN
VDDA24	REFCLK4P	TP[65]	VDDI	VSS	TP[63]	TP[62]	TP[59]	TP[58]	VDDO	VSS	TP[56]	TP[53]	TP[52]	TP[49]	VDDI		AP
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 Pin Description

Table 1 Pin Description

Pin Name	Type	Pin No.	Function
ELVDS Ports (260 Signals)			
RP[1]	Analog ELVDS Input	N33	**Receive Serial Data.** The differential receive serial data links (RP[65:1]/RN[65:1]) carry the receive SONET/SDH frame data from upstream sources in bit serial format. In STS-12 mode, each differential pair RP[*X*]/RN[*X*] carries a constituent STS-12 stream. Data on RP[*X*]/RN[*X*] is scrambled or encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. In STS-48 mode, each differential pair RP[*X*]/RN[*X*] carries a constituent STS-48 stream. Data on RP[*X*]/RN[*X*] is scrambled. The most significant bit of each byte is transmitted first and the least significant bit is transmitted last. Links 33-65 are configurable to either STS-12 or STS-48 mode. Links 1-32 are fixed at STS-12 mode. Link rates of configurable links are configured by the STSLR register bits. RP[*X*]/RN[*X*] differential pairs are grouped into faces of links. Face 1 consists of links 1-16. Face 2 consists of links 17-32. Face 3 consists of links 33-48. Face 4 consists of links 49-65 All RP[*X*]/RN[*X*] differential pairs on a face must be frequency locked to each other. If multiple faces are configured to the same rate of operation, all RP[*X*]/RN[*X*] differential pairs on those faces must be frequency locked. Unused RP[X]/RN[X] pad pairs can be left floating if the associated internal analog blocks (RXLV #X and DRU #X) are disabled.
RN[1]		M34	
RP[2]		R31	
RN[2]		P32	
RP[3]		P31	
RN[3]		N32	
RP[4]		M33	
RN[4]		L34	
RP[5]		L33	
RN[5]		K34	
RP[6]		N31	
RN[6]		M32	
RP[7]		M31	
RN[7]		L32	
RP[8]		K33	
RN[8]		J34	
RP[9]		G33	
RN[9]		F34	
RP[10]		J31	
RN[10]		H32	
RP[11]		H31	
RN[11]		G32	
RP[12]		F33	
RN[12]		E34	
RP[13]		E33	
RN[13]		D34	
RP[14]		G31	
RN[14]		F32	
RP[15]		F31	
RN[15]		E32	
RP[16]		D33	
RN[16]		C34	
RP[17]		D15	
RN[17]		C14	
RP[18]		B13	
RN[18]		A12	
RP[19]		B12	
RN[19]		A11	
RP[20]		D14	
RN[20]		C13	
RP[21]		D13	
RN[21]		C12	
RP[22]		B11	
RN[22]		A10	
RP[23]		B10	
RN[23]		A9	
RP[24]		D12	
RN[24]		C11	
RP[25]		B7	

Pin Name	Type	Pin No.	Function
RN[25]		A6	
RP[26]		D9	
RN[26]		C8	
RP[27]		D8	
RN[27]		C7	
RP[28]		B6	
RN[28]		A5	
RP[29]		B5	
RN[29]		A4	
RP[30]		D7	
RN[30]		C6	
RP[31]		D6	
RN[31]		C5	
RP[32]		B4	
RN[32]		A3	
RP[33]		AB2	
RN[33]		AC1	
RP[34]		Y4	
RN[34]		AA3	
RP[35]		AA4	
RN[35]		AB3	
RP[36]		AC2	
RN[36]		AD1	
RP[37]		AD2	
RN[37]		AE1	
RP[38]		AB4	
RN[38]		AC3	
RP[39]		AC4	
RN[39]		AD3	
RP[40]		AE2	
RN[40]		AF1	
RP[41]		AH2	
RN[41]		AJ1	
RP[42]		AF4	
RN[42]		AG3	
RP[43]		AG4	
RN[43]		AH3	
RP[44]		AJ2	
RN[44]		AK1	
RP[45]		AK2	
RN[45]		AL1	
RP[46]		AH4	
RN[46]		AJ3	
RP[47]		AJ4	
RN[47]		AK3	
RP[48]		AL2	
RN[48]		AM1	
RP[49]		AN19	
RN[49]		AP20	
RP[50]		AN22	
RN[50]		AP23	
RP[51]		AL20	
RN[51]		AM21	
RP[52]		AL21	
RN[52]		AM22	
RP[53]		AN23	

Pin Name	Type	Pin No.	Function
RN[53] RP[54] RN[54] RP[55] RN[55] RP[56] RN[56] RP[57] RN[57] RP[58] RN[58] RP[59] RN[59] RP[60] RN[60] RP[61] RN[61] RP[62] RN[62] RP[63] RN[63] RP[64] RN[64] RP[65] RN[65]		AP24 AN24 AP25 AL22 AM23 AL23 AM24 AN25 AP26 AN28 AP29 AL26 AM27 AL27 AM28 AN29 AP30 AN30 AP31 AL28 AM29 AL29 AM30 AN31 AP32	
TP[1] TN[1] TP[2] TN[2] TP[3] TN[3] TP[4] TN[4] TP[5] TN[5] TP[6] TN[6] TP[7] TN[7] TP[8] TN[8] TP[9] TN[9] TP[10] TN[10] TP[11] TN[11] TP[12] TN[12] TP[13] TN[13] TP[14] TN[14] TP[15] TN[15] TP[16]	Analog ELVDS Output	AM34 AL33 AK32 AJ31 AJ32 AH31 AL34 AK33 AK34 AJ33 AH32 AG31 AG32 AF31 AJ34 AH33 AF34 AE33 AD32 AC31 AC32 AB31 AE34 AD33 AD34 AC33 AB32 AA31 AA32 Y31 AC34	**Transmit Serial Data.** The differential transmit working serial data links (TP[65:1]/TN[65:1]) carry the transmit data to downstream devices in bit serial format. In STS-12 mode each differential pair carries a constituent STS-12 stream. Data on TP[*X*]/TN[*X*] is scrambled or encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last. In STS-48 mode each differential pair TP[*X*]/TN[*X*] carries a constituent STS-48 stream. Data on TP[*X*]/TN[*X*] is scrambled. The most significant bit is transmitted first and the least significant bit is transmitted last. Links 33-65 are configurable to either STS-12 or STS-48 mode. Links 1-32 are fixed at STS-12 mode. Link rates of configurable links are configured by the STSLR register bits. TP[*X*]/TN[*X*] differential pairs are grouped into faces of links. Face 1 consists of links 1-16. Face 2 consists of links 17-32. Face 3 consists of links 33-48. Face 4 consists of links 49-65 All TP[*X*]/TN[*X*] differential pairs on a face are frequency locked to each other. If multiple faces are configured to the same rate of operation, all TP[*X*]/TN[*X*] differential pairs on those faces are be frequency locked. Unused TP[X]/TN[X] pad pairs can be left unconnected.

Pin Name	Type	Pin No.	Function
TN[16]		AB33	
TP[17]		C30	
TN[17]		D29	
TP[18]		A32	
TN[18]		B31	
TP[19]		A31	
TN[19]		B30	
TP[20]		C29	
TN[20]		D28	
TP[21]		C28	
TN[21]		D27	
TP[22]		A30	
TN[22]		B29	
TP[23]		A29	
TN[23]		B28	
TP[24]		C27	
TN[24]		D26	
TP[25]		C24	
TN[25]		D23	
TP[26]		A26	
TN[26]		B25	
TP[27]		A25	
TN[27]		B24	
TP[28]		C23	
TN[28]		D22	
TP[29]		C22	
TN[29]		D21	
TP[30]		A24	
TN[30]		B23	
TP[31]		A23	
TN[31]		B22	
TP[32]		C21	
TN[32]		D20	
TP[33]		C1	
TN[33]		D2	
TP[34]		E3	
TN[34]		F4	
TP[35]		F3	
TN[35]		G4	
TP[36]		D1	
TN[36]		E2	
TP[37]		E1	
TN[37]		F2	
TP[38]		G3	
TN[38]		H4	
TP[39]		H3	
TN[39]		J4	
TP[40]		F1	
TN[40]		G2	
TP[41]		L3	
TN[41]		M4	
TP[42]		J1	
TN[42]		K2	
TP[43]		K1	
TN[43]		L2	
TP[44]		M3	

Pin Name	Type	Pin No.	Function
TN[44]		N4	
TP[45]		N3	
TN[45]		P4	
TP[46]		L1	
TN[46]		M2	
TP[47]		M1	
TN[47]		N2	
TP[48]		P3	
TN[48]		R4	
TP[49]		AP3	
TN[49]		AN4	
TP[50]		AM5	
TN[50]		AL6	
TP[51]		AM6	
TN[51]		AL7	
TP[52]		AP4	
TN[52]		AN5	
TP[53]		AP5	
TN[53]		AN6	
TP[54]		AM7	
TN[54]		AL8	
TP[55]		AM8	
TN[55]		AL9	
TP[56]		AP6	
TN[56]		AN7	
TP[57]		AM11	
TN[57]		AL12	
TP[58]		AP9	
TN[58]		AN10	
TP[59]		AP10	
TN[59]		AN11	
TP[60]		AM12	
TN[60]		AL13	
TP[61]		AM13	
TN[61]		AL14	
TP[62]		AP11	
TN[62]		AN12	
TP[63]		AP12	
TN[63]		AN13	
TP[64]		AM14	
TN[64]		AL15	
TP[65]		AP15	
TN[65]		AN16	

Pin Name	Type	Pin No.	Function
Control and Clocking (21 Signals)			
SYSCLK	Input	M8	**System Clock.** The system clock signal (SYSCLK) provides frame timing for the device. When register bit R8KCLK in Master Configuration #2 Register 0003H is high (8kHz frame pulse mode), SYSCLK is an 8kHz clock, with a nominal 50% duty cycle. SYSCLK is also used as the frame pulse and the RJ0FP signal is ignored. A software configurable delay from SYSCLK rising edge are used to indicate that the J0 section trace byte has been delivered on all the receive serial data links (RP[65:1]/RN[65:1]) and J0 bytes are ready for processing by the time-space-time switching elements. When register bit R8KCLK is low (77MHz frame pulse mode), SYSCLK is a 77.76 MHz clock with a nominal 50% duty cycle. The RJ0FP input is used as the frame pulse. SYSCLK and the PECL reference clock must be derived from a common clock source. CMP_A, CMP_B, RWSEL_A, RWSEL_B, and RJ0FP are sampled on the rising edge of SYSCLK.
REFCLK1N REFCLK1P	Input	V32 U32	**Reference Clock 1.** The PECL reference clock signals (REFCLK1N/REFCLK1P) provide a clock reference for one of the 4 clock synthesis unit blocks on the device, which in turn generates the transmit serial data clock for links 1-16. REFCLK1 can be either a 155.52 MHz clock or 77.76 MHz clock with a nominal 50% duty cycle. The 77.76 MHz rate is supported for only those faces configured for 777.6 MHz operation. The 155.52 MHz rate is supported for all rates of operation. All REFCLKs must have a common clock source. All REFCLKs must be driven by an active clock regardless whether the associated face is active or not. REFCLK inputs have internal 100-ohm PECL termination and biasing. Requires external 0.01uF AC coupling capacitor. Input signal range between 1200mV and 2000mV pk-pk. differential.
REFCLK2N REFCLK2P	Input	C18 C17	**Reference Clock 2.** The PECL reference clock signals (REFCLK2N/REFCLK2P) provide a clock reference for one of the 4 clock synthesis unit blocks on the device, which in turn generates the transmit serial data clock for links 17-32. REFCLK2 can be either a 155.52 MHz clock or 77.76 MHz clock with a nominal 50% duty cycle. The 77.76 MHz rate is supported for only those faces configured for 777.6 MHz operation. The 155.52 MHz rate is supported for all rates of operation. All REFCLKs must have a common clock source. All REFCLKs must be driven by an active clock regardless whether the associated face is active or not. REFCLK inputs have internal 100-ohm PECL termination and biasing. Requires external 0.01uF AC coupling capacitor. Input signal range between 1200mV and 2000mV pk-pk. differential.

Pin Name	Type	Pin No.	Function
REFCLK3N REFCLK3P	Input	U3 V3	**Reference Clock 3.** The PECL reference clock signals (REFCLK3N/REFCLK3P) provide a clock reference for one of the 4 clock synthesis unit blocks on the device, which in turn generates the transmit serial data clock for links 33-48. REFCLK3 can be either a 155.52 MHz clock or 77.76 MHz clock with a nominal 50% duty cycle. The 77.76 MHz rate is supported for only those faces configured for 777.6 MHz operation. The 155.52 MHz rate is supported for all rates of operation. All REFCLKs must have a common clock source. All REFCLKs must be driven by an active clock regardless whether the associated face is active or not. REFCLK inputs have internal 100-ohm PECL termination and biasing. Requires external 0.01uF AC coupling capacitor. Input signal range between 1200mV and 2000mV pk-pk. differential.
REFCLK4N REFCLK4P	Input	AN17 AP16	**Reference Clock 4.** The PECL reference clock signals (REFCLK4N/REFCLK4P) provide a clock reference for one of the 4 clock synthesis unit block on the device, which in turn generates the transmit serial data clock for links 49-65. REFCLK4 can be either a 155.52 MHz clock or 77.76 MHz clock with a nominal 50% duty cycle. The 77.76 MHz rate is supported for only those faces configured for 777.6 MHz operation. The 155.52 MHz rate is supported for all rates of operation. All REFCLKs must have a common clock source. All REFCLKs must be driven by an active clock regardless whether the associated face is active or not. REFCLK inputs have internal 100-ohm PECL termination and biasing. Requires external 0.01uF AC coupling capacitor. Input signal range between 1200mV and 2000mV pk-pk. differential.
RJ0FP	Input	K6	**Receive Frame Pulse.** The receive frame pulse signal (RJ0FP) provides system timing for the receive serial interface. RJ0FP is supplied in common to all devices in a system containing one or more devices. When register bit R8KCLK in Master Configuration #2 Register 0003H is low (77 MHz frame pulse mode), RJ0FP is treated as a synchronous frame pulse. In this mode, RJ0FP pulses occur exactly every 125 us (9720 SYSCLK cycles) or multiple thereof. Two software configurable delay registers, RJ0DLY_A, and RJ0DLY_B, are used to indicate to the device the delay from the RJ0FP pulse to the time when the J0 section trace byte is present in all the receive FIFOs for the respective timing plane. The device uses this event (RJ0FP plus indicated delay) to align the frames internally, prior to switching. When R8KCLK is high (8 kHz frame pulse mode), RJ0FP is ignored. RJ0FP is sampled on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
TJ0FPA	Output	AJ10	**Transmit Frame Pulse A** The transmit frame pulse signal for timing plane A (TJ0FPA) provides system timing for timing plane A configured transmit links. The TJ0FPA will pulse high to indicate that all J0 signals of a frame should have been transmitted from the timing plane A configured TN/TP signals at the time the pulse occurs. TJ0FPA is a pessimistic signal. It assumes that one of the transmit links in timing plane A is configured for the slowest operation: STS-12 link rate with transmit time switching enabled. TJ0FPA is for diagnostic purposes only and is not intended as a reference for timing. TJ0FPA is an asynchronous output that will pulse high for at least 20ns.
TJ0FPB	Output	K5	**Transmit Frame Pulse B** The transmit frame pulse signal for timing plane B (TJ0FPB) provides system timing for timing plane B configured transmit links. The TJ0FPB will pulse high to indicate that all J0 signals of a frame should have been transmitted from the timing plane B configured TN/TP signals at the time the pulse occurs. TJ0FPB is a pessimistic signal. It assumes that one of the transmit links in timing plane B is configured for the slowest operation: STS-12 link rate with transmit time switching enabled. TJ0FPB is for diagnostic purposes only and is not intended as a reference for timing. TJ0FPB is an asynchronous output that will pulse high for at least 20ns.
RWSEL_A	Input	K7	**Receive Working Select A.** The receive working select A signal (RWSEL_A) selects between working and protect interfaces as the source for any timing plane A ports. The designation of ports as working, protect and line is software controlled. When RWSEL_A is logic 1, then line ports select the working interface as the data source. When RWSEL_A is logic 0, then line ports select the protect interface as the data source. Link sensitivity to RWSEL_A can be disabled using the RWSEL_EN[65:1] bits in the SSWE RWSEL Enable registers. RWSEL_A is essentially an 8 kHz signal. It is sampled on the rising edge of SYSCLK, but only the sample corresponding to the frame pulse position is used. In 77 MHz frame pulse mode (register bit R8KCLK low), only the sample corresponding to the RJ0FP pulse position is used. In 8 kHz frame pulse mode, (register bit R8KCLK high) every SYSCLK rising edge is a frame pulse, so every RWSEL_A sample is used. Refer to RWSEL_A functional timing for an indication of when a change to RWSEL_A takes effect.

Pin Name	Type	Pin No.	Function
RWSEL_B	Input	L8	**Receive Working Select B.** The receive working select B signal (RWSEL_B) selects between working and protect interfaces as the source for any timing plane B ports. The designation of ports as working, protect and line is software controlled. When RWSEL_B is logic 1, then line ports select the working interface as the data source. When RWSEL_B is logic 0, then line ports select the protect interface as the data source. Link sensitivity to RWSEL_B can be disabled using the RWSEL_EN[65:1] bits in the SSWE RWSEL Enable registers. RWSEL_B is essentially an 8 kHz signal. It is sampled on the rising edge of SYSCLK, but only the sample corresponding to the frame pulse position is used. In 77 MHz frame pulse mode (register bit R8KCLK low), only the sample corresponding to the RJ0FP pulse position is used. In 8 kHz frame pulse mode, (register bit R8KCLK high) every SYSCLK rising edge is a frame pulse, so every RWSEL_B sample is used. Refer to RWSEL_B functional timing for an indication of when a change to RWSEL_B takes effect.
CMP_A	Input	H5	**Connection Memory Page Select A.** The transmit connection memory page select signal (CMP_A) controls the selection of the connection memory page for timing plane A configured links. In each timing plane A block with connection memory, CMP_A is XORed with a software configurable page select bit. When the result is high, connection memory page 1 is selected. When the result is low, connection memory page 0 is selected. CMP_A is essentially an 8 kHz signal. It is sampled on the rising edge of SYSCLK, but only the sample corresponding to the frame pulse position is used. In 77 MHz frame pulse mode (register bit R8KCLK low), only the sample corresponding to the RJ0FP pulse position is used. In 8 kHz frame pulse mode, (register bit R8KCLK high) every SYSCLK rising edge is a frame pulse, so every CMP_A sample is used. Refer to CMP_A functional timing for a description of when a change to CMP_A takes effect.
CMP_B	Input	J6	**Connection Memory Page Select B.** The transmit connection memory page select signal (CMP_B) controls the selection of the connection memory page for timing plane B configured links. In each timing plane B block with connection memory, CMP_B is XORed with a software configurable page select bit. When the result is high, connection memory page 1 is selected. When the result is low, connection memory page 0 is selected. CMP_B is essentially an 8 kHz signal. It is sampled on the rising edge of SYSCLK, but only the sample corresponding to the frame pulse position is used. In 77 MHz frame pulse mode (register bit R8KCLK low), only the sample corresponding to the RJ0FP pulse position is used. In 8 kHz frame pulse mode, (register bit R8KCLK high) every SYSCLK rising edge is a frame pulse, so every CMP_B sample is used. Refer to CMP_B functional timing for a description of when a change to CMP_B takes effect.

Pin Name	Type	Pin No.	Function
RSTB	Input	L7	**Reset Enable Bar.** The active low reset signal (RSTB) provides an asynchronous reset for the device. RSTB is a Schmitt triggered input with an integral pull-up resistor.
PRES1 PRES2 PRES3 PRES4		W34 A20 R1 AK19	**Precision Resistor.** A precision resistor 10K Ohm 1% reference resistor is connected between each of these pins and ground. This sets the internal reference current sources.

Pin Name	Type	Pin No.	Function
Microprocessor Interface (37 Signals)			
CSB	Input	AK9	**Chip Select Bar.** The active low chip select signal (CSB) controls microprocessor access to registers in the device. CSB is set low during Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses. If CSB is not required (i.e., register accesses are controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.
RDB	Input	AJ11	**Read Enable Bar.** The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the device. RDB and CSB are set low during Microprocessor Interface Port register read accesses. The device drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	AK10	**Write Enable Bar.** The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the device. WRB and CSB are set low during Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AE30 AD29 AC28 AB27 AC27 AD28 AE29 AF30 AG30 AF29 AE28 AD27 AE27 AF28 AG29 AH30	**Microprocessor Data Bus.** The bi-directional data bus (D[15:0]) is used during Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.

Pin Name	Type	Pin No.	Function
A[15]/TRS A[14] A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	E26 F25 E25 F24 G23 H22 G24 H23 G25 H24 E27 F26 E28 F27 G26 H25	**Microprocessor Address Bus.** The microprocessor address bus (A[15:0]) selects specific Microprocessor Interface Port registers during device register accesses. A[15] is also the Test Register Select (TRS) address pin and selects between normal and test mode register accesses. TRS is set high during test mode register accesses and is set low during normal mode register accesses.
ALE	Input	M7	**Address Latch Enable.** The address latch enable signal (ALE) is active high and latches the address pins (A[15:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the device to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Open Drain Output	N8	**Interrupt Request Bar**. The active low interrupt enable signal (INTB) output goes low when a device interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Pin Name	Type	Pin No.	Function
JTAG Port (5 Signals)			
TCK	Input	G5	**Test Clock.** The JTAG test clock signal (TCK) provides timing for test operations that are carried out using the IEEE P1149.1 test access port. If unused, an external pulldown should be placed on TCK.
TMS	Input	AK7	**Test Mode Select.** The JTAG test mode select signal (TMS) controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	AJ8	**Test Data Input.** The JTAG test data input signal (TDI) carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tri-state	H6	**Test Data Output.** The JTAG test data output signal (TDO) carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when data scanning is in progress.

Pin Name	Type	Pin No.	Function
			JTAG Port (5 Signals)
TRSTB	Input	AK8	**Test Reset Bar.** The active low JTAG test reset signal (TRSTB) provides an asynchronous device, test access port reset, via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. The TAP controller must be placed in the Test-Logic-Reset state after applying power to the device to guarantee correct device operation. This is easily accomplished by connecting TRSTB to the RSTB input and performing a device reset, but is not necessary if another method of resetting the TAP controller is implemented.

Pin Name	Type	Pin No.	Function
			Reserved (17 Signals)
Reserved		AK22 AJ21 AP19 AN18 Y1 W2 W1 V2 A16 B17 A15 B16 R34 T33 T34 U33 J5	**Reserved.** The reserved pins should be left unconnected.

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
VDDA[24:1]	Power	AP17 AJ18 AM18 AM17 AK20 AP18 T5 T2 V1 U1 T1 U2 E19 B19 A17 A18 A19 B18 W30 V33 U34 V34 Y34 W33	The analog power pins (VDDA[24:1]) should be connected to a properly filtered +1.8 V DC supply. These balls require linear voltage regulation and external filtering. Filtering recommendations available in PMC-2011065.
VDDI (247 Balls)	Power	A2 A14 A21 A33 AA1 AA2 AA11 AA12 AA13 AA14 AA16 AA17 AA18 AA19 AA21 AA22 AA23 AA24 AA33 AA34 AB10 AB11 AB14 AB15 AB16 AB19 AB20 AB21 AB24 AB25	The digital/analog core power pins (VDDI) should be connected to a properly-decoupled +1.8 V DC supply. Decoupling recommendations available in PMC-2011065.

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		AC10 AC11 AC12 AC14 AC15 AC20 AC21 AC23 AC24 AC25 AD9 AD12 AD13 AD14 AD21 AD22 AD23 AD26 AE6 AE9 AE10 AE12 AE13 AE22 AE23 AE25 AE26 AF6 AF7 AF10 AF11 AF24 AF25 AG7 AG8 AG11 AG12 AG27 AG28 AH5 AH8 AH9 AH12 AH17 AH18 AH26 AH27 AJ5 AJ6 AJ9 AJ17 AJ25 AJ26 AJ29 AJ30	

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		AK6 AK25 AK28 AK29 AL16 AL19 AM16 AM19 AN1 AN2 AN14 AN21 AN33 AN34 AP2 AP14 AP21 AP33 B1 B2 B14 B21 B33 B34 C16 C19 D16 D19 E6 E9 E10 E29 F5 F6 F8 F9 F17 F18 F29 F30 G8 G11 G12 G16 G17 G27 G30 H7 H8 H10 H11 H27 H28 J10 J24	

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		J25 J28 J29 K9 K10 K12 K13 K22 K23 K25 K26 K29 K30 L12 L13 L14 L21 L22 L23 L26 L27 M10 M11 M12 M14 M15 M20 M21 M23 M24 M25 M27 M28 N10 N11 N14 N15 N16 N19 N20 N21 N24 N25 P1 P2 P11 P12 P13 P14 P16 P17 P18 P19 P21 P22	

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		P23 P24 P33 P34 R12 R13 R16 R19 R22 R23 T3 T4 T13 T14 T15 T16 T19 T20 T21 T22 T31 T32 U6 U14 U21 U28 U29 V6 V7 V14 V21 V29 W3 W4 W5 W13 W14 W15 W16 W19 W20 W21 W22 W31 W32 Y5 Y12 Y13 Y16 Y19 Y22 Y23	
VDDO (232 Balls)	Power	A8 A27	The digital I/O power pins (VDDO) should be connected to a properly-decoupled +3.3 V DC supply. Decoupling

Pin Name	Type	Pin No.	Function
			Power (503 Balls)
		AA7 AA8 AA10 AA25 AA27 AA28 AB5 AB8 AB9 AB17 AB18 AB26 AB30 AC5 AC6 AC9 AC16 AC17 AC18 AC19 AC26 AC29 AC30 AD6 AD7 AD15 AD16 AD19 AD20 AE3 AE4 AE5 AE7 AE8 AE14 AE15 AE16 AE19 AE20 AE21 AE31 AE32 AF5 AF12 AF13 AF16 AF17 AF18 AF19 AF22 AF23 AG1 AG2 AG13 AG14	recommendations available in PMC-2011065.

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		AG17 AG18 AG21 AG22 AG25 AG33 AG34 AH14 AH15 AH20 AH21 AH24 AH25 AJ12 AJ15 AJ16 AJ19 AJ20 AJ23 AJ24 AK12 AK13 AK16 AK23 AL3 AL4 AL10 AL25 AL31 AL32 AM4 AM10 AM25 AM31 AN8 AN27 AP8 AP27 B8 B27 C4 C10 C25 C31 D3 D4 D10 D25 D31 D32 E12 E13 E16 E22 E23	

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		F11 F12 F15 F16 F19 F20 F23 G14 G15 G20 G21 H1 H2 H14 H17 H18 H21 H33 H34 J13 J14 J16 J17 J18 J19 J22 J23 K3 K4 K8 K14 K15 K16 K19 K20 K21 K31 K32 L6 L15 L16 L19 L20 L28 L29 M5 M6 M16 M17 M18 M19 M26 M29 M30 N5	

Pin Name	Type	Pin No.	Function
Power (503 Balls)			
		N9 N17 N18 N26 N27 N30 P7 P8 P10 P25 P27 P28 R6 R7 R10 R11 R24 R25 R28 R29 T6 T9 T10 T11 T12 T23 T24 T25 T26 T29 T30 U8 U9 U12 U13 U22 U23 U26 U27 V8 V9 V12 V13 V22 V23 V26 V27 W6 W9 W10 W11 W12 W23 W24 W25	

Pin Name	Type	Pin No.	Function
		Power (503 Balls)	
		W26 W29 Y6 Y7 Y10 Y11 Y24 Y25 Y28 Y29	

Pin Name	Type	Pin No.	Function
		Ground (309 Balls)	
VSS	Ground	A7 A13 A22 A28 AA5 AA6 AA9 AA15 AA20 AA26 AA29 AA30 AB1 AB6 AB7 AB12 AB13 AB22 AB23 AB28 AB29 AB34 AC7 AC8 AC13 AC22 AD4 AD5 AD8 AD10 AD11 AD17 AD18 AD24 AD25 AD30 AD31 AE11 AE17	The ground pins (VSS) should be connected to GND.

Pin Name	Type	Pin No.	Function
		AE18 AE24 AF2 AF3 AF8 AF9 AF14 AF15 AF20 AF21 AF26 AF27 AF32 AF33 AG5 AG6 AG9 AG10 AG15 AG16 AG19 AG20 AG23 AG24 AG26 AH1 AH6 AH7 AH10 AH11 AH13 AH16 AH19 AH22 AH23 AH28 AH29 AH34 AJ7 AJ13 AJ14 AJ22 AJ27 AJ28 AK4 AK5 AK11 AK14 AK15 AK17 AK18 AK21 AK24 AK26 AK27 AK30	

Pin Name	Type	Pin No.	Function
		AK31 AL5 AL11 AL17 AL18 AL24 AL30 AM2 AM3 AM9 AM15 AM20 AM26 AM32 AM33 AN3 AN9 AN15 AN20 AN26 AN32 AP7 AP13 AP22 AP28 B3 B9 B15 B20 B26 B32 C2 C3 C9 C15 C20 C26 C32 C33 D5 D11 D17 D18 D24 D30 E4 E5 E7 E8 E11 E14 E15 E17 E18 E20 E21	

Pin Name	Type	Pin No.	Function
		E24 E30 E31 F7 F10 F13 F14 F21 F22 F28 G1 G6 G7 G9 G10 G13 G18 G19 G22 G28 G29 G34 H9 H12 H13 H15 H16 H19 H20 H26 H29 H30 J2 J3 J7 J8 J9 J11 J12 J15 J20 J21 J26 J27 J30 J32 J33 K11 K17 K18 K24 K27 K28 L4 L5 L9	

Pin Name	Type	Pin No.	Function
		L10 L11 L17 L18 L24 L25 L30 L31 M9 M13 M22 N1 N6 N7 N12 N13 N22 N23 N28 N29 N34 P5 P6 P9 P15 P20 P26 P29 P30 R2 R3 R5 R8 R9 R14 R15 R17 R18 R20 R21 R26 R27 R30 R32 R33 T7 T8 T17 T18 T27 T28 U4 U5 U7 U10 U11	

Pin Name	Type	Pin No.	Function
		U15 U16 U17 U18 U19 U20 U24 U25 U30 U31 V4 V5 V10 V11 V15 V16 V17 V18 V19 V20 V24 V25 V28 V30 V31 W7 W8 W17 W18 W27 W28 Y2 Y3 Y8 Y9 Y14 Y15 Y17 Y18 Y20 Y21 Y26 Y27 Y30 Y32 Y33	
TOTAL = 1152			

Notes on Pin Descriptions

1. All device inputs and bi-directionals except the ELVDS inputs present minimum capacitive loading and operate at TTL logic levels.
2. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
3. All outputs except the ELVDS links have 8mA drive capability – this includes TDO, INTB and D[15:0]).

4. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
5. It is mandatory that every power pin (VDDA,VDDO & VDDI) be connected to the appropriate printed circuit board power plane to ensure reliable device operation.
6. All VDDA pins (analog power) can be sensitive to noise. They must be isolated from the VDDO, VDDI, and VSS. Care must be taken to correctly decouple these pins. Please refer to the Operation sections.
7. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.
8. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operation section.
9. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
10. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

9 Functional Description

The switching function can be divided into two timing planes, A and B, each of which has a separate independent transport frame alignment. Receive and transmit links are independently designated to one of the timing planes through the RGRPASEL and TGRPASEL register bits in Master Configuration Registers #3 and #4 respectively. For example, receive link 1 does not necessarily belong to the same timing plane as transmit link 1. Transmit links designated to timing plane A can only source data from receive links in timing plane A. Transmit links designated to timing plane B can only source data from receive links in timing plane B.

The device has 2 different core clock rate modes, determined by the maximum link rate. One core rate has switches based on 12 timeslots. The other core rate switches are based on 48 timeslots. If the maximum link rate is STS-12, then the core is limited to 12 timeslot switching. Otherwise the device switches based on 48 timeslots. The core clock rate mode is set using the CTSS[1:0] bits in Master Configuration Register #2.

The RTSI and TTSI blocks serve to bridge between the link rate and the core rate. In the case of a receive STS-12 link rate and a 48 timeslot core clock rate, the received timeslot data 1,2,3,. . .,12 is mapped to RTSI input timeslots 1,5,9 . . .45 respectively. This has the consequence that in setting up the RTSI connection memory for STS-12 links with an STS-48 core, the user must access only timeslots 1,5,9 . . . 45. This mapping is not done for SONET byte interleaving. It is done because in this case a slow stream is written into a fast pipe (4x as fast), so only every fourth byte is written.

In the case of STS-48 link rate and a 48 timeslot core, the received data 1,2,3,…,48 are mapped to timeslots 1,2,3,…,48 respectively.

9.1 Serial TelecomBus

The links on the device can be configured for either serial TelecomBus or scrambled operation. Table 2 provides the correspondence of 8B/10B control characters to their meaning in the Serial TelecomBus Protocol. Note that different disparities of some control characters are used for different TelecomBus conditions. In these cases disparity violations are allowed with respect to the 8B/10B spec.

From Table 2, there are three levels of TelecomBus encoding: MST, HPT, and LPT. If data is received and transmitted on a serial TelecomBus configured link, all levels of serial TelecomBus encoding are supported, and serial TelecomBus characters are preserved.

If data is received on a serial TelecomBus configured links and transmitted on a scrambled link, the mapped value for the control character is represented in Table 2 as the unencoded value. In this case it is recommended that only MST level encoding is used. Note that MST encoding will not be preserved in a cross connect mixing serial TelecomBus and scrambled links. If the High Order Path AIS condition is indicated (encoded as K28.4-) on a STS-1 coming into the cross connect on 777 links, that encoding is lost on scrambled links. That STS-1 would carry encoded FFh data (replacing the K28.4- characters) on the 777 link exiting the cross connect.

If data is received on a scrambled link and transmitted on a serial TelecomBus link, no special characters with the exception of the K28.5 (J0) and K28.4- (High Order Path AIS) special characters will be seen on the transmit data. For the Receive Scrambled and Transmit Serial TelecomBus case, the user must enable J0 insertion in the TSEC blocks on those serial TelecomBus transmit links for the framers on the receiving device.

Table 2 Serial TelecomBus Control Characters

Code Group Name	Signal Description	Encoded Value	Unencoded Value	Disparity Violation Allowed
Multiplex Section Termination (MST) Mode				
K28.5	Transport J0 frame alignment	001111 1010 110000 0101	0000 0001	No
K.28.4-	High-order path AIS	001111 0010	1111 1111	Yes
High Order Path (HPT) Mode				
K28.0-	High-order path H3 byte, no negative justification event	001111 0100	Undefined	Yes
K28.0+	High-order path PSO byte, positive justification event	110000 1011	Undefined	Yes
K28.6	High-order path J1 frame alignment	001111 0110 110000 1001	Undefined	No
Low Order Path Termination (LPT) Mode				
K27.7-	Low order path frame alignment #1: IV5 = 1 and ID[5,0,4] = ‘b000 ERDI[1:0] = ‘b00, REI = ‘b0, ERDI[1:0] and REI are encoded in the V5 byte.	110110 1000	Undefined	Yes
K27.7+	Low order path frame alignment #2: IV5 = 1 and ID[5,0,4] = ‘b100 ERDI[1:0] = ‘b00, REI = ‘b1, ERDI[1:0] and REI are encoded in the V5 byte.	001001 0111	Undefined	Yes
K28.7-	Low order path frame alignment #3: ERDI[1:0] = ‘b01, REI = ‘b0, ERDI[1:0] and REI are encoded in the V5 byte, ID[5,0,4]=’b001	001111 1000	Undefined	Yes
K28.7+	Low order path frame alignment #4: IV5 = 1 and ID[5,0,4] = ‘b101 ERDI[1:0] = ‘b01, REI = ‘b1, ERDI[1:0] and REI are encoded in the V5 byte.	110000 0111	Undefined	Yes
K29.7-	Low order path frame alignment #5: IV5 = 1 and ID[5,0,4] = ‘b010 ERDI[1:0] = ‘b01, REI = ‘b1, ERDI[1:0] and REI are encoded in the V5 byte.	101110 1000	Undefined	Yes
K29.7+	Low order path frame alignment #6: IV5 = 1 and ID[5,0,4] = ‘b110 ERDI[1:0] = ‘b10, REI = ‘b1, ERDI[1:0] and REI are encoded in the V5 byte.	010001 0111	Undefined	Yes

Code Group Name	Signal Description	Encoded Value	Unencoded Value	Disparity Violation Allowed
K30.7-	Low order path frame alignment #7: IV5 = 1 and ID[5,0,4] = 'b011 ERDI[1:0] = 'b11, REI = 'b0, ERDI[1:0] and REI are encoded in the V5 byte.	011110 1000	Undefined	Yes
K30.7+	Low order path frame alignment #8: IV5 = 1 and ID[5,0,4] = 'b111 ERDI[1:0] = 'b11, REI = 'b1, ERDI[1:0] and REI are encoded in the V5 byte.	100001 0111	Undefined	Yes
K23.7	Non low-order path payload overhead bytes (RSOH, MSOH, POH, R, V1, V2, V3, V4)	111010 1000 000101 0111	Undefined	No
K.28.4+	Low-order path AIS	110000 1101	Undefined	Yes

9.2 Clock Synthesis Unit (CSU) and Clock Synthesis Unit Interface (CSUI)

The clock synthesis unit uses a PLL to synthesize a baud clock from the clock reference inputs. The baud clock is used to transmit serial data on all channels. No external components are required by the PLL other than a precision resistor on the precision resistor terminals. The baud clock frequency may be varied over a range of .622 GHz to 2.488 GHz. The PLL has three fixed multiplication ratios of 4, 5, and 16, to accommodate the supported baud rates of 0.622, 0.7776, and 2.488 Gbit/s respectively from a REFCLK frequency of 155.52 MHz. The PLL can also be configured for a baud rate of 0.7776 Gbit/s from a REFCLK frequency of 77.76 MHz. A clock output is provided for operating the internal logic of the device. A total of 4 CSUs blocks are instantiated in the device, one for each face.

The clock synthesis unit interface (CSUI) provides a microprocessor interface to set control and access status information for the CSU. It also provides additional per face control for the PISOs, DRUs, TXLVs, and RXLVs on the corresponding face. The CSUI also generates a core clock with a rate dependent on the core time slot mode. Four CSUIs are instantiated on the device, one for each CSU.

9.3 Serializer (PISO)

The Parallel Data In, Serial Data Out (PISO) is an analog block that serializes the output DataStream prior to its transmission by the TXLV block. The PISO accepts 8 or 10-bit characters and converts them to a serial bit stream at the selected baud rate.

The PISO has three modes: 10-bit, Scrambled NRZ, and Half Rate mode. 10-bit and Scrambled NRZ modes are mutually exclusive.

In 10-Bit Mode, the PISO divides the transmit serial clock generated from the CSU by 10, uses the divided clock to clock in 10 bit parallel data, and outputs the serial data at transmit serial clock rate. 10-Bit mode PISO configuration supports the links configured for 777.6 Gbit/s Serial TelecomBus operation.

In Scrambled NRZ mode, the PISO divides the transmit serial clock generated from the CSU by 8, uses the divided clock to clock in 8 bit parallel data and outputs the serial data at transmit serial clock rate. Scrambled NRZ mode PISO configuration supports the links configured for 622 Mbit/s and 2.488 Gbit/s operation.

In Half Rate mode, the PISO accepts half the bits of the designated word width, and outputs each bit twice at the transmit serial clock. This mode can be used in conjunction with 10-Bit mode or Scrambled NRZ mode. Half Rate mode PISO configuration supports the links configured for either 622 or 777.6 Mbit/s operation.

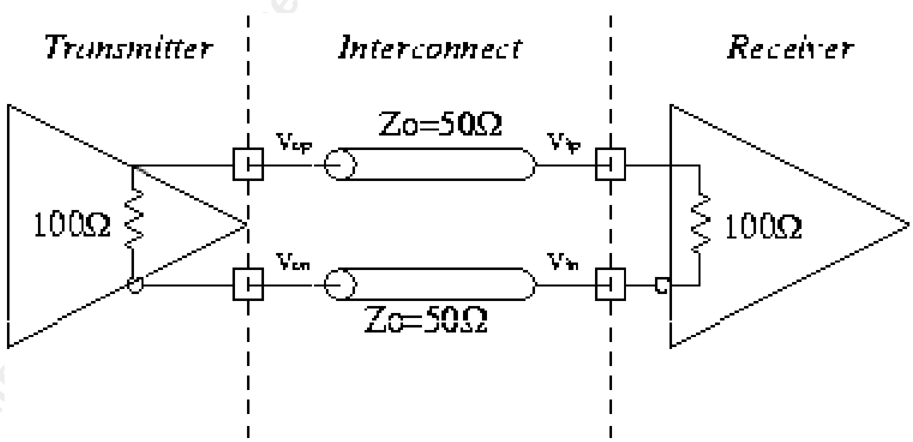
A total of 65 PISO blocks are instantiated in the device.

9.4 High Speed Receiver (RXLV)

The RXLV block is a 2.488 Gbit/s Enhanced Low Voltage Differential Signaling (ELVDS) receiver according to the PMC ELVDS Electrical Specification. Together with the TXLV, the RXLV block forms a complete 2.488 Gbit/s point-to-point ELVDS link.

A generic ELVDS link is illustrated below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines.

Figure 7 Generic ELVDS Link Block Diagram



9.5 High Speed Output Driver (TXLV)

High speed output data is driven differentially by the TXLV block, and may directly drive optical, cable, or pc-board interconnects. The High Speed 2.488 ELVDS line driver (TXLV) is designed to transmit data at a maximum rate of 2.488 Gbit/s over controlled impedance lines (50 ohms). The TXLV is capable of transmitting up to 2.488 Gbit/s over 40” of FR4. It provides both differential outputs and an on-chip differential termination (100 ohms differential).

For backplanes implemented with FR4 or similar materials, significant dielectric losses will occur. These losses are frequency dependent and severely limit the achievable separation between transmitter and receiver. To mitigate this problem, the device offers optional output pre-emphasis. The pre-emphasis circuit drives the output more strongly when the data sequence contains high-frequency information.. Signal characteristics should be verified for each system to determine which mode should be used. Pre-emphasis mode is intended for 2.488 Gbit/s links only. Use on 777.6 Mbit/s or 622 Mbit/s links is not supported.

Also included is a low-swing mode, which saves power by reducing the amplitude on the TN/TP outputs for shorter reach applications.

Pre-emphasis and low-swing operation are mutually exclusive.

A total of 65 TXLV blocks are instantiated in the device.

9.6 Clock and Data Recovery Unit (DRU)

The Clock and Data Recovery Unit (DRU) is an analog block that recovers clock and data from a serial data stream, deserializes the data, and outputs the parallel data with a synchronized low speed clock.

A baud-rate receive clock is extracted from the transition rich serial data stream independently on each channel. The data rate of the transmitted serial bit stream must be frequency locked to the REFCLK clock signals. Transitions in the data are used to steer sampling towards the center of the eye.

The DRU has three modes: 10-bit, Scrambled NRZ, and Half Rate mode. 10-bit and Scrambled NRZ modes are mutually exclusive.

In 10-Bit mode, the DRU converts the serial data to a 10-bit word and outputs the parallel data at $1/10^{th}$ of the serial data rate with the synchronized clock. 10-Bit mode DRU configuration supports the links configured for 777.6 Mbit/s Serial TelecomBus operation.

In Scrambled NRZ mode, the DRU expects a “Scrambled NRZ” serial data stream. In Scrambled NRZ mode the DRU will convert the serial data to an 8-bit word and outputs the parallel data at $1/8^{th}$ of the serial data rate with the synchronized clock. Scrambled NRZ mode DRU configuration supports the links configured for 622 Mbit/s and 2.488 Gbit/s operation.

In Half Rate mode, the DRU recovers serial data stream at half rate of the CSU provided clocks. This mode can be used in conjunction with 10-Bit Mode or Scrambled NRZ Mode. Half Rate mode DRU configuration supports the links configured for either 622 or 777.6 Mbit/s operation.

A total of 65 DRU blocks are instantiated in the device.

9.7 Receive SONET Data Framer (RSEF)

The RSEF block performs character alignment and frame alignment on an unaligned SONET/SDH data stream received from the DRU block.

The RSEF block recovers character and frame alignment in two modes: Serial TelecomBus encoded data, and scrambled data. Serial TelecomBus encoding is based on 8B/10B encoding except that it permits the emission of specific incorrect disparity control characters that would normally result in a line code violation at the 8B/10B receiver. The exceptional control characters (and disparities) are as follows: K28.0-, K28.0+, K28.4-, K28.4+, K27.7-, K27.7+, K28.7-, K28.7+, K29.7-, K29.7+, K30.7-, K30.7+.

In Serial TelecomBus mode, the RSEF recovers character alignment by searching for the 8B/10B K28.5 frame alignment control character, which is used to identify the J0 position of the SONET/SDH frame. When the RSEF is out of character alignment, it is also necessarily out of frame alignment. When the RSEF is out of character alignment, the first K28.5 character found will determine the character alignment and transition the RSEF into the character alignment state. A count of line code violations (LCVs), either unrecognized 8B/10B characters or incorrect disparity characters, is maintained. If the number of LCVs within a window of 15 received characters exceeds a threshold of 4, frame and character alignment is lost and the block attempts to reframe on the next J0 character. To find frame alignment, the RSEF must locate two K28.5 characters at the correct position with respect to each other, separated by 9720 bytes, regardless of whether the RSEF is currently character aligned or not. If the RSEF goes out of character alignment while the RSEF is attempting to frame align, the RSEF will not frame align even if the well separated K28.5 character condition is satisfied. To go out of frame, the RSEF must either go out of character alignment or encounter four instances of K28.5 characters not in the J0 position of the current frame alignment and uninterrupted by an instance of a J0 being in the correct position.

Additionally, in this mode, the 8B/10B DataStream is decoded into an internal format of 8-bits data and 1-bit control.

In scrambled mode, the RSEF block performs character and frame alignment on the incoming scrambled DataStream based on the SONET/SDH A1/A2 framing pattern. The RSEF achieves character alignment on detecting a pattern of 3 A1 characters followed by 3 A2 characters. If frame alignment is not found in the next frame, character alignment is lost. Frame alignment is attained when the RSEF is character aligned, and it detects an A1 character at the first A1 timeslot and the first 4 bits of the A2 character at the last A2 timeslot, based on the alignment predicted by the character aligner. A minimum of three and a maximum of four consecutive errors in detecting the A1/A2 pattern above will result in loss of frame and character alignment. Following framing, the DataStream is descrambled. The resultant stream is mapped into 8 bits data, and 1 bit control to achieve uniformity of output data with the RSEFs receiving Serial TelecomBus.

Character and frame alignment state can be monitored through the MPIF. Additionally, software can force the RSEF out of either character and/or frame alignment.

The RSEF also performs block-based bit interleaved parity (BIP-8) checking on the B1 byte in the SONET/SDH frame following the character and frame alignment functions. An interrupt indication and B1 error count allow monitoring of the B1 status. B1 errors are counted and interrupts generated regardless of character/frame alignment state. The B1 error count is only valid for unencoded data.

The RSEF provides control for the input replication feature. Except for the 65th channel, all Receive channels are paired such that an odd channel is paired with the next even channel. If input port replication is enabled for an even RSEF, it selects the odd channel in the pair as its data source. If input port replication is enabled for an odd RSEF, it selects the even channel in the pair as its data source. If input port replication is not enabled, the RSEF selects its own channel as its data source. Input port replication is enabled on a per channel basis using the Register MN04H RSEF Control #3 SWAP_INPUTB bits. For applications of this feature see Section 12.8.

The RSEF provides control to mask K28.5 characters in the DataStream. These characters are seen in Serial TelecomBus data streams. If they are not masked, then the time slot interchange blocks have to be configured to prevent J0/Z0 reordering. Masking K28.5 characters at the RSEF and reinserting them at the J0 position for TSECs configured for Serial TelecomBus allows J0/Z0 switching.

The RSEF also provides control for line code violation propagation on Serial TelecomBus Receive data streams. If line code violation propagation is enabled, a special character is inserted into the DataStream which is mapped to a line code violation by Serial TelecomBus configured TSECs. Otherwise line code violations are mapped to 0FH.

A total of 65 RSEF blocks are instantiated in the device.

9.8 Receive Time Slot Interchange (RTSI)

The RTSI accepts SONET/SDH frame aligned cyclic groups of STS-1 samples from the associated RSEF and outputs these samples in an arbitrary time permutation to the space switch stage. The time permutation is determined by the contents of a microprocessor accessible control table. The control table is composed of two sets of switch settings, or pages, each of which describes which STS-1 sample should be output during the i^{th} STS-1 time slot. The pages are dynamically designated as standby or active, controllable by the CMP_A and CMP_B pins. The designation of the RTSI to timing plane A or B is achieved with the Master Configuration #3 Register 0004H RGRPASEL[15:0] and Master Configuration #2 Register 0003H RTPGRPASEL register bits. The standby page is available for modification via the microprocessor interface. The active page provides the current switch settings.

The RTSI uses a FIFO to bridge between the receive data clock domain and the core clock domain. The FIFO also enables the RTSI to frame align its output data to the output data from the other multiple receive ports in its timing plane.

The RTSI has a mode in which no timeslot interchange is performed and latency through the data path is minimized. Time slot interchange in the RTSI on a data stream introduces an additional 154 ns delay on the data stream.

A total of 65 RTSI blocks are instantiated in the device.

9.9 Space Switch Element (SSWE)

The SSWE accepts fully aligned SONET/SDH streams from 65 RTSIs. The space stage implements a space switch for each STS-1 sample in the data stream and delivers the STS-1 samples to the 65 Transmit Time Slot Interchange Blocks.

The SSWE is equivalent to a crossbar, with switch settings taken from a control table for each output port for each timeslot. Each SSWE control table is composed from two pages of control. At a given time, one page is designated as active and the other page is designated as standby. The active page is used to control the MUXes in the crossbar while the standby page is available for update though the microprocessor interface. The CMP_A and CMP_B pins control the dynamic standby/active designation of the control register pages. Each page has a switch setting for each timeslot of the DataStream. The designation of an SSWE output port to timing plane A or B is achieved with the Master Configuration #5 Register 0005H TGRPASEL and Master Configuration #2 Register 0003H TTPGRPASEL register bits.

Receive working/protect selection is supported on both timing groups using the RWSEL_A and RWSEL_B pins for line outputs. This allows switching between working and protect traffic without performing a page switch. The timing plane A working ports on the system side interface are selected as the source for transmit data on the timing plane A line ports when RWSEL_A is logic 1. The timing plane A protection ports on the system side interface are selected as the source for transmit data on the timing plane A line ports when RWSEL_A is logic 0. Function of RWSEL_B is similar to RWSEL_A except that it applies to timing plane B ports.

There is an independent receive working select enable for all line ports in the SSWE RWSEL Enable registers. Working ports are designated through the connection memory settings. The protect ports are simply a software configurable fixed offset from the working ports. Refer to the SSWE RWSEL Configuration Register 0065H WPMASK[4:2] bits description for more rules on locating working and protect ports and controlling the fixed offset between them. Control of the port offset between Receive Working/Protect is software enabled on a per-output basis.

One SSWE block is instantiated in the device.

9.10 Transmit Time Slot Interchange (TTSI)

The TTSI accepts SONET/SDH frame aligned cyclic groups of STS-1 samples from the SSWE and outputs these samples in an arbitrary time permutation to the associated output links. The time permutation is determined by the contents of a microprocessor accessible control table. The control table is composed of two sets of switch settings or pages, each of which describes which STS-1 sample should be output during the i^{th} STS-1 time slot. The pages are dynamically designated as standby or active, controllable by the CMP_A and CMP_B pins. The standby page is available for modification via the microprocessor interface. The active page provides the current switch settings. The designation of the TTSI to timing plane A or B is achieved with the Master Configuration #5 Register 0005H TGRPASEL and Master Configuration #2 Register 0003H TTPGRPASEL register bits.

The TTSI also provide the facility for per STS-1 monitoring and insertion of a 24 bit connection identifier (CID) in Z2 across multiple frames. CID insertion and monitoring are done following time slot interchange. Six bits of the CID are available for insertion, while 18 bits are available for insertion and monitoring. Two pages of CID settings allow switchover of the Z2 monitor/insert settings simultaneous to connection memory switchover. CID settings are stored with the TTSI connection memory. A CID capture function permits capturing the CID from a selected stream. Note that when CID insertion is enabled, CID insertion has higher priority than AIS insertion. CID insertion overwrites the Z2/M1 byte positions

The TTSI provides control for the transmit channel multiplexing feature where data from two TTSIs is multiplexed into a single DataStream. The transmit channels are grouped into pairs, an odd channel and the next even channel. The multiplexed data is transmitted on the odd channel. If transmit channel multiplexing is enabled, using the even channel Register MN23H: TTSI Interrupt Enable #1 SLAVE bit, the odd channel TTSI channel selection bits control the transmit channel mux with STS-1 granularity. For applications of this feature see Section 12.8.

The TTSI uses a FIFO to bridge between the core data clock time domain and the transmit clock time domain. The TTSI has a mode in which no timeslot interchange is performed and latency through the data path is minimized. Time slot interchange introduces an additional 154 ns delay on the data.

A total of 65 TTSI blocks are instantiated in the device.

9.11 Transmit SONET/SDH Data Scrambler/ 8B/10B Encoder (TSEC)

The TSEC block converts the internal data representation to the selected external serial transmission format. If configured for emission of scrambled data, the TSEC applies SONET/SDH scrambling to the DataStream. Alternately, the TSEC can be configured for the emission of a Serial TelecomBus DataStream in which the DataStream is encoded using the 8B/10B based Serial TelecomBus format.

Serial TelecomBus differs from 8B/10B in that it permits the emission of specific incorrect disparity control characters that would normally result in a line code violation at the 8B/10B receiver. The exceptional control characters (and disparities) are as follows: K28.0-, K28.0+, K28.4-, K28.4+, K27.7-, K27.7+, K28.7-, K28.7+, K29.7-, K29.7+, K30.7-, K30.7+.

The TSEC can be configured to overwrite the DataStream with a pseudo random bit sequence (PRBS) onto the SONET/SDH frames. The PRBSed bytes exclude the path overhead and fixed stuff bytes of the SPE. The TSEC supports PRBS generation of concatenated SONET/SDH streams at the line rate: STS-12c, or STS-48c. The STS-Nc SPE payload is fixed inside the transport frame with the J1 following the H3 bytes (active offset of 0). The PRBS polynomial used is $x^{23}+x^{18}+1$.

The TSEC provides a per channel control for pre-emphasis of the transmit differential signal with the MN32H: Port #1 - #65 TSEC Enable Control PREEMPH_EN bits.

A total of 65 TSEC blocks are instantiated in the device.

9.12 Pointer Interpreter and PRBS Monitor

The Pointer Interpreter and PRBS Monitor (PIPM) contain a simplified pointer interpreter that identifies the J1 position in the concatenated SONET/SDH payloads and follows pointer justification events. A frame pulse indicates the start of the SPE to the PRBS monitor. The PIPM also provides PRBS monitoring for concatenated SONET/SDH payloads. The PIPM can be configured to determine J1 position using the Serial TelecomBus pointer position control characters (K28.0-, K28.0+, and K28.6). This mode can only be used when the data was Serial TelecomBus encoded at the High-order Path Termination (HPT) level. Pointer interpreter mode is selected using the Register MN40H: PIPM Configuration and Status MON_MODE bit.

The PIPM pointer interpreter does not implement the full specification for SONET/SDH pointer processing. Particularly, error conditions (AIS, LOP) are ignored, since the PIPM pointer interpreter assumes that the frames containing PRBS will be correctly formatted. The fundamental operations (new pointer value during normal operation, new data flag, increment and decrement) are fully implemented according to ANSI T1.105-1995.

The PIPM supports PRBS monitoring of the concatenated SONET/SDH streams STS-Nc payload capacity at the line rates: STS-12c/C-4-4c, STS-48c/C-4-16c. The STS-Nc SPE/VC-4-Xc payload is floating inside the transport frame, so the PIPM must identify the J1 position in order to locate the STS-Nc payload capacity/C-4-Xc.

The incoming PRBS data is tested against the $X^{23} + X^{18} + 1$ polynomial. The PRBS data is optionally inverted before being checked.

The PRBS monitoring process consists of two steps. First, the monitor LFSR is synchronized with the incoming PRBS data. Second, the LFSR is used to generate subsequent expected PRBS words and to compare them with the incoming PRBS words. If the expected and received words are not equal, then a mismatch error is detected in that word. Mismatch errors are counted while the monitor is synchronized with the incoming stream. Mismatch errors optionally result in the generation of an interrupt. The monitor mismatch error counter does not count bit errors since multiple bit errors in a byte will be considered as a single byte error. Four consecutive byte errors will force the monitor out of synchronization. The current synchronization state is available through the microprocessor interface. A change in the synchronization state will also generate an interrupt.

Synchronization begins by loading the LFSR with consecutive bits from the incoming PRBS pattern. This requires three bytes of data. One byte is ignored. If the next 4 bytes generated by the LFSR after it is loaded match the incoming bytes, then the monitor is considered synchronized. If a mismatch occurs, then the monitor remains unsynchronized and continues to attempt to synchronize by repeating this process with the next bytes in the DataStream. Given the unpredictability of the state of the PRBS monitor, PRBS monitor synchronization is not guaranteed for less than 12 consecutive correct PRBS bytes, although it is possible for synchronization to occur on greater than 7 consecutive correct PRBS bytes.

The PIPM will not synchronize to the input PRBS data if the data is a sequence of either all 0 bits or all 1 bits The monitor will check specifically for this case and will not synchronize to it.

9.13 JTAG

The device provides standard 5 signal IEEE 1149.1 JTAG support for testing device interconnection on a PC board. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The TBS 9953 identification code is 153070CD hexadecimal.

9.14 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the device to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the device. The register set is accessed as shown in the Register Memory Map table below. Addresses that are not shown are not used and must be treated as Reserved.

The ports are organized into 65 Port Sets. A Port Register Set is specified for each Port Set. Registers for Port Register Set 1 are specified in the register memory map starting at base address 0x100. For the remaining Port Register Sets, only the range of registers is specified. As with Port Register Set 1, not all addresses within a range correspond to actual registers. To obtain a corresponding register for port set N+1, take the base register address for Port Register Set N and add 0x100. This means the base address of Port Register Set N is:

$$0x100 * N :: 1 \leq N \leq 65$$

Let *MN* denote the hexadecimal representation of the register set number. The address in hexadecimal for the registers at a common offset from a port base address is denoted as:

$$0xMN00 :: 0x01 \leq MN \leq 0x41$$

The grouping of the Receive and Transmit ELVDS ports to a port register set is defined as follows: Port Register Set N controls blocks associated with receive ELVDS links RP[N]/RN[N]. This includes RXLV, DRU, and RSEF blocks N, and RTSI block N. Port Register Set N also controls blocks associated with transmit ELVDS links TP[N]/TN[N]. This includes TTSI block N, TSEC, PISO, and TXLV block N.

Table 3 Register Memory Map

Address	Register
0000	Master Reset
0001	Master Clock Activity and Accumulation Trigger
0002	Master Configuration #1
0003	Master Configuration #2
0004	Master Configuration #3
0005	Master Configuration #4
0006	Master Power Control
0007	Master Frame Pulse Delay A

Address	Register
0008	Master Frame Pulse Delay B
0009	Master Interrupt Enable
000A	Master Interrupt Block Identifier
000B	Master JTAG ID High
000C	Master JTAG ID Low
000D	Master User Defined
000E	Master RSEF Interrupt Source #1
000F	Master RSEF Interrupt Source #2
0010	Master RSEF Interrupt Source #3
0011	Master RSEF Interrupt Source #4
0012	Master PIPM Interrupt Source #1
0013	Master PIPM Interrupt Source #2
0014	Master PIPM Interrupt Source #3
0015	Master PIPM Interrupt Source #4
0016	Master RTSI Interrupt Source #1
0017	Master RTSI Interrupt Source #2
0018	Master RTSI Interrupt Source #3
0019	Master RTSI Interrupt Source #4
001A	Master TTSI Interrupt Source #1
001B	Master TTSI Interrupt Source #2
001C	Master TTSI Interrupt Source #3
001D	Master TTSI Interrupt Source #4
001E	Master Test Port and CSUI Interrupt Source
001F-002F	Reserved
0030	CSUI #1 Interrupt Enable and CSU Lock Status
0031	CSUI #1 Interrupt Status
0032	CSUI #1 Feedback Divider
0033	CSUI #1 Control
0034	CSUI #1 AC Coupling Control
0035	Reserved
0036	Face #1 Configuration
0037	Reserved
0038	CSUI #2 Interrupt Enable and CSU Lock Status
0039	CSUI #2 Interrupt Status
003A	CSUI #2 Feedback Divider
003B	CSUI #2 Control
003C	CSUI #2 AC Coupling Control
003D	Reserved
003E	Face #2 Configuration

Address	Register
003F	Reserved
0040	CSUI #3 Interrupt Enable and CSU Lock Status
0041	CSUI #3 Interrupt Status
0042	CSUI #3 Feedback Divider
0043	CSUI #3 Control
0044	CSUI #3 AC Coupling Control
0045	Reserved
0046	Face #3 Configuration
0047	Reserved
0048	CSUI #4 Interrupt Enable and CSU Lock Status
0049	CSUI #4 Interrupt Status
004A	CSUI #4 Feedback Divider
004B	CSUI #4 Control
004C	CSUI #4 AC Coupling Control
004D	Reserved
004E	Face #4 Configuration
004F-005F	Reserved
0060	SSWE Indirect Access Configuration
0061	SSWE Indirect Access Data 1
0062	SSWE Indirect Access Data 2
0063	SSWE Configuration
0064	SSWE Interrupt Status
0065	SSWE RWSEL Configuration
0066	SSWE RWSEL Enable #1
0067	SSWE RWSEL Enable #2
0068	SSWE RWSEL Enable #3
0069	SSWE RWSEL Enable #4
006A – 00FF	Reserved
0100-01FF	**Port Register Set 1**
0100	Port Register Set 1: RSEF Control and Status
0101	Port Register Set 1: RSEF Interrupt Status and Clock Monitor
0102	Port Register Set 1: RSEF LCV and BIP8 Error Count
0103	Port Register Set 1: RSEF Control #2
0104	Port Register Set 1: RSEF Control #3
0105 – 010F	Port Register Set 1: Reserved
0110	Port Register Set 1: RTSI Indirect Access Configuration
0111	Port Register Set 1: RTSI Indirect Access Data
0112	Port Register Set 1: RTSI Configuration
0113	Port Register Set 1: RTSI Interrupt Status

Address	Register
0114 – 011F	Port Register Set 1: Reserved
0120	TTSI Indirect Access Configuration
0121	TTSI Indirect Access Data #1
0122	TTSI Indirect Access Data #2
0123	TTSI Interrupt Enable #1
0124	TTSI Interrupt Enable #2
0125	TTSI Interrupt Enable #3
0126	TTSI Interrupt Enable #4
0127	TTSI Interrupt Status #1
0128	TTSI Interrupt Status #2
0129	TTSI Interrupt Status #3
012A	TTSI Interrupt Status #4
012B	TTSI Connection ID Capture Register #1
012C	TTSI Connection ID Capture Register #2
012D	TTSI Connection ID Capture Register #3
012E – 012F	Port Register Set 1: Reserved
0130	Port Register Set 1: TSEC Control and Status
0131	Port Register Set 1: TSEC Test Pattern
0132	Port Register Set 1: TSEC Enable Control
0133 – 013F	Port Register Set 1: Reserved
0140	Port Register Set 1: PIPM Configuration and Status
0141	Port Register Set 1: PIPM Interrupt Status
0142	Port Register Set 1: PIPM Error Count
0143-01FF	Port Register Set 1: Reserved
0200 – 02FF	**Port Register Set 2**
0300 – 03FF	**Port Register Set 3**
0400 – 04FF	**Port Register Set 4**
0500 – 05FF	**Port Register Set 5**
0600 – 06FF	**Port Register Set 6**
0700 – 07FF	**Port Register Set 7**
0800 – 0FFF	**Port Register Set 8 – 15**
1000 – 3FFF	**Port Register Set 16 – 63**
4000 – 40FF	**Port Register Set 64**
4100 – 41FF	**Port Register Set 65**
8000	Master Test
8001	Master Test Mode Address Force Enable
8002	Master Test Mode Address Force Value
8003	TM0 and Scan

Address	Register
8004 – FFFF	Reserved for Test

Notes on Register Memory Map

1. For all register accesses, CSB must be set low.
2. Addresses that are not shown must be treated as Reserved.
3. A[15] is the test register select (TRS) and should be set to logic 0 for normal mode register access.
4. See Table 20 for the Test Mode Register Memory Map

10 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the device. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[15]) is low.

Notes on Normal Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the device to determine the programming state of the device.

3. Writeable normal mode register bits are set to their default value upon reset as indicated in the Default column of each register bit definition table.

4. A readable normal mode register bit with a default value of X indicates uncertainty in that bits value during the operation of the device. This can include interrupt indication bits, TIP bits, BUSY bits, and self clearing bits.

5. Writing into read-only normal mode register bit locations does not affect device operation unless otherwise noted.

6. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the device operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

7. Register addresses described as MNXXH are defined for 01H<=MN<=41H.

Register: 0000H Master Reset

Bit	Type	Function	Default
Bit 15	R/W	DRESET	0
Bit 14	R/W	ARESET	0
Bit 13	R/W	DBLOCK_RESET	0
Bit 12	R/W	FACE_RESET[4]	0
Bit 11	R/W	FACE_RESET[3]	0
Bit 10	R/W	FACE_RESET[2]	0
Bit 9	R/W	FACE_RESET[1]	0
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register allows separate software reset of digital and analog circuitry on the device.

FACE_RESET[4:1]

The face reset bits (FACE_RESET[4:1]) allow face groups of RSEF, PIPM, RTSI, and TTSI blocks to be reset under software control. When FACE_RESET is high all RSEF, PIPM, RTSI, TTSI, and TSEC blocks associated with the face will be held in reset and all register bits associated with those blocks will be set to their default value.

These bits are not self-clearing. Therefore, a logic 0 must be written to bring the face out of reset. A hardware reset clears the FACE_RESET[4:1] bits, thus negating the digital software reset.

Table 4 Face Reset Port Association

FACE	FACE_RESET Bit	Receive and Transmit Links
1	FACE_RESET[1]	1 to 16
2	FACE_RESET[2]	17 to 32
3	FACE_RESET[3]	33 to 48
4	FACE_RESET[4]	49 to 65

DBLOCK_RESET

The digital block reset bit (DBLOCK_RESET) allows all digital logic except for the CSUI blocks and the master registers to be reset under software control. If DBLOCK_RESET is high, all digital logic is held in reset and all register bits will be set to the default value except for the master registers (registers 000H-001EH inclusive) and the following CSUI registers:

0030H, 00038H, 0040H, 0048H CSUI #1 – #4 Interrupt Enable and CSU Lock Status

0031H, 0039H, 0041H, 0049H CSUI #1 - #4 Interrupt Status

0032H, 003AH, 0042H, 004AH CSUI #1 - #4 Feedback Divider

0033H, 003BH, 0043H, 004BH CSUI #1 - #4 Control

0034H, 003CH, 0044H, 004CH CSUI #1 - #4 AC Coupling Control

This bit is not self-clearing. Therefore, a logic 0 must be written to bring the digital blocks out of reset. A hardware reset clears the DBLOCK_RESET bit, thus negating the digital block software reset.

ARESET

The ARESET bit allows the analog circuitry in the device to be reset under software control. If the ARESET bit is a logic 1, all the analog circuitry is held in reset. ARESET must be held at logic 1 for at least 100us to ensure correct reset of the CSU. Note the CSU should not need to be reset under ordinary conditions. The CSU is automatically reset when a lock detection circuit discovers the CSU is not locked on the reference clock.

This bit is not self-clearing. Therefore, a logic 0 must be written to bring the device out of reset. A hardware reset clears the ARESET bit, thus negating the analog software reset.

DRESET

The DRESET bit allows the digital circuitry in the device, including all registers except for bits in Register 000H: Master Reset, to be reset under software control. If the DRESET bit is a logic 1, all the device digital circuitry is held in reset.

This bit is not self-clearing. Therefore, a logic 0 must be written to bring the device out of reset. A hardware reset clears the DRESET bit, thus negating the digital software reset.

Register: 0001H Master Clock Activity and Accumulation Trigger

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	RJ0FPAEA	X
Bit 2	R	RJ0FPA	X
Bit 1	R	TIP	X
Bit 0	R	SYSCLKA	X

This register provides activity monitoring on the SYSCLK input. Writing to this register also initiates a transfer of counts from the performance monitor accumulation registers to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent saturation of counters, accumulation intervals should be regular. The bits in this register are not affected by write accesses.

SYSCLKA

The SYSCLK active (SYSCLKA) bit monitors for low to high transitions on the SYSCLK clock input. SYSCLKA is set high on a rising edge of SYSCLK and is set low when this register is read. When the corresponding bit register reads low, this indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

TIP

The Transfer in Progress (TIP) initiates and monitors the state of RSEF LCV/BIP8 error count, and PIPM error count performance meter register transfers. Writing any value to this register initiates a device-wide accumulation interval transfer and loads all the performance meter registers in the device. TIP is set to logic 1 while the transfer is in progress and is set to a logic 0 when the transfer is complete.

If individual performance meter register transfers are initiated (by writing directly to the individual register), TIP will monitor the state of those transfers as well. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Note: The bit may be stuck high following reset. Initiating a normal performance meter register transfer, by writing to Register 0001H Master Clock Activity and Accumulation Trigger will result in the bit being cleared.

RJ0FPA

The Frame Pulse active (RJ0FPA) bit monitors for low to high transitions on the sampled RJ0FP input. RJ0FPA is set high on a rising edge of the sampled RJ0FP input and is set low when this register is read. When the corresponding bit register reads low, this indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions. RJ0FP is sampled on rising edge of SYSCLK.

RJ0FPAEA

The Frame Pulse alignment event activity bit (RJ0FPAEA) bit monitors for loss of alignment on the frame pulse. The frame pulse is provided either though the RJ0FP (in 77 MHz frame pulse mode) or the SYSCLK (in 8 kHz frame pulse mode). In either mode, the frame pulse is position is expected to occur every 125.0 us (or multiple thereof) and the event results in a check of the internal frame counter. If the frame counter is within a safe range when the frame pulse occurs, the frame counter is not disturbed. If the frame pulse occurs outside the safe range of the frame counter , then the frame counter is realigned and RJ0FPAEA is set to logic 1. RJ0FPAEA is set low when this register is read. When the CORE_FP_CENTER bit is logic 1, the internal counter is aligned every frame pulse regardless of distance from the reference position. In this case RJ0FPAEA will only be set when the internal counter alignment changes the counter value from the predicted value.

Note that the reference point for checking frame pulse position is the internal frame counter, and this is set by the last frame pulse that resulted in a counter realignment – and caused RJ0FPAEA to be set. Successor frame pulses are expected at within a small delta from a multiple of 125.0 us from that initial frame pulse. Specification of this delta depends on the frame pulse mode , 8 kHz frame pulse mode, or 77.76 MHz frame pulse mode.

In 8 kHz frame pulse mode the rising edge of SYSCLK provides the frame pulse. RJ0FPAEA will not be asserted if difference between the frame pulse and the ideal position is less than 51 ns. RJ0FPAEA will be asserted if the difference between the frame pulse and the ideal position is greater than 64 ns. RJ0FPAEA may be asserted if the difference between the frame pulse and the ideal position is between 51 ns and 64 ns

In 77.76 MHz frame pulse mode the RJ0FP pulse provides the frame pulse. RJ0FPAEA will not be asserted if difference between the frame pulse and the ideal position is less than 4 SYSCLK cycles. RJ0FPAEA will be asserted if the difference between the frame pulse and the ideal position is greater than 5 SYSCLK cycles. RJ0FPAEA may be asserted if the difference between the frame pulse and the ideal position is between 4-5 SYSCLK cycles.

Register: 0002H Master Configuration #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	STSLR4[1]	0
Bit 10	R/W	STSLR4[0]	0
Bit 9	R/W	STSLR3[1]	0
Bit 8	R/W	STSLR3[0]	0
Bit 7	R/W	Reserved [3]	0
Bit 6	R/W	Reserved [2]	0
Bit 5	R/W	Reserved [1]	0
Bit 4	R/W	Reserved [0]	0
Bit 3	R/W	SCREN[4]	0
Bit 2	R/W	SCREN[3]	0
Bit 1	R/W	SCREN[2]	0
Bit 0	R/W	SCREN[1]	0

The Reserved [3:0] bits should be written to their default value for correct operation of the device.

This register controls the data format used in the device on a per-face basis.

SCREN[4:1]

The scrambler/descrambler enable bits (SCREN[4:1]) control the scrambling function for the ports on a per-face basis. SCREN[1] controls face 1 (links 1-16). SCREN[2] controls face 2 (links 17-32). SCREN[3] controls face 3 (links 33-48). SCREN[4] controls face 4 (links 49-65). When SCREN[*n*] is high, scrambling/descrambling is enabled for the corresponding face. When SCREN[*n*] is low, scrambling/descrambling is disabled for the corresponding face. A SCREN[*n*] bit must be high when the corresponding face is configured for STS-12 (622 Mbit/s) or STS-48. A SCREN[*n*] bit must be low when the corresponding face is configured for STS-12 (777.6 Mbit/s) operation.

STSLR3[1:0]

The STS link rate bits for face 3 (STSLR3[1:0]) configures the link data format and rate for the 16 links (links 33-48) on face 3. Table 5 indicates the correspondence between STSLR bits, data format and data rate.

STSLR4[1:0]

The STS link rate bits for face 4 (STSLR4[1:0]) configures the link data format and rate for the 17 links (links 49-65) on face 4. Table 5 indicates the correspondence between STSLR bits, data format and data rate.

Table 5 STSLR*n* Data Format

STSLR*n*[1:0]	Line Data Rate	Line Data Rate (Gbit/s)
00	STS-12	.777 or .622
01	STS-48	2.488
1x	Reserved	N/A

Register: 0003H Master Configuration #2

Bit	Type	Function	Default
Bit 15	R/W	CTSS[1]	0
Bit 14	R/W	CTSS[0]	0
Bit 13	R/W	CORE_FP_CENTER	0
Bit 12	R/W	Reserved[1]	0
Bit 11	R/W	Reserved[0]	0
Bit 10	R/W	WCIMODE	0
Bit 9	R/W	R8KCLK	0
Bit 8	R/W	CORE_SRC[1]	0
Bit 7	R/W	CORE_SRC[0]	0
Bit 6	—	Unused	X
Bit 5	R/W	TPASSTHRU_B	0
Bit 4	R/W	RPASSTHRU_B	0
Bit 3	R/W	TPASSTHRU_A	0
Bit 2	R/W	RPASSTHRU_A	0
Bit 1	R/W	RTPGRPASEL	0
Bit 0	R/W	TTPGRPASEL	0

The Reserved [1:0] bits should be written to their default value for correct operation of the device.

This register configures the test port time plane designation, core clock source, core timeslots and the time switch block configuration in the device.

TTPGRPASEL

The transmit test port group A select bit (TTPGRPASEL) associates the transmit test port to a timing plane. More specifically, TTPGRPASEL specifies which frame alignment delay register (RJ0DLY_A or RJ0DLY_B) is associated with the transmit test port channel (TN[65]/TP[65]). If TTPGRPASEL is logic 1, the transmit test port channel and the TTSI block on that channel belongs to timing plane A and is frame aligned to RJ0DLY_A, and TTSI/SSWE test port page switching is controlled by CMP_A. If the TTPGRPASEL bit is logic 0, the transmit test port channel belongs to timing plane B and is frame aligned to RJ0DLY_B, and the TTSI/SSWE test port page switching is controlled by CMP_B. All receive links with data selected by the transmit test output port must have the same receive group setting as the transmit test port.

RTPGRPASEL

The receive test port group A select bit (RTPGRPASEL) associates the receive test port to a timing plane. More specifically, RTPGRPASEL specifies which frame alignment delay register (RJ0DLY_A or RJ0DLY_B) is associated with the receive test port channel (RN[65]/RP[65]). If RTPGRPASEL is logic 1, the receive test port channel, specifically the RTSI block on that channel, belongs to timing plane A, is frame aligned to RJ0DLY_A, and its page switching is controlled by CMP_A. If RTPGRPASEL is logic 0, the receive test port channel, specifically the RTSI block on that channel, belongs to timing plane B, is frame aligned to RJ0DLY_B, and its page switching is controlled by CMP_B. All transmit links that select data from the receive test port must have the same group setting as the receive test port.

RPASSTHRU_A

The time plane A receive time switch pass-through mode bit (RPASSTHRU_A) allows traffic on time plane A to avoid the ingress time slot interchange. When RPASSTHRU_A is logic 1, the RTSIs in time plane A perform no switching (allowing minimal delay through the those blocks). When RPASSTHRU_A is low, the RTSIs in time plane A perform switching as configured by the user in the connection memory. The RTSI time plane assignment is configured by the RTPGRPASEL and RGRPASEL register bits.

TPASSTHRU_A

The time plane A transmit time switch pass-through mode bit (TPASSTHRU_A) allows traffic on time plane A to avoid the transmit time slot interchange. When TPASSTHRU_A is logic 1, the TTSIs in time plane A perform no switching (allowing minimal delay through the those blocks). When TPASSTHRU_A is low, the TTSIs in time plane A perform switching as configured by the user in the connection memory. The TTSI time plane assignment is configured by the TTPGRPASEL and TGRPASEL register bits.

RPASSTHRU_B

The time plane B receive time switch pass-through mode bit (RPASSTHRU_B) allows traffic on time plane B to avoid the ingress time slot interchange. When RPASSTHRU_B is logic 1, the RTSIs in time plane B perform no switching (allowing minimal delay through the those blocks). When RPASSTHRU_B is low, the RTSIs in time plane B perform switching as configured by the user in the connection memory. The RTSI time plane assignment is configured by the RTPGRPASEL and RGRPASEL register bits.

TPASSTHRU_B

The time plane B transmit time switch pass-through mode bit (TPASSTHRU_B) allows traffic on time plane B to avoid the transmit time slot interchange. When TPASSTHRU_B is logic 1, the TTSIs in time plane B perform no switching (allowing minimal delay through the those blocks). When TPASSTHRU_B is low, the TTSIs in time plane B perform switching as configured by the user in the connection memory. The TTSI time plane assignment is configured by the TTPGRPASEL and TGRPASEL register bits.

CORE_SRC[1:0]

The core clock source bits (CORE_SRC[1:0]) select the REFCLK used to provide the clock to the core logic. Table 6 shows the correspondence between CORE_SRC and the REFCLK selected. CORE_SRC must select the highest rate REFCLK connected to the device on an active face. It is possible, although unlikely, to have different rate REFCLKs driving the faces of the device (some 77.76 MHz, some 155.52 MHz). If all REFCLKs are the same rate, the REFCLK selected is arbitrary. Selecting the REFCLK on a disabled face is not valid during regular device operation, though is not an issue for startup configuration.

Table 6 Core Clock Source Selection

CORE_SRC[1:0]	Core Clock Source REFCLK
00	REFCLK1N/P
01	REFCLK2N/P
10	REFCLK3N/P
11	REFCLK4N/P

R8KCLK

The receive 8 kHz clock bit (R8KCLK) controls whether RJ0FP or SYSCLK signals are used as the frame pulse. When R8KCLK is high, SYSCLK is treated as an 8kHz clock and used as the frame pulse. When R8KCLK is low, RJ0FP is treated as a synchronous frame pulse and is sampled on the rising edge of SYSCLK.

WCIMODE

The write-clear-interrupt mode bit (WCIMODE) controls whether interrupt status bits are cleared on a read or a write to the corresponding register. If WCIMODE is logic 1, all interrupt status bits in the interrupt status register are cleared when logic 1 is written to the corresponding interrupt bit. Otherwise, interrupt status bits are cleared on a register read. WCIMODE is a static bit., it should be set to the appropriate value during configuration and not changed during device operation. Changing WCIMODE during device operation can result in the incorrect assertion of interrupt indication bits.

CORE_FP_CENTER

The core frame pulse center bit sets the internal frame alignment counter to the received frame pulse position either RJ0FP, or SYSCLK in 8kHz mode. This bit should be set to logic 1 following any device reset (FACE_RESET, ARESET, DRESET, RSTB pin) and then reset to logic 0 before proper operation can occur. To have an effect, CORE_FP_CENTER must be set when the system frame pulse occurs. It should not be cleared until an RJ0FP pulse occurs, in 77MHz frame pulse mode, or until a SYSCLK edge occurs, in 8khz frame pulse mode.

CTSS[1:0]

The core timeslot select bits (CTSS[1:0]) select the core timeslot mode of the device. The setting of these bits depends on the setting of the STSLR*n*[1:0] bits. If all faces are configured for STS-12 operation, then CTSS must be set to “00” for 12 core timeslots.

Table 7 CTSS, STSLR*n* Correspondence

CTSS[1:0]	Core Timeslot Mode	Legal Values of STSLR*n*[1:0]
00	12	00
01	48	00, 01
1x	N/A	Reserved

Register: 0004 Master Configuration #3

Bit	Type	Function	Default
Bit 15	R/W	RGRPASEL [15]	0
Bit 14	R/W	RGRPASEL [14]	0
Bit 13	R/W	RGRPASEL [13]	0
Bit 12	R/W	RGRPASEL [12]	0
Bit 11	R/W	RGRPASEL [11]	0
Bit 10	R/W	RGRPASEL [10]	0
Bit 9	R/W	RGRPASEL [9]	0
Bit 8	R/W	RGRPASEL [8]	0
Bit 7	R/W	RGRPASEL [7]	0
Bit 6	R/W	RGRPASEL [6]	0
Bit 5	R/W	RGRPASEL [5]	0
Bit 4	R/W	RGRPASEL [4]	0
Bit 3	R/W	RGRPASEL [3]	0
Bit 2	R/W	RGRPASEL [2]	0
Bit 1	R/W	RGRPASEL [1]	0
Bit 0	R/W	RGRPASEL [0]	0

This register configures receive port time plane designation.

RGRPASEL[15:0]

The receive group A select bits (RGRPASEL[15:0]) specify the timing plane association for the receive channels. Timing plane A receive channels will synchronize to the frame alignment register, RJ0DLY_A, and use the CMP_A and RWSEL_A pins. Timing plane B receive channels will synchronize to the frame alignment register, RJ0DLY_B, and use the CMP_B and RWSEL_B pins. If RGRPASEL[*n*] is logic 1, the corresponding 4 receive channels, specifically the RTSI blocks on those channels, are associated with timing plane A. If the RGRPASEL bit{*n*] is logic 0, the corresponding 4 receive channels are associated with timing plane B. Each bit of RGRPASEL[*n*] controls 4 input links as specified in Table 8. All receive links with data selected by a common transmit link must have the same RGRPASEL setting, which must be the same as the TGRPASEL of that transmit link.

Table 8 Synchronization Select Port Association

RGRPASEL Bit	Receive Links
RGRPASEL[0]	1 to 4
RGRPASEL[1]	5 to 8
…	…
RGRPASEL[*n*]	(*n**4+1) to (*n**1+4)
…	…
RGRPASEL[15]	61 to 64

Register: 0005 Master Configuration #4

Bit	Type	Function	Default
Bit 15	R/W	TGRPASEL [15]	0
Bit 14	R/W	TGRPASEL [14]	0
Bit 13	R/W	TGRPASEL [13]	0
Bit 12	R/W	TGRPASEL [12]	0
Bit 11	R/W	TGRPASEL [11]	0
Bit 10	R/W	TGRPASEL [10]	0
Bit 9	R/W	TGRPASEL [9]	0
Bit 8	R/W	TGRPASEL [8]	0
Bit 7	R/W	TGRPASEL [7]	0
Bit 6	R/W	TGRPASEL [6]	0
Bit 5	R/W	TGRPASEL [5]	0
Bit 4	R/W	TGRPASEL [4]	0
Bit 3	R/W	TGRPASEL [3]	0
Bit 2	R/W	TGRPASEL [2]	0
Bit 1	R/W	TGRPASEL [1]	0
Bit 0	R/W	TGRPASEL [0]	0

This register configures transmit port time plane designation.

TGRPASEL[15:0]

The transmit group A select bits (TGRPASEL[15:0]) specify the timing plane association for the transmit channels. Timing plane A transmit channels will synchronize to the frame alignment register, RJ0DLY_A, and use the CMP_A and RWSEL_A pins. Timing plane B transmit channels will synchronize to the frame alignment register, RJ0DLY_B, and use the CMP_B and RWSEL_B pins. If TGRPASEL[*n*] is logic 1, the corresponding 4 transmit channels, specifically the TTSI blocks and SSWE ports on those channels are associated with timing plane A. If the TGRPASEL bit{*n*] is logic 0, the corresponding 4 transmit channels are associated with timing plane B. Each bit of TGRPASEL[*n*] controls 4 input links as specified in Table 8. All receive links with data selected by a common transmit link must have the same RGRPASEL setting, which must be the same as the TGRPASEL of that transmit link.

Table 9 Synchronization Select Port Association

TGRPASEL Bit	Transmit Links
TGRPASEL[0]	1 to 4
TGRPASEL[1]	5 to 8
…	…
TGRPASEL[*n*]	(*n**4+1) to (*n**1+4)
…	…
TGRPASEL[15]	61 TO 64

Register: 0006H Master Power Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	POWERDOWN[4]	1
Bit 2	R/W	POWERDOWN[3]	1
Bit 1	R/W	POWERDOWN[2]	1
Bit 0	R/W	POWERDOWN[1]	1

This register provides power saving features for applications that do not utilize the entire device.

POWERDOWN[4:1]

The POWERDOWN[4:1] bits must be set to “0000” following power up or reset of the device, where the device reset is either through the RSTB pin or the DRESET bit. This is essential for proper operation of the device. A power down function is no longer supported with these bits. For instructions on minimizing the power consumption for a face please refer to section 12.5. To minimize power consumption caused by enabling all faces, apply the face low power mode settings contained in Table 25 in the indicated order before clearing this bit.

Register: 0007H Master Frame Pulse Delay A

Bit	Type	Function	Default
Bit 15	R/W	RJ0DLY_A[15]	0
Bit 14	R/W	RJ0DLY_A[14]	0
Bit 13	R/W	RJ0DLY_A[13]	0
Bit 12	R/W	RJ0DLY_A[12]	0
Bit 11	R/W	RJ0DLY_A[11]	0
Bit 10	R/W	RJ0DLY_A[10]	0
Bit 9	R/W	RJ0DLY_A[9]	0
Bit 8	R/W	RJ0DLY_A[8]	0
Bit 7	R/W	RJ0DLY_A[7]	0
Bit 6	R/W	RJ0DLY_A[6]	0
Bit 5	R/W	RJ0DLY_A[5]	0
Bit 4	R/W	RJ0DLY_A[4]	0
Bit 3	R/W	RJ0DLY_A[3]	0
Bit 2	R/W	RJ0DLY_A[2]	0
Bit 1	R/W	RJ0DLY_A[1]	0
Bit 0	R/W	RJ0DLY_A[0]	1

This register communicates to the device the delay between the arrival of RJ0FP and the actual reception of the J0 character in the relevant RTSI for blocks.

RJ0DLY_A[15:0]

The receive J0 frame pulse delay A bits (RJ0DLY_A[15:0]) represent the delay in terms of internal clock cycles between the RJ0FP frame pulse signal being sampled high and the J0 character being sampled from the timing plane A RTSI FIFOs. The internal clock cycle period varies with the CTSS value and is given in Table 10. RJ0DLY_A is set such that after the specified delay, all active receive links would have delivered the J0 character. RJ0DLY_A has a valid range between 1 to 19,440 inclusive when the core is operating in 48 timeslot mode (CTSS is “01"). RJ0DLY_A has a valid range between 1 to 4,860 inclusive when the core is operating in 12 timeslot mode (CTSS is “00"). Determining an appropriate value for RJ0DLY_A depends on frame pulse position relative to the data, and the system configuration, and is described in Section 13, Functional Timing.

Note: change to RJ0DLY_A in an operational system will result in loss of data.

Table 10 Core Clock Period

Core Timeslot Mode	Clock Period (ns)
12	25.72016
48	6.43004

Register: 0008H Master Frame Pulse Delay B

Bit	Type	Function	Default
Bit 15	R/W	RJ0DLY_B[15]	0
Bit 14	R/W	RJ0DLY_B[14]	0
Bit 13	R/W	RJ0DLY_B[13]	0
Bit 12	R/W	RJ0DLY_B[12]	0
Bit 11	R/W	RJ0DLY_B[11]	0
Bit 10	R/W	RJ0DLY_B[10]	0
Bit 9	R/W	RJ0DLY_B[9]	0
Bit 8	R/W	RJ0DLY_B[8]	0
Bit 7	R/W	RJ0DLY_B[7]	0
Bit 6	R/W	RJ0DLY_B[6]	0
Bit 5	R/W	RJ0DLY_B[5]	0
Bit 4	R/W	RJ0DLY_B[4]	0
Bit 3	R/W	RJ0DLY_B[3]	0
Bit 2	R/W	RJ0DLY_B[2]	0
Bit 1	R/W	RJ0DLY_B[1]	0
Bit 0	R/W	RJ0DLY_B[0]	1

This register communicates to the device the delay between the arrival of RJ0FP and the actual reception of the J0 character in the relevant RTSI for blocks.

RJ0DLY_B[15:0]

The receive J0 frame pulse delay B bits (RJ0DLY_B[15:0]) represent the delay in terms of internal clock cycles between the RJ0FP frame pulse signal being sampled high and the J0 character being sampled from the timing plane B RTSI FIFOs. The internal clock cycle period varies with the CTSS value and is given in Table 10. RJ0DLY_B is set such that after the specified delay, all active receive links would have delivered the J0 character. RJ0DLY_B has a valid range between 1 to 19,440 inclusive when the core is operating in 48 timeslot mode (CTSS is “01"). RJ0DLY_B has a valid range between 1 to 4,860 inclusive when the core is operating in 12 timeslot mode (CTSS is “00”). Determining an appropriate value for RJ0DLY_B depends on frame pulse position relative to the data, and the system configuration, and is described in Section 13, Functional Timing. Note, change to RJ0DLY_B in an operational system will result in loss of data.

Register: 0009H Master Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	CSUIE	0
Bit 4	R/W	SSWEE	0
Bit 3	R/W	TTSIE	0
Bit 2	R/W	RTSIE	0
Bit 1	R/W	PIPME	0
Bit 0	R/W	RSEFE	0

This register allows the source of an active interrupt to contribute to the device INTB pin (on a per-block type basis).

RSEFE

The RSEF Master Interrupt Enable bit (RSEFE), when high, allows INTB to be driven low when an interrupt request is active from one of the 65 Receive Scrambled 8B/10B Encoded Framer (RSEF) blocks (any condition in which ID_RSEFI is high). When RSEFE is low, ID_RSEFI will have no effect on the INTB pin.

PIPME

The PIPM Master Interrupt Enable bit (PIPME), when high, allows INTB to be driven low when an interrupt request is active from one of the 65 Pointer Interpreter and PRBS Monitor (PIPM) blocks (any condition in which ID_PIPMI is high). When PIPME is low, ID_PIPMI will have no effect on the INTB pin.

RTSIE

The RTSI Master Interrupt Enable bit (RTSIE), when high, allows INTB to be driven low when an interrupt request is active from one of the 65 Receive Time Slot Interchange (RTSI) blocks (any condition in which ID_RTSII is high). When RTSIE is low, ID_RTSII will have no effect on the INTB pin.

TTSIE

The TTSI Master Interrupt Enable bit (TTSIE), when high, allows INTB to be driven low when an interrupt request is active from one of the 65 Transmit Time Slot Interchange (TTSI) blocks (any condition in which ID_TTSII is high). When TTSIE is low, ID_TTSII will have no effect on the INTB pin.

SSWEE

The SSWE Master Interrupt Enable bit (SSWEE), when high, allows INTB to be driven low when an interrupt request is active from the Space Switch Element (SSWE) block (any condition in which ID_SSWEI is high). When SSWEE is low, ID_SSWEI will have no effect on the INTB pin.

CSUIE

The CSUI Master Interrupt Enable bit (CSUII), when high, allows INTB to be driven low when an interrupt request is active from one of the 4 CSUI blocks (any condition in which ID_CSUII is high). When CSUIE is low, ID_CSUII will have no effect on the INTB pin.

Register: 000AH Master Interrupt Block Identifier

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	ID_CSUII	X
Bit 4	R	ID_SSWEI	X
Bit 3	R	ID_TTSII	X
Bit 2	R	ID_RTSII	X
Bit 1	R	ID_PIPMI	X
Bit 0	R	ID_RSEFI	X

The Reserved bit should be written to its default value for correct operation of the device.

This register allows the source of an active interrupt to be identified down to the block function level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

ID_RSEFI

The ID_RSEFI bit is high when an interrupt request is active from one of the 65 Receive Scrambled 8B/10B Encoded Framer (RSEF) blocks. The particular RSEF block that set the interrupt can be identified by reading the RSEF Interrupt Source registers. The ID_RSEFI bit is cleared when the interrupt is cleared.

ID_PIPMI

The ID_PIPMI bit is high when an interrupt request is active from one of the 65 Pointer Interpreter and PRBS Monitor (PIPM) blocks. The particular PIPM block that set the interrupt can be identified by reading the PIPM Interrupt Source registers. The ID_PIPMI bit is cleared when the interrupt is cleared.

ID_RTSII

The ID_RTSII bit is high when an interrupt request is active from one of the 65 Receive Time Slot Interchange (RTSI) blocks. The particular RTSI block that set the interrupt can be identified by reading the RTSI Interrupt Source registers. The ID_RTSII bit is cleared when the interrupt is cleared.

ID_TTSII

The ID_TTSII bit is high when an interrupt request is active from one of the 65 Transmit Time Slot Interchange (TTSI) blocks. The particular TTSI block that set the interrupt can be identified by reading the TTSI Interrupt Source registers. The ID_TTSII bit is cleared when the interrupt is cleared.

ID_SSWEI

The ID_SSWEI bit is high when an interrupt request is active from the Space Switch Element (SSWE) block. The ID_SSWEI bit is cleared when the interrupt is cleared.

ID_CSUII

The ID_CSUII bit is high when an interrupt request is active from one of the CSUI blocks and indicates a change in the lock status of a CSU. The particular CSUI block that set the interrupt can be identified by reading the CSUI Interrupt Source registers. The ID_CSUII bit is cleared when the interrupt is cleared.

Register: 000BH Master JTAG ID High

Bit	Type	Function	Default
Bit 15	R	ID[3]	0
Bit 14	R	ID[2]	0
Bit 13	R	ID[1]	0
Bit 12	R	ID[0]	1
Bit 11	R	DEVID[15]	0
Bit 10	R	DEVID[14]	1
Bit 9	R	DEVID[13]	0
Bit 8	R	DEVID[12]	1
Bit 7	R	DEVID[11]	0
Bit 6	R	DEVID[10]	0
Bit 5	R	DEVID[9]	1
Bit 4	R	DEVID[8]	1
Bit 3	R	DEVID[7]	0
Bit 2	R	DEVID[6]	0
Bit 1	R	DEVID[5]	0
Bit 0	R	DEVID[4]	0

The Master JTAG ID registers hold the JTAG identification code for the device. The device revision number and device identification are available through these registers.

DEVID[15:0]

The DEVID bits can be read to distinguish the TBS 9953 from other devices. DEVID returns 5307H when read.

ID[3:0]

The ID bits can be read to provide a binary TBS 9953 revision number.

Register: 000CH Master JTAG ID Low

Bit	Type	Function	Default
Bit 15	R	DEVID[3]	0
Bit 14	R	DEVID[2]	1
Bit 13	R	DEVID[1]	1
Bit 12	R	DEVID[0]	1
Bit 11	R	MID[10]	0
Bit 10	R	MID[9]	0
Bit 9	R	MID[8]	0
Bit 8	R	MID[7]	0
Bit 7	R	MID[6]	1
Bit 6	R	MID[5]	1
Bit 5	R	MID[4]	0
Bit 4	R	MID[3]	0
Bit 3	R	MID[2]	1
Bit 2	R	MID[1]	1
Bit 1	R	MID[0]	0
Bit 0	R	JID	1

JID

The JID bit is bit 0 in the JTAG identification code.

MID[10:0]

The MID bits provide the manufacturer identity field in the JTAG identification code. MID returns 066H when read.

DEVID[15:0]

The DEVID bits can be read to distinguish the TBS 9953 from other devices. DEVID returns 5307H when read.

Register: 000DH Master User Defined

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	FREE[7]	X
Bit 6	R/W	FREE[6]	X
Bit 5	R/W	FREE[5]	X
Bit 4	R/W	FREE[4]	X
Bit 3	R/W	FREE[3]	X
Bit 2	R/W	FREE[2]	X
Bit 1	R/W	FREE[1]	X
Bit 0	R/W	FREE[0]	X

FREE[7:0]

The FREE[7:0] register bits do not perform any function. They are free for user defined read/write operations. The FREE bits cannot be reset.

Register: 000EH Master RSEF Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	RSEFI[16]	X
Bit 14	R	RSEFI[15]	X
Bit 13	R	RSEFI[14]	X
Bit 12	R	RSEFI[13]	X
Bit 11	R	RSEFI[12]	X
Bit 10	R	RSEFI[11]	X
Bit 9	R	RSEFI[10]	X
Bit 8	R	RSEFI[9]	X
Bit 7	R	RSEFI[8]	X
Bit 6	R	RSEFI[7]	X
Bit 5	R	RSEFI[6]	X
Bit 4	R	RSEFI[5]	X
Bit 3	R	RSEFI[4]	X
Bit 2	R	RSEFI[3]	X
Bit 1	R	RSEFI[2]	X
Bit 0	R	RSEFI[1]	X

This register is used to indicate interrupts generated from the RSEF blocks #1 through #16.

RSEFI[16:1]

The RSEF #*X* interrupt event indication (RSEFI[X]) transitions to logic 1 when a hardware interrupt event is sourced from RSEF #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 000FH Master RSEF Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	RSEFI[32]	X
Bit 14	R	RSEFI[31]	X
Bit 13	R	RSEFI[30]	X
Bit 12	R	RSEFI[29]	X
Bit 11	R	RSEFI[28]	X
Bit 10	R	RSEFI[27]	X
Bit 9	R	RSEFI[26]	X
Bit 8	R	RSEFI[25]	X
Bit 7	R	RSEFI[24]	X
Bit 6	R	RSEFI[23]	X
Bit 5	R	RSEFI[22]	X
Bit 4	R	RSEFI[21]	X
Bit 3	R	RSEFI[20]	X
Bit 2	R	RSEFI[19]	X
Bit 1	R	RSEFI[18]	X
Bit 0	R	RSEFI[17]	X

This register is used to indicate interrupts generated from the RSEF blocks #17 through #32.

RSEFI[32:17]

The RSEF #*X* interrupt event indication (RSEFI[X]) transitions to logic 1 when a hardware interrupt event is sourced from RSEF #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0010H Master RSEF Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	RSEFI[48]	X
Bit 14	R	RSEFI[47]	X
Bit 13	R	RSEFI[46]	X
Bit 12	R	RSEFI[45]	X
Bit 11	R	RSEFI[44]	X
Bit 10	R	RSEFI[43]	X
Bit 9	R	RSEFI[42]	X
Bit 8	R	RSEFI[41]	X
Bit 7	R	RSEFI[40]	X
Bit 6	R	RSEFI[39]	X
Bit 5	R	RSEFI[38]	X
Bit 4	R	RSEFI[37]	X
Bit 3	R	RSEFI[36]	X
Bit 2	R	RSEFI[35]	X
Bit 1	R	RSEFI[34]	X
Bit 0	R	RSEFI[33]	X

This register is used to indicate interrupts generated from the RSEF blocks #33 through #48.

RSEFI[48:33]

The RSEF #*X* interrupt event indication (RSEFI[X]) transitions to logic 1 when a hardware interrupt event is sourced from RSEF #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0011H Master RSEF Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	RSEFI[64]	X
Bit 14	R	RSEFI[63]	X
Bit 13	R	RSEFI[62]	X
Bit 12	R	RSEFI[61]	X
Bit 11	R	RSEFI[60]	X
Bit 10	R	RSEFI[59]	X
Bit 9	R	RSEFI[58]	X
Bit 8	R	RSEFI[57]	X
Bit 7	R	RSEFI[56]	X
Bit 6	R	RSEFI[55]	X
Bit 5	R	RSEFI[54]	X
Bit 4	R	RSEFI[53]	X
Bit 3	R	RSEFI[52]	X
Bit 2	R	RSEFI[51]	X
Bit 1	R	RSEFI[50]	X
Bit 0	R	RSEFI[49]	X

This register is used to indicate interrupts generated from the RSEF blocks #49 through #64.

RSEFI[64:49]

The RSEF #*X* interrupt event indication (RSEFI[X]) transitions to logic 1 when a hardware interrupt event is sourced from RSEF #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0012H Master PIPM Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	PIPMI[16]	X
Bit 14	R	PIPMI[15]	X
Bit 13	R	PIPMI[14]	X
Bit 12	R	PIPMI[13]	X
Bit 11	R	PIPMI[12]	X
Bit 10	R	PIPMI[11]	X
Bit 9	R	PIPMI[10]	X
Bit 8	R	PIPMI[9]	X
Bit 7	R	PIPMI[8]	X
Bit 6	R	PIPMI[7]	X
Bit 5	R	PIPMI[6]	X
Bit 4	R	PIPMI[5]	X
Bit 3	R	PIPMI[4]	X
Bit 2	R	PIPMI[3]	X
Bit 1	R	PIPMI[2]	X
Bit 0	R	PIPMI[1]	X

This register is used to indicate interrupts generated from the PIPM blocks #1 through #16.

PIPMI[16:1]

The PIPM #*X* interrupt event indication (PIPMI[X]) transitions to logic 1 when a hardware interrupt event is sourced from PIPM #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0013H Master PIPM Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	PIPMI[32]	X
Bit 14	R	PIPMI[31]	X
Bit 13	R	PIPMI[30]	X
Bit 12	R	PIPMI[29]	X
Bit 11	R	PIPMI[28]	X
Bit 10	R	PIPMI[27]	X
Bit 9	R	PIPMI[26]	X
Bit 8	R	PIPMI[25]	X
Bit 7	R	PIPMI[24]	X
Bit 6	R	PIPMI[23]	X
Bit 5	R	PIPMI[22]	X
Bit 4	R	PIPMI[21]	X
Bit 3	R	PIPMI[20]	X
Bit 2	R	PIPMI[19]	X
Bit 1	R	PIPMI[18]	X
Bit 0	R	PIPMI[17]	X

This register is used to indicate interrupts generated from the PIPM blocks #17 through #32.

PIPMI[32:17]

The PIPM #*X* interrupt event indication (PIPMI[X]) transitions to logic 1 when a hardware interrupt event is sourced from PIPM #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0014H Master PIPM Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	PIPMI[48]	X
Bit 14	R	PIPMI[47]	X
Bit 13	R	PIPMI[46]	X
Bit 12	R	PIPMI[45]	X
Bit 11	R	PIPMI[44]	X
Bit 10	R	PIPMI[43]	X
Bit 9	R	PIPMI[42]	X
Bit 8	R	PIPMI[41]	X
Bit 7	R	PIPMI[40]	X
Bit 6	R	PIPMI[39]	X
Bit 5	R	PIPMI[38]	X
Bit 4	R	PIPMI[37]	X
Bit 3	R	PIPMI[36]	X
Bit 2	R	PIPMI[35]	X
Bit 1	R	PIPMI[34]	X
Bit 0	R	PIPMI[33]	X

This register is used to indicate interrupts generated from the PIPM blocks #33 through #48.

PIPMI[48:33]

The PIPM #*X* interrupt event indication (PIPMI[X]) transitions to logic 1 when a hardware interrupt event is sourced from PIPM #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0015H Master PIPM Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	PIPMI[64]	X
Bit 14	R	PIPMI[63]	X
Bit 13	R	PIPMI[62]	X
Bit 12	R	PIPMI[61]	X
Bit 11	R	PIPMI[60]	X
Bit 10	R	PIPMI[59]	X
Bit 9	R	PIPMI[58]	X
Bit 8	R	PIPMI[57]	X
Bit 7	R	PIPMI[56]	X
Bit 6	R	PIPMI[55]	X
Bit 5	R	PIPMI[54]	X
Bit 4	R	PIPMI[53]	X
Bit 3	R	PIPMI[52]	X
Bit 2	R	PIPMI[51]	X
Bit 1	R	PIPMI[50]	X
Bit 0	R	PIPMI[49]	X

This register is used to indicate interrupts generated from the PIPM blocks #49 through #64.

PIPMI[64:49]

The PIPM #*X* interrupt event indication (PIPMI[X]) transitions to logic 1 when a hardware interrupt event is sourced from PIPM #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0016H Master RTSI Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	RTSII[16]	X
Bit 14	R	RTSII[15]	X
Bit 13	R	RTSII[14]	X
Bit 12	R	RTSII[13]	X
Bit 11	R	RTSII[12]	X
Bit 10	R	RTSII[11]	X
Bit 9	R	RTSII[10]	X
Bit 8	R	RTSII[9]	X
Bit 7	R	RTSII[8]	X
Bit 6	R	RTSII[7]	X
Bit 5	R	RTSII[6]	X
Bit 4	R	RTSII[5]	X
Bit 3	R	RTSII[4]	X
Bit 2	R	RTSII[3]	X
Bit 1	R	RTSII[2]	X
Bit 0	R	RTSII[1]	X

This register is used to indicate interrupts generated from the RTSI blocks #1 through #16.

RTSII[16:1]

The RTSI #*X* interrupt event indication (RTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from RTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0017H Master RTSI Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	RTSII[32]	X
Bit 14	R	RTSII[31]	X
Bit 13	R	RTSII[30]	X
Bit 12	R	RTSII[29]	X
Bit 11	R	RTSII[28]	X
Bit 10	R	RTSII[27]	X
Bit 9	R	RTSII[26]	X
Bit 8	R	RTSII[25]	X
Bit 7	R	RTSII[24]	X
Bit 6	R	RTSII[23]	X
Bit 5	R	RTSII[22]	X
Bit 4	R	RTSII[21]	X
Bit 3	R	RTSII[20]	X
Bit 2	R	RTSII[19]	X
Bit 1	R	RTSII[18]	X
Bit 0	R	RTSII[17]	X

This register is used to indicate interrupts generated from the RTSI blocks #17 through #32.

RTSII[32:17]

The RTSI #*X* interrupt event indication (RTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from RTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0018H Master RTSI Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	RTSII[48]	X
Bit 14	R	RTSII[47]	X
Bit 13	R	RTSII[46]	X
Bit 12	R	RTSII[45]	X
Bit 11	R	RTSII[44]	X
Bit 10	R	RTSII[43]	X
Bit 9	R	RTSII[42]	X
Bit 8	R	RTSII[41]	X
Bit 7	R	RTSII[40]	X
Bit 6	R	RTSII[39]	X
Bit 5	R	RTSII[38]	X
Bit 4	R	RTSII[37]	X
Bit 3	R	RTSII[36]	X
Bit 2	R	RTSII[35]	X
Bit 1	R	RTSII[34]	X
Bit 0	R	RTSII[33]	X

This register is used to indicate interrupts generated from the RTSI blocks #33 through #48.

RTSII[48:33]

The RTSI #*X* interrupt event indication (RTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from RTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0019H Master RTSI Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	RTSII[64]	X
Bit 14	R	RTSII[63]	X
Bit 13	R	RTSII[62]	X
Bit 12	R	RTSII[61]	X
Bit 11	R	RTSII[60]	X
Bit 10	R	RTSII[59]	X
Bit 9	R	RTSII[58]	X
Bit 8	R	RTSII[57]	X
Bit 7	R	RTSII[56]	X
Bit 6	R	RTSII[55]	X
Bit 5	R	RTSII[54]	X
Bit 4	R	RTSII[53]	X
Bit 3	R	RTSII[52]	X
Bit 2	R	RTSII[51]	X
Bit 1	R	RTSII[50]	X
Bit 0	R	RTSII[49]	X

This register is used to indicate interrupts generated from the RTSI blocks #49 through #64.

RTSII[64:49]

The RTSI #*X* interrupt event indication (RTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from RTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 001AH Master TTSI Interrupt Source #1

Bit	Type	Function	Default
Bit 15	R	TTSII[16]	X
Bit 14	R	TTSII[15]	X
Bit 13	R	TTSII[14]	X
Bit 12	R	TTSII[13]	X
Bit 11	R	TTSII[12]	X
Bit 10	R	TTSII[11]	X
Bit 9	R	TTSII[10]	X
Bit 8	R	TTSII[9]	X
Bit 7	R	TTSII[8]	X
Bit 6	R	TTSII[7]	X
Bit 5	R	TTSII[6]	X
Bit 4	R	TTSII[5]	X
Bit 3	R	TTSII[4]	X
Bit 2	R	TTSII[3]	X
Bit 1	R	TTSII[2]	X
Bit 0	R	TTSII[1]	X

This register is used to indicate interrupts generated from the TTSI blocks #1 through #16.

TTSII[16:1]

The TTSI #*X* interrupt event indication (TTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from TTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 001BH Master TTSI Interrupt Source #2

Bit	Type	Function	Default
Bit 15	R	TTSII[32]	X
Bit 14	R	TTSII[31]	X
Bit 13	R	TTSII[30]	X
Bit 12	R	TTSII[29]	X
Bit 11	R	TTSII[28]	X
Bit 10	R	TTSII[27]	X
Bit 9	R	TTSII[26]	X
Bit 8	R	TTSII[25]	X
Bit 7	R	TTSII[24]	X
Bit 6	R	TTSII[23]	X
Bit 5	R	TTSII[22]	X
Bit 4	R	TTSII[21]	X
Bit 3	R	TTSII[20]	X
Bit 2	R	TTSII[19]	X
Bit 1	R	TTSII[18]	X
Bit 0	R	TTSII[17]	X

This register is used to indicate interrupts generated from the TTSI blocks #17 through #32.

TTSII[32:17]

The TTSI #*X* interrupt event indication (TTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from TTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 001CH Master TTSI Interrupt Source #3

Bit	Type	Function	Default
Bit 15	R	TTSII[48]	X
Bit 14	R	TTSII[47]	X
Bit 13	R	TTSII[46]	X
Bit 12	R	TTSII[45]	X
Bit 11	R	TTSII[44]	X
Bit 10	R	TTSII[43]	X
Bit 9	R	TTSII[42]	X
Bit 8	R	TTSII[41]	X
Bit 7	R	TTSII[40]	X
Bit 6	R	TTSII[39]	X
Bit 5	R	TTSII[38]	X
Bit 4	R	TTSII[37]	X
Bit 3	R	TTSII[36]	X
Bit 2	R	TTSII[35]	X
Bit 1	R	TTSII[34]	X
Bit 0	R	TTSII[33]	X

This register is used to indicate interrupts generated from the TTSI blocks #33 through #48.

TTSII[48:33]

The TTSI #*X* interrupt event indication (TTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from TTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 001DH Master TTSI Interrupt Source #4

Bit	Type	Function	Default
Bit 15	R	TTSII[64]	X
Bit 14	R	TTSII[63]	X
Bit 13	R	TTSII[62]	X
Bit 12	R	TTSII[61]	X
Bit 11	R	TTSII[60]	X
Bit 10	R	TTSII[59]	X
Bit 9	R	TTSII[58]	X
Bit 8	R	TTSII[57]	X
Bit 7	R	TTSII[56]	X
Bit 6	R	TTSII[55]	X
Bit 5	R	TTSII[54]	X
Bit 4	R	TTSII[53]	X
Bit 3	R	TTSII[52]	X
Bit 2	R	TTSII[51]	X
Bit 1	R	TTSII[50]	X
Bit 0	R	TTSII[49]	X

This register is used to indicate interrupts generated from the TTSI blocks #49 through #64.

TTSII[64:49]

The TTSI #*X* interrupt event indication (TTSII[X]) transitions to logic 1 when a hardware interrupt event is sourced from TTSI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 001EH Master Test and CSUI Interrupt Source

Bit	Type	Function	Default
Bit 15	R	TST_RSEFI	X
Bit 14	R	TST_RTSII	X
Bit 13	R	TST_PIPMI	X
Bit 12	R	TST_TTSII	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	CSUII[4]	X
Bit 2	R	CSUII[3]	X
Bit 1	R	CSUII[2]	X
Bit 0	R	CSUII[1]	X

This register is used to indicate interrupts generated from the CSUI blocks #1 through #4.

CSUII[4:1]

The CSUI #*X* interrupt event indication (CSUII[X]) transitions to logic 1 when a hardware interrupt event is sourced from CSUI #*X* block. This bit is cleared to logic 0 when the interrupt is cleared.

TST_TTSII

The test port TTSI interrupt event indication (TST_TTSII) transitions to logic 1 when a hardware interrupt event is sourced from the test port TTSI block, TTSI #65. This bit is cleared to logic 0 when the interrupt is cleared.

TST_PIPMI

The test port PIPM interrupt event indication (TST_PIPMI) transitions to logic 1 when a hardware interrupt event is sourced from the test port PIPM block, PIPM #65. This bit is cleared to logic 0 when the interrupt is cleared.

TST_RSTII

The test port RTSI interrupt event indication (TST_RTSII) transitions to logic 1 when a hardware interrupt event is sourced from the test port RTSI block, RTSI #65. This bit is cleared to logic 0 when the interrupt is cleared.

TST_RSEFI

The test port RSEF interrupt event indication (TST_RSEFI) transitions to logic 1 when a hardware interrupt event is sourced from the test port RSEF block, RSEF #65. This bit is cleared to logic 0 when the interrupt is cleared.

Register: 0030H, 0038H, 0040H, 0048H CSUI #1 – #4 Interrupt Enable and CSU Lock Status

Bit	Type	Function	Default
Bit 15	R	Reserved [5]	X
Bit 14	R	Reserved [4]	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R	Reserved [3]	X
Bit 9	R	Reserved [2]	X
Bit 8	R	PLL_LOCKV	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	Reserved [1]	0
Bit 1	R/W	Reserved [0]	0
Bit 0	R/W	PLL_LOCKE	0

The Reserved [1:0] bits should be written to their default value for correct operation of the device.

This register configures the operation of CSUI blocks #1 through #4. Register 0030H, 0038H, 0040H, and 0048H control the CSU for faces # 1, #2, #3, and #4 respectively.

PLL_LOCKE

The CSU PLL lock interrupt enable bit (PLL_LOCKE) controls the assertion of the PLL lock state interrupt by the device. When PLL_LOCKE is high, an interrupt is generated on INTB when the PLL lock state changes. Interrupts due to changes in the PLL lock state are masked when PLL_LOCKE is set low. Note that PLL_LOCKE only affects the INTB output; the PLL_LOCKI bit remains valid at all times.

PLL_LOCKV

The CSU PLL lock status bit (PLL_LOCKV) indicates whether the PLL in the clock synthesis unit is currently locked with the associated reference clock on the same face. PLL_LOCKV is set high when the PLL is in lock, the normal operating mode. PLL_LOCKV is set low when the PLL is not in the locked condition.

Register: 0031H, 0039H, 0041H, 0049H CSUI #1 - #4 Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	Reserved [1]	X
Bit 1	R	Reserved [0]	X
Bit 0	R	PLL_LOCKI	X

Registers 0031H, 0039H, 0041H, and 0049H report the interrupt status for the CSUs for faces # 1, #2, #3, and #4 respectively.

PLL_LOCKI

The CSU PLL lock interrupt status bit (LOCKI) indicates when the CSU either achieves or loses lock on REFCLK. The PLL_LOCKI register bit is set high when the PLL lock state changes. The PLL_LOCKI bit is cleared according to the value of WCIMODE. If WCIMODE is “0”, The PLL_LOCKI register bit is cleared when it is read. If WCIMODE is “1”, the PLL_LOCKI register bit is cleared when a ‘1’ is written to it. When PLL_LOCKE is set high, PLL_LOCKI contributes to the interrupt output INTB. Whether or not the interrupt is masked by the PLL_LOCKE and Register 0009H: Master Interrupt Enable CSUIE bits, the PLL_LOCKI bit itself remains valid and may be polled to detect change of lock status events.

Register: 0032H, 003AH, 0042H, 004AH CSUI #1 - #4 Feedback Divider

Bit	Type	Function	Default
Bit 15	R/W	TM_FBDIVCTRL	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TM_FBDIV[11]	0
Bit 10	R/W	TM_FBDIV[10]	1
Bit 9	R/W	TM_FBDIV[9]	1
Bit 8	R/W	TM_FBDIV[8]	1
Bit 7	R/W	TM_FBDIV[7]	0
Bit 6	R/W	TM_FBDIV[6]	0
Bit 5	R/W	TM_FBDIV[5]	0
Bit 4	R/W	TM_FBDIV[4]	0
Bit 3	R/W	TM_FBDIV[3]	1
Bit 2	R/W	TM_FBDIV[2]	1
Bit 1	R/W	TM_FBDIV[1]	0
Bit 0	R/W	TM_FBDIV[0]	0

Registers 0032H, 003AH, 0042H, and 004AH provide CSU Feedback divider settings for faces # 1, #2, #3, and #4 respectively.

TM_FBDIV[11:0]

The CSU Feedback Divider (TM_FBDIV[11:0]) register bits are used as the CSU feedback divider input when TM_FBDIVCTRL is logic 1. When TM_FBDIVCTRL is logic 0, default (with the exception of STS-12 scrambled mode and STS-12 8B/10B encoded mode using a 77.76 MHz clock) correct values are used as the CSU feedback divider input and the TM_FBDIV values are not used. Legal values of TM_FBDIV are listed below.

Desired Operation	TMFBDIV_CTRL required setting	TM_FBDIV [11:0] if TMFBDIVCTRL=1
STS-48 REFCLK = 155.52 MHz	N/A	0111 1100 1100
STS-12 – 8B/10B encoded REFCLK = 155.52 MHz	N/A	0111 0000 1100
STS-12 – 8B/10B encoded REFCLK = 77.76 MHz	1	1111 0000 1100
STS-12 – Scrambled REFCLK =	1	0110 0000 1000

Desired Operation	TMFBDIV_CTRL required setting	TM_FBDIV [11:0] if TMFBDIVCTRL=1
155.52MHz		
STS-12 – Scrambled REFCLK = 77.76MHz	1	1110 0000 1000

TM_FBDIVCTRL

The CSU FBDIV test mode control (TM_FBDIVCTRL) controls whether the TM_FBDIV register is used as the CSU feedback value. The CSU uses hard wired values when TM_FBDIVCTRL is logic 0. The CSU uses the TM_FBDIV register when TM_FBDIVCTRL is logic 1.

Register: 0033H, 003BH, 0043H, 004BH CSUI #1 - #4 Control

Bit	Type	Function	Default
Bit 15	R/W	ELVDS_RSTB	1
Bit 14	R/W	ELVDS_PWRDNB	0
Bit 13	—	Unused	X
Bit 12	R/W	Reserved [12]	0
Bit 11	R/W	Reserved [11]	0
Bit 10	R/W	Reserved [10]	0
Bit 9	R/W	Reserved [9]	0
Bit 8	R/W	Reserved [8]	0
Bit 7	R/W	Reserved [7]	0
Bit 6	R/W	Reserved [6]	0
Bit 5	R/W	Reserved [5]	0
Bit 4	R/W	Reserved [4]	0
Bit 3	R/W	Reserved [3]	0
Bit 2	R/W	Reserved [2]	0
Bit 1	R/W	Reserved [1]	0
Bit 0	R/W	Reserved [0]	1

The Reserved[12:0] bits should be written to their default value for correct operation of the device.

Registers 0033H, 003BH, 0043H, and 004BH provide access to the CSUI control settings on faces # 1, #2, #3, and #4 respectively.

ELVDS_PWRDNB

The ELVDS_PWRDNB bit must be set to logic 1 following power up or reset of the device, where the device reset is either through the RSTB pin or the DRESET bit. This is essential for proper operation of the device. A ELVDS powerdown function is no longer supported with these bits. For instructions on minimizing the power consumption for a face please refer to Section 12.5. To minimize power consumption caused by enabling all faces, apply the face low power mode settings contained in Table 25 in the indicated ordering immediately prior to setting this bit.

ELVDS_RSTB

The ELVDS_RSTB bit drives a software reset signal that forces all the ELVDS analog blocks including the CSU on the face into reset. The top level ARESET register bit and RSTB pin will also force the CSU into reset. For normal operation, ELVDS_RSTB is held at logic ‘1’. To properly reset the ELVDS blocks, the ELVDS_RSTB pin should be held low for at least 100 us. Invoking this feature effectively disables the corresponding face. When the CSU is held in reset, either all or some major sub-block contained within digital blocks RSEF, PIPM, RTSI, TTSI, and TSEC on the corresponding face will not receive a clock, and are effectively disabled.. Note the CSU should not need to be reset under ordinary conditions. The CSU is automatically reset when a lock detection circuit discovers the CSU is not locked on the reference clock.

Register: 0034H, 003CH, 0044H, 004CH CSUI #1 - #4 AC Coupling Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved [10]	0
Bit 14	R/W	Reserved [9]	0
Bit 13	R/W	Reserved [8]	0
Bit 12	R/W	ACCOUPLE[4]	0
Bit 11	R/W	Reserved [7]	0
Bit 10	R/W	Reserved [6]	0
Bit 9	R/W	Reserved [5]	0
Bit 8	R/W	Reserved [4]	1
Bit 7	R/W	ACCOUPLE[3]	0
Bit 6	R/W	ACCOUPLE[2]	0
Bit 5	R/W	ACCOUPLE[1]	0
Bit 4	R/W	ACCOUPLE[0]	0
Bit 3	R/W	Reserved [3]	0
Bit 2	R/W	Reserved [2]	0
Bit 1	R/W	Reserved [1]	0
Bit 0	R/W	Reserved [0]	0

The Reserved[10:0] bits should be written to their default value for correct operation of the device.

Registers 0034H, 003CH, 0044H, and 004CH provide access to the CSUI test output enable control settings on faces # 1, #2, #3, and #4 respectively.

ACCOUPLE[4]

The ELVDS receive channel AC coupling control bit (ACCOUPLE[4]) selects either AC or DC coupling for the ELVDS 65th receive channel (test port). AC coupling allows the ELVDS links to interoperate with PECL or CML level transmitters. The ACCOUPLE bit should be set to logic 1 when the corresponding receive channels are externally AC coupled. The ACCOUPLE bit should be set to logic 0, when the corresponding channels are externally DC coupled. **This bit is only present in register 004CH.**

ACCOUPLE[3:0]

The ELVDS receive channel AC coupling control bits (ACCOUPLE[3:0]) selects either AC or DC coupling in the ELVDS receive channels. AC coupling allows the ELVDS links to interoperate with PECL or CML level transmitters. Each ACCOUPLE[3:0] bit controls 4 channels. The correspondence of ACCOUPLE bit to channels is detailed in Table 11. The ACCOUPLE bit should be set to logic 1 if the corresponding receive channels are externally AC coupled. The ACCOUPLE bit should be set to logic 0 if the corresponding channels are externally DC coupled.

Table 11 ACCOUPLE Link Correspondence

ACCOUPLE[i]	Face 1	Face 2	Face 3	Face 4
0	1-4	17-20	33-36	49-52
1	5-8	21-24	37-40	53-56
2	9-12	25-28	41-44	57-60
3	13-16	29-32	45-48	61-64
4	N/A	N/A	N/A	65

Register: 0036H, 003E, 0046H, 004EH FACE #1 - #4 Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved [11]	0
Bit 14	R/W	Reserved [10]	0
Bit 13	R/W	Reserved [9]	0
Bit 12	R/W	RFCLKR_SEL	0
Bit 11	R/W	EBTBENB	0
Bit 10	R/W	HR_MODEB	0
Bit 9	R/W	HICUR	0
Bit 8	R/W	Reserved [8]	0
Bit 7	R/W	Reserved [7]	0
Bit 6	R/W	Reserved [6]	0
Bit 5	R/W	Reserved [5]	0
Bit 4	R/W	Reserved [4]	0
Bit 3	R/W	Reserved [3]	0
Bit 2	R/W	Reserved [2]	0
Bit 1	R/W	Reserved [1]	0
Bit 0	R/W	Reserved [0]	0

The Reserved [11:0] bits should be written to their default value for correct operation of the device.

Registers 0036H, 003EH, 0046H, and 004EH provide per channel configuration on faces 1,2,3 and 4 respectively.

HICUR

The High Current Mode select bit (HICUR) controls the TXLV driver power selection on the associated face. When HICUR is set to logic 1 the TXLV driver is in “high current” mode. This is suitable for longer trace lengths. When HICUR is set to logic 0, the TXLV driver is in “Low-Swing” mode. This mode is suitable for those situations when the board trace length is shorter and direct. Low-Swing mode is appropriate for the transmitters if the far end receivers are on the same card. For Low-Swing mode, both the Register MN32H: TSEC Enable Control PREEMPH_EN bits and HICUR should be logic 0. For Normal Operation, HICUR should be logic 1 and PREEMPH_EN should be logic 0. For pre-emphasis mode, both HICUR and PREEMPH_EN should be logic 1.

HR_MODEB

The HR_MODEB bit configures the DRUs and PISOs on the associated face for half rate mode operation. HR_MODEB must be set to logic 0 on faces configured for STS-12 operation. HR_MODEB must be set to logic 1 for faces not configured for STS-12 operation.

EBTBENB

The EBTBENB bit configures a face for 8B/10B operation._EBTBENB also configures the data width interface between the Analog Receive and Transmit Blocks and their respective interfacing digital blocks, the RSEF and TSEC. When set to logic 0, the interface is 10 bits wide for 8B/10B encoded data. When set to logic 1 the interface is eight bits wide for scrambled data. EBTBENB must be set to logic 0 for STS-12 8B/10B encoded data. EBTBENB must be set to logic 1 otherwise.

RFCLKR_SEL

The REFCLK Rate Select (RFCLKR_SEL) bit configures a face for operation with the two allowed REFCLK frequencies. If the REFCLK_N/P for the face is 155.52 MHz, the RFCLKR_SEL must be logic 0. If the REFCLK_N/P for the face is 77.76, then RFCLKR_SEL must be logic 1. Note: a REFCLK_N/P rate of 77.76 MHz is supported for only 777.6 MHz links.

Register: 0060H SSWE Indirect Access Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	PAGE	0
Bit 12	R/W	TS_SEL[5]	0
Bit 11	R/W	TS_SEL[4]	0
Bit 10	R/W	TS_SEL[3]	0
Bit 9	R/W	TS_SEL[2]	0
Bit 8	R/W	TS_SEL[1]	0
Bit 7	R/W	TS_SEL[0]	1
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	DOUTSEL[4]	0
Bit 3	R/W	DOUTSEL[3]	0
Bit 2	R/W	DOUTSEL[2]	0
Bit 1	R/W	DOUTSEL[1]	0
Bit 0	R/W	DOUTSEL[0]	0

This register provides the outgoing stream, time slot, and control page used to access the multiplexer control blocks of the outgoing data streams. Writing to this register triggers an indirect register access.

DOUTSEL[4:0]

DOUTSEL[4:0] selects the set of four outputs to be configured during the indirect access. DOUTSEL is used in conjunction with the DINSEL0, DINSEL1, DINSEL2 and DINSEL3 fields in the two SSWE Indirect Access Data Registers to facilitate simultaneous read/write to four outputs. Table 12 shows the correspondence between DOUTSEL, DINSEL*n*, and the output port.

Table 12 Outputs Selection with DOUTSEL and DINSEL*n*

DOUTSEL[4:0]	Corresponding Output Ports			
	DINSEL0	DINSEL1	DINSEL2	DINSEL3
0	1	2	3	4
1	5	6	7	8
.	.	.	.	.
N	4*N+1	4*N+2	4*N+3	4*N+4
.	.	.	.	.
15	61	62	63	64

DOUTSEL[4:0]	Corresponding Output Ports			
	DINSEL0	DINSEL1	DINSEL2	DINSEL3
16	65	Not Used	Not Used	Not Used
17-31	Invalid DOUTSEL	Invalid DOUTSEL	Invalid DOUTSEL	Invalid DOUTSEL

Note: When the value of DOUTSEL is 16, output 65 is selected. In this case DINSEL0 (the low order byte in Indirect Access Data 1) contains the output control word and the DINSEL1, DINSEL2, and DINSEL3 values are ignored.

TS_SEL[5:0]

The indirect time-slot number bits (TS_SEL[5:0]) indicate the time-slot to be configured or interrogated in the indirect access. The decimal value of TS_SEL corresponds to the timeslot to be configured – e.g. if TS_SEL is 5, then the configuration/interrogation is for timeslot #5. The following table shows valid TS_SEL values.

Table 13 Control Word Index

Core Timeslot Mode	Invalid TS_SEL	Valid TS_SEL	Invalid TS_SEL
12	0	1-12	13-63
48	0	1-48	49-63

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

Table 14 PAGE Index

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control memory. The address to the control memory is constructed from the PAGE, DOUTSEL[4:0] and TS_SEL[5:0] fields. Writing a logic 0 to RWB triggers an indirect write operation; the data that is to be written is taken from the Indirect Access Data registers. Writing a logic 1 to RWB triggers an indirect read operation. Addressing of the RAM is the same as in an indirect write operation. The data read can be found in the Indirect Access Data registers after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access and will stay high until the access is complete. Once the indirect operation is complete, the BUSY bit is cleared (low). This register should be polled to determine when data from an indirect read operation is available in the Indirect Access Data registers or to determine when a new indirect write operation may commence. Any indirect operation that is initiated while BUSY is still high will corrupt data.

Register: 0061H SSWE Indirect Access Data 1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	DINSEL1[6]	0
Bit 13	R/W	DINSEL1[5]	0
Bit 12	R/W	DINSEL1[4]	0
Bit 11	R/W	DINSEL1[3]	0
Bit 10	R/W	DINSEL1[2]	0
Bit 9	R/W	DINSEL1[1]	0
Bit 8	R/W	DINSEL1[0]	0
Bit 7	—	Unused	X
Bit 6	R/W	DINSEL0[6]	0
Bit 5	R/W	DINSEL0[5]	0
Bit 4	R/W	DINSEL0[4]	0
Bit 3	R/W	DINSEL0[3]	0
Bit 2	R/W	DINSEL0[2]	0
Bit 1	R/W	DINSEL0[1]	0
Bit 0	R/W	DINSEL0[0]	0

This register and the SSWE Indirect Access Data 2 register contain the data to be written into the control word in an indirect write access or the data read from the control word in an indirect read access. Note that the used bits in this register default to 0, but words in the control memory do not have any default.

DINSEL0[6:0], DINSEL1[6:0]

The input data port select (DINSELn[6:0]) selects an input port as the data source for the output port for the timeslot specified in the TS_SEL register. Each DINSELn represents one control setting within a control word that contains 4 control settings. In an indirect write operation, each control setting must be set up in this register before triggering the indirect write. When read back, DINSELn reflects the value written until the completion of a subsequent indirect channel write operation. This register should not be read or written to unless the BUSY bit in the SSWE Indirect Access Configuration register indicates that the previous indirect access operation is complete. When DOUTSEL in the SSWE Indirect Access Configuration register is equal to 16, DINSEL0 is the only DINSEL value used. Table 12 shows the mapping of DINSELn and DOUTSEL to output ports. Table 15 illustrates how the value of DINSELn controls the corresponding mux. Note: prior to any indirect write both SSWE Indirect Access Data registers (0061H and 0062H) must be written to update their contents, regardless of the data read from them.

Table 15 DINSEL*n*[6:0] Mapping

Mux Control word DINSEL*n*[6:0]	Input Port Selection
0	1
1	2
2	3
.	.
N	N+1
.	.
63	64
64	65
65-127	Invalid Selection

Register: 0062H SSWE Indirect Access Data 2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	DINSEL3[6]	0
Bit 13	R/W	DINSEL3[5]	0
Bit 12	R/W	DINSEL3[4]	0
Bit 11	R/W	DINSEL3[3]	0
Bit 10	R/W	DINSEL3[2]	0
Bit 9	R/W	DINSEL3[1]	0
Bit 8	R/W	DINSEL3[0]	0
Bit 7	—	Unused	X
Bit 6	R/W	DINSEL2[6]	0
Bit 5	R/W	DINSEL2[5]	0
Bit 4	R/W	DINSEL2[4]	0
Bit 3	R/W	DINSEL2[3]	0
Bit 2	R/W	DINSEL2[2]	0
Bit 1	R/W	DINSEL2[1]	0
Bit 0	R/W	DINSEL2[0]	0

This register and the SSWE Indirect Access Data 1 register contain the data to be written into the control word in an indirect write access or the data read from the control word in an indirect read access. Note that the used bits in this register default to 0, but words in the control memory do not have any default.

DINSEL2[6:0], DINSEL3[6:0]

The input data port select (DINSEL*n*[6:0]) selects an input port as the data source for the output port for the timeslot specified in the TS_SEL register. Each DINSELn represents one control setting within a control word that contains 4 control settings. In an indirect write operation, each control setting must be set up in this register before triggering the indirect write. When read back, DINSEL*n* reflects the value written until the completion of a subsequent indirect channel write operation. This register should not be read or written to unless the BUSY bit in the SSWE Indirect Access Configuration register indicates that the previous indirect access operation is complete. When DOUTSEL in the SSWE Indirect Access Configuration register is equal to 16, DINSEL0 is the only DINSEL value used. Table 12 shows the mapping of DINSEL*n* and DOUTSEL to output ports. Table 15 illustrates how the value of DINSEL*n* controls the corresponding mux. Note: prior to any indirect write both SSWE Indirect Access Data registers (0061H and 0062H) must be written to update their contents, regardless of the data read from them.

Register: 0063H SSWE Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved [1]	0
Bit 14	R/W	Reserved [0]	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R	AWPBV	X
Bit 10	R	AWPAV	X
Bit 9	R/W	COWPBE	0
Bit 8	R/W	COWPAE	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	ACTIVEBV	X
Bit 4	R	ACTIVEAV	X
Bit 3	R/W	PSEL_B	0
Bit 2	R/W	PSEL_A	0
Bit 1	R/W	COAPBE	0
Bit 0	R/W	COAPAE	0

The Reserved [1:0] bits should be written to their default value for correct operation of the device.

This register provides interrupt enable in the SSWE, as well as page selection and receive working port configuration.

COAPAE

The change of active page interrupt enable for timing plane A (COAPAE) bit masks the change of page interrupt. When the COAPAE bit is set to logic 1, an interrupt is generated when the timing plane A active page changes from page 0 to page 1 or from page 1 to page 0. When COAPAE is set to logic 0 no interrupts are generated as a result of a change of page on timing plane A.

COAPBE

The change of active page interrupt enable for timing plane B (COAPBE) bit masks the change of page interrupt. When the COAPBE bit is set to logic 1, an interrupt is generated when the timing plane B active page changes from page 0 to page 1 or from page 1 to page 0. When COAPBE is set to logic 0 no interrupts are generated as a result of a change of page on timing plane B.

PSEL_A

The page select for timing plane A (PSEL_A) bit is used in the selection of the current active page in connection memory for timing plane A. This bit is logically XORed with the value of the external CMP_A signal to determine which control page is currently active for outputs within timing plane A. The delay between a PSEL_A change and the resulting change of page will be greater than 1 and less than 2 frame times.

PSEL_B

The page select for timing plane B (PSEL_B) bit is used in the selection of the current active page in connection memory for timing plane B. This bit is logically XORed with the value of the external CMP_B signal to determine which control page is currently active for outputs within timing plane B. The delay between a PSEL_B change and the resulting change of page will be greater than 1 and less than 2 frame times.

ACTIVEAV

The active page indication for timing plane A (ACTIVEAV) bit indicates which control page is currently active for timing plane A. When this bit is logic 0, then page 0 is used to switch timeslots within timing plane A. When this bit is logic 1, then page 1 is used to switch those timeslots.

ACTIVEBV

The active page indication for timing plane B (ACTIVEBV) bit indicates which control page is currently active for timing plane B. When this bit is logic 0, then page 0 is used to switch timeslots within timing plane B. When this bit is logic 1, then page 1 is used to switch those timeslots.

COWPAE

The change of working/protect timing plane A interrupt enable (COWPAE) bit masks the change of timing plane A working/protect interrupt. When the COWPAE bit is set to logic 1, an interrupt is generated when the timing plane A line interface changes from working to protect or protect to working. When COWPAE is set to logic 0, no interrupt is generated as a result of a change of working/protect on the timing plane A line interface.

COWPBE

The change of working/protect timing plane B interrupt enable (COWPBE) bit masks the change of timing plane B working/protect interrupt. When the COWPBE bit is set to logic 1, an interrupt is generated when the timing plane B line interface changes from working to protect or protect to working. When COWPBE is set to logic 0, no interrupt is generated as a result of a change of working/protect on the timing plane B line interface.

AWPAV

The active working/protect for timing plane A (AWPAV) bit indicates whether the line interface for timing plane A is receiving from the working interface or the protect interface. This bit is only meaningful if the RWSEL_A pin is being used and at least one RWSEL_EN bit for the timing plane A outputs is logic 1. When the AWPAV bit is logic 0, the timing plane A line interface is receiving from the protect interface. When this bit is logic 1, the timing plane A line interface is receiving from the working interface.

AWPBV

The active working/protect for timing plane B (AWPBV) bit indicates whether the line interface for timing plane B is receiving from the working interface or the protect interface. This bit is only meaningful if the RWSEL_B pin is being used and at least one RWSEL_EN bit for the timing plane B outputs is logic 1. When the AWPBV bit is logic 0, the timing plane B line interface is receiving from the protect interface. When this bit is logic 1, the timing plane B line interface is receiving from the working interface.

Register: 0064H SSWE Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R	COWPBI	X
Bit 8	R	COWPAI	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	COAPBI	X
Bit 0	R	COAPAI	X

This register provides interrupt status in the SSWE.

COAPAI

The change of active page interrupt statue bit (COAPAI) reports the status of the change of active page interrupt for timing plane A. COAPAI is set to logic 1 when the active control page for timing plane A changes from page 0 to page 1 or from page 1 to page 0. When WCIMODE is logic 0, COAPAI is cleared immediately following a read to this register. When WCIMODE is logic 1, COAPAI is cleared by writing a logic 1 to the COAPAI bit location. COAPAI remains operational when the interrupt is not enabled (COAPAE or Register 0009H: Master Interrupt Enable SSWEE bits set to logic 0) and may be polled to detect change of active control page events on timing plane A.

COAPBI

The change of active page interrupt bit (COAPBI) reports the status of the change of active page interrupt for timing plane B. COAPBI is set to logic 1 when the active control page for timing plane B changes from page 0 to page 1 or from page 1 to page 0. When WCIMODE is logic 0, COAPBI is cleared immediately following a read to this register. When WCIMODE is logic 1, COAPBI is cleared by writing a logic 1 to the COAPBI bit location. COAPBI remains operational when the interrupt is not enabled (COAPBE or Register 0009H: Master Interrupt Enable SSWEE bits set to logic 0) and may be polled to detect change of active control page events on timing plane B.

COWPAI

The change of working/protect timing plane A interrupt bit (COWPAI) reports the status of the change of working/protect interfaces for the enabled outgoing line interfaces within timing plane A. COWPAI is set to logic 1 when the line interface for timing plane A switches between working to protect or from protect to working. COWPAI is cleared immediately following a read to this register. COWPAI remains operational when the interrupt is not enabled (COWPAE or Register 0009H: Master Interrupt Enable SSWEE bits set to logic 0) and may be polled to detect change of working/protect on the timing plane A line interface.

COWPBI

The change of working/protect timing plane B interrupt bit (COWPBI) reports the status of the change of working/protect interfaces for the enabled outgoing line interfaces within timing plane B. COWPBI is set to logic 1 when the line interface for timing plane B switches between working to protect or from protect to working. When WCIMODE is logic 0, COWPBI is cleared immediately following a read to this register. When WCIMODE is logic 1, COWPBI is cleared by writing a logic 1 to the COWPBI bit location. COWPBI remains operational when the interrupt is not enabled (COWPBE or Register 0009H: Master Interrupt Enable SSWEE bits set to logic 0) and may be polled to detect change of working/protect on the timing plane B line interface.

Register: 0065H SSWE RWSEL Configuration

Bit	Type	Function	Default
Bit 15	R/W	RWSEL_EN[65]	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	WPMASK[4]	0
Bit 1	R/W	WPMASK[3]	0
Bit 0	R/W	WPMASK[2]	0

This register provides enable and offset bits for RWSEL operation.

WPMASK[4:2]

The working / protect link address mask (WPMASK[4:2]) bits control which address bits from the connection memory (DINSELn[4:2]) are affected by the working select pin (RWSEL). When WPMASK[i] is set high, DINSELn[i] is replaced by the complement of RWSEL_A or RWSEL_B for output ports that are enabled for working/protect selection (RWSEL_EN[x] = 1). Timing plane A transmit links use the complement of RWSEL_A. Timing plane B transmit links use the complement of RWSEL_B. When WPMASK[i] is set low, DINSELn[i] is used directly. WPMASK[4:2] has no effect on output ports that are not enabled for working / protect selection (RWSEL_EN[x] = 0). For those output ports, DINSELn[4:2] are used verbatim. Valid settings for WPMASK[4:2] are 000b, 001b, 010b, and 100b. Other settings are not supported.

RWSEL_EN[65]

The receive working select enable bit 65 (RWSEL_EN[65]) enables the RWSEL function for port 65. The RWSEL_EN bits are used to enable receive working/protect selection on a per output basis. If RWSEL_EN[I] is logic 1, then the i^{th} port is sensitive to RWSEL and the WPMASK bits are applied to the connection memory settings for that port. If RWSEL_EN[I] is logic 0, then the i^{th} port uses the connection memory settings without modification.

Register: 0066H SSWE RWSEL Enable #1

Bit	Type	Function	Default
Bit 15	R/W	RWSEL_EN[64]	0
Bit 14	R/W	RWSEL_EN[63]	0
Bit 13	R/W	RWSEL_EN[62]	0
Bit 12	R/W	RWSEL_EN[61]	0
Bit 11	R/W	RWSEL_EN[60]	0
Bit 10	R/W	RWSEL_EN[59]	0
Bit 9	R/W	RWSEL_EN[58]	0
Bit 8	R/W	RWSEL_EN[57]	0
Bit 7	R/W	RWSEL_EN[56]	0
Bit 6	R/W	RWSEL_EN[55]	0
Bit 5	R/W	RWSEL_EN[54]	0
Bit 4	R/W	RWSEL_EN[53]	0
Bit 3	R/W	RWSEL_EN[52]	0
Bit 2	R/W	RWSEL_EN[51]	0
Bit 1	R/W	RWSEL_EN[50]	0
Bit 0	R/W	RWSEL_EN[49]	0

This register provides RWSEL enable bits for output ports 49 through 64.

RWSEL_EN[64:49]

The receive working select enable bits (RWSEL_EN[64:49]) enable the RWSEL function for ports 64 to 49 respectively. The RWSEL_EN bits are used to enable receive working/protect selection on a per output basis. If RWSEL_EN[I] is logic 1, then the i^{th} port is sensitive to RWSEL and the WPMASK bits are applied to the connection memory settings for that port. If RWSEL_EN[I] is logic 0, then the i^{th} port uses the connection memory settings without modification.

Register: 0067H SSWE RWSEL Enable #2

Bit	Type	Function	Default
Bit 15	R/W	RWSEL_EN[48]	0
Bit 14	R/W	RWSEL_EN[47]	0
Bit 13	R/W	RWSEL_EN[46]	0
Bit 12	R/W	RWSEL_EN[45]	0
Bit 11	R/W	RWSEL_EN[44]	0
Bit 10	R/W	RWSEL_EN[43]	0
Bit 9	R/W	RWSEL_EN[42]	0
Bit 8	R/W	RWSEL_EN[41]	0
Bit 7	R/W	RWSEL_EN[40]	0
Bit 6	R/W	RWSEL_EN[39]	0
Bit 5	R/W	RWSEL_EN[38]	0
Bit 4	R/W	RWSEL_EN[37]	0
Bit 3	R/W	RWSEL_EN[36]	0
Bit 2	R/W	RWSEL_EN[35]	0
Bit 1	R/W	RWSEL_EN[34]	0
Bit 0	R/W	RWSEL_EN[33]	0

This register provides RWSEL enable bits for output ports 33 through 48.

RWSEL_EN[48:33]

The receive working select enable bits (RWSEL_EN[48:33]) enable the RWSEL function for ports 48 to 33 respectively. The RWSEL_EN bits are used to enable receive working/protect selection on a per output basis. If RWSEL_EN[I] is logic 1, then the i^{th} port is sensitive to RWSEL and the WPMASK bits are applied to the connection memory settings for that port. If RWSEL_EN[I] is logic 0, then the i^{th} port uses the connection memory settings without modification.

Register: 0068H SSWE RWSEL Enable #3

Bit	Type	Function	Default
Bit 15	R/W	RWSEL_EN[32]	0
Bit 14	R/W	RWSEL_EN[31]	0
Bit 13	R/W	RWSEL_EN[30]	0
Bit 12	R/W	RWSEL_EN[29]	0
Bit 11	R/W	RWSEL_EN[28]	0
Bit 10	R/W	RWSEL_EN[27]	0
Bit 9	R/W	RWSEL_EN[26]	0
Bit 8	R/W	RWSEL_EN[25]	0
Bit 7	R/W	RWSEL_EN[24]	0
Bit 6	R/W	RWSEL_EN[23]	0
Bit 5	R/W	RWSEL_EN[22]	0
Bit 4	R/W	RWSEL_EN[21]	0
Bit 3	R/W	RWSEL_EN[20]	0
Bit 2	R/W	RWSEL_EN[19]	0
Bit 1	R/W	RWSEL_EN[18]	0
Bit 0	R/W	RWSEL_EN[17]	0

This register provides RWSEL enable bits for output ports 17 through 32.

RWSEL_EN[32:17]

The receive working select enable bits (RWSEL_EN[32:17]) enable the RWSEL function for ports 32 to 17 respectively. The RWSEL_EN bits are used to enable receive working/protect selection on a per output basis. If RWSEL_EN[I] is logic 1, then the i^{th} port is sensitive to RWSEL and the WPMASK bits are applied to the connection memory settings for that port. If RWSEL_EN[I] is logic 0, then the i^{th} port uses the connection memory settings without modification.

Register: 0069H SSWE RWSEL Enable #4

Bit	Type	Function	Default
Bit 15	R/W	RWSEL_EN[16]	0
Bit 14	R/W	RWSEL_EN[15]	0
Bit 13	R/W	RWSEL_EN[14]	0
Bit 12	R/W	RWSEL_EN[13]	0
Bit 11	R/W	RWSEL_EN[12]	0
Bit 10	R/W	RWSEL_EN[11]	0
Bit 9	R/W	RWSEL_EN[10]	0
Bit 8	R/W	RWSEL_EN[9]	0
Bit 7	R/W	RWSEL_EN[8]	0
Bit 6	R/W	RWSEL_EN[7]	0
Bit 5	R/W	RWSEL_EN[6]	0
Bit 4	R/W	RWSEL_EN[5]	0
Bit 3	R/W	RWSEL_EN[4]	0
Bit 2	R/W	RWSEL_EN[3]	0
Bit 1	R/W	RWSEL_EN[2]	0
Bit 0	R/W	RWSEL_EN[1]	0

This register provides RWSEL enable bits for output ports 1 through 16.

RWSEL_EN[16:1]

The receive working select enable bits (RWSEL_EN[16:1]) enable the RWSEL function for ports 16 to 1 respectively. The RWSEL_EN bits are used to enable receive working/protect selection on a per output basis. If RWSEL_EN[I] is logic 1, then the i^{th} port is sensitive to RWSEL and the WPMASK bits are applied to the connection memory settings for that port. If RWSEL_EN[I] is logic 0, then the i^{th} port uses the connection memory settings without modification.

Register: MN00H Port Set #1 - #65 RSEF Control and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved [1]	0
Bit 14	R/W	RSEF_ENB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	DINV	0
Bit 9	R/W	OFAAIS	0
Bit 8	R/W	Reserved [0]	0
Bit 7	R/W	BIP8E	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

The Reserved [1:0] bits should be written to their default value for correct operation of the device.

This register provides control and reports the status of the RSEF block for input port #N.

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic 0 to logic 1 in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the character alignment search character. This bit must be manually set to logic 0 before it can be used again. If the receive DataStream is 8B/10B encoded, invoking the FOCA function will force the RSEF out of frame alignment as well.

Note: The RSEF character aligner can misalign to invalid data due to a floating link or an incorrectly configured upstream device. In most cases when the data becomes valid again, the block will be realign automatically due to detected LCVs. If the condition where the block indicates character alignment but not frame alignment persists once the data stream becomes valid., then the FOCA bit can be used to force realignment.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic 0 to logic 1 in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment framing pattern. This bit must be manually set to logic 0 before it can be used again. If the receive DataStream is not 8B/10B encoded, invoking the FOFA function will force the RSEF out of character alignment as well.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is not in the in-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the generation of the out-of-character-alignment interrupt. When the OCAE bit is set to logic 1, an interrupt is generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set to logic 0, no interrupt is generated as a result of a change of state in the character alignment block.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the generation of the out-of-frame-alignment interrupt. When OFAE is set to logic 1, an interrupt is generated when the character alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set to logic 0, no interrupt is generated as a result of a change in the frame alignment state.

LCVE

The line code violation interrupt enable bit (LCVE) controls the generation of the line code violation interrupt. When LCVE is set to logic 1, an interrupt is generated when a line code violation is detected. When LCVE is set to logic 0, no interrupt is generated as a result of line code violations. Interrupts due to LCVs are masked when LCVE is set low.

The LCVE bit should be set to logic 0 when operating in scrambled NRZ mode to prevent false interrupts from being generated due to line code violations.

BIP8E

The BIP8 interrupt enable bit (BIP8E) controls the generation of the BIP8 error interrupt. When BIP8E is set to logic 1, an interrupt is generated when a BIP8 error is detected. When BIP8E is set to logic 0, no interrupt is generated as a result of BIP8 errors. Interrupts due to BIP8 errors are masked when BIP8E is set low. The BIP8E bit should be set to logic 0 when operating in 8B/10B framing mode to prevent false interrupts due to BIP8 errors from being generated.

OFAAIS

The out-of-frame alignment alarm indication signal (OFAAIS) is set high to force a high-order AIS path alarm if the RSEF is in the out-of-frame alignment state. The AIS character inserted differs with the transmit link format. On scrambled transmit links, if the RSEF is out of frame alignment and OFAAIS is logic 1, all bytes in the constituent STS-1 streams will be overwritten with FFH. On Serial TelecomBus transmit links, if the RSEF is out of frame alignment and OFAAIS is logic 1, all bytes in the constituent STS-1 streams will be overwritten with 0F2H (K28.4-),. No bits are overwritten if OFAAIS is logic 0.

DINV

The parallel incoming data invert bit (DINV) controls the inversion of the incoming DataStream. When DINV is logic 1, the receive data is complemented before character alignment in the RSEF. When DINV is logic 0, the receive data is not modified.

RSEF_ENB

The active-low RSEF enable bit (RSEF_ENB) allows the core logic of the RSEF to be placed into a low power mode. When RSEF_ENB is low, the RSEF core logic and registers operate normally. When RSEF_ENB is high, the RSEF core logic is disabled and placed in a low power mode. In this mode, the RSEF control bits operate normally. All other RSEF register bits should be considered invalid in this mode.

Register: MN01H Port Set #1 - #65 RSEF Interrupt Status and Clock Monitor

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	BIP8I	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3	R	Reserved [1]	X
Bit 2	R	Reserve [0]	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment and detection of line code violations for the RSEF block for input port #N.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE or Register 0009H: Master Interrupt Enable RSEFE bits, the OCAI remains valid and may be polled to detect change of frame alignment events. When WCIMODE is logic 1, an interrupt is cleared immediately following a write of 1 to the interrupt status register bit. When WCIMODE is logic 0, interrupts are cleared immediately following a read of the register. **Note:** the device may toggle in and out of character alignment on a floating 777.6 Mbit/s configured receive link.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs. When the interrupt is masked by the OFAE or Register 0009H: Master Interrupt Enable RSEFE bits, the OFAI remains valid and may be polled to detect change of frame alignment events. When WCIMODE is logic 1, an interrupt is cleared immediately following a write of 1 to the interrupt status register bit. When WCIMODE is logic 0, interrupts are cleared immediately following a read of the register. **Note:** the device may toggle in and out of frame alignment on a floating 777.6 Mbit/s configured receive link.

LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming DataStream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE or Register 0009H: Master Interrupt Enable RSEFE bits, the LCVI remains valid and may be polled to detect change of frame alignment events. When WCIMODE is logic 1, an interrupt is cleared immediately following a write of 1 to the interrupt status register bit. When WCIMODE is logic 0, interrupts are cleared immediately following a read of the register. LCVI is valid only on links carrying 8B/10B encoded data, and should be masked for links carrying non-encoded data

BIP8I

The BIP8 violation event interrupt status bit (BIP8I) reports and acknowledges BIP8 violation interrupts. Interrupts are generated when the BIP8 monitor block detects a BIP8 error in the incoming scrambled DataStream. The RSEF calculates the BIP8 over a frame prior to descrambling and compares that to the value of the descrambled B1 byte for STS-1 # 1 of the following frame. BIP8I is set high when a BIP8 error is detected. When the interrupt is masked by the BIP8E or Register 0009H: Master Interrupt Enable RSEFE bits, the BIP8I remains valid and may be polled to detect BIP8 error events. When WCIMODE is logic 1, an interrupt is cleared immediately following a write of 1 to the interrupt status register bit. When WCIMODE is logic 0, interrupts are cleared immediately following a read of the register. BIP8I is valid only on links carrying scrambled data and should be masked for links carrying 8B/10B encoded data

Register: MN02H Port Set #1 - #65 RSEF LCV and BIP8 Error Count

Bit	Type	Function	Default
Bit 15	R	RSEF_TIP	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	LCVBIP8[7]	X
Bit 6	R	LCVBIP8[6]	X
Bit 5	R	LCVBIP8[5]	X
Bit 4	R	LCVBIP8[4]	X
Bit 3	R	LCVBIP8[3]	X
Bit 2	R	LCVBIP8[2]	X
Bit 1	R	LCVBIP8[1]	X
Bit 0	R	LCVBIP8[0]	X

This register reports the number of detected bit interleaved parity errors and line code violations in the previous accumulation period for the RSEF block for input port #N.

LCVBIP8[7:0]

For Serial TelecomBus configured links, the LCVBIP8[7:0] bits report the number of line code violations that have been detected since the last time the LCV registers were polled. For the scrambled links, the LCVBIP8[7:0] bits report the number of BIP8 errors that have been detected since the last time the LCVBIP8 registers were polled. The BIP8 errors are counted on a block basis; regardless of the number of bits the BIP8 logic detects in error, only one error will be counted. The LCVBIP8 registers are polled by a write to the accumulation trigger register (0001H) or by writing to this register. Either event transfers the internally accumulated error count to the LCVBIP8 registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. Both the RSEF_TIP and TIP register bits will be set to logic 1 while the transfer is in progress and will be set to logic 0 when the transfer is completed. At that time, this register will hold the updated counter value. When the value is transferred, the internal counter is cleared. The error counter will saturate at ‘hFF; it will not wrap around to ‘h00.

RSEF_TIP

The RSEF Transfer In Progress bit (RSEF_TIP) reflects the state of the LCVBIP8 error counter transfer. When RSEF_TIP is high, the transfer of the error counter to the holding register has been initiated but is not complete. When RSEF_TIP becomes low, the value of the error counter is available in the holding register. This bit can be polled after an error counter transfer request to determine if the counter value has been updated.

Note: This bit may be stuck high following reset. If the bit is used, then initiating a normal LCVBIP8 error counter transfer, by writing to either Register 0001H Master Clock Activity and Accumulation Trigger or Register MN02H Port Set #1 - #65 RSEF LCV and BIP8 Error Count will result in the bit being cleared. This action is unnecessary for disabled RSEF blocks.

Register: MN03H Port Set #1 - #65 RSEF Control #2

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	J0MASK	0
Bit 1	R/W	CH_ENB	1
Bit 0	—	Unused	X

This register controls masking of J0 characters for receive channel #N. The register also provides enable control for the ELVDS transmit and receive blocks on channel #N.

CH_ENB

The channel enable bit (CH_ENB) enables the ELVDS transmit and receive blocks for channel #N. The channel is disabled when CH_ENB is logic 1. The channel is enabled when CH_ENB is logic 0. CH_ENB defaults to 1 to minimize power consumption in the device following reset.

J0MASK

The J0 masking bit (J0MASK) enables the removal of K28.5 8B/10B (used to indicate the J0 byte position in the Serial TelecomBus encoded data) characters in the DataStream. J0MASK must be used in conditions where Serial TelecomBus receive data is mapped to Serial TelecomBus transmit links, and either a time slot interchange is being performed on the DataStream or STS-1s from this receive channel is being transmitted with STS-1s from other channels. This is to prevent the K28.5 from being transmitted from the device in a non-J0 byte position. K28.5 characters can be reinserted into the DataStream using the J0 insertion feature in the TSEC to allow framing by downstream devices. When J0MASK is logic 1, K28.5 characters are removed from the DataStream. When J0MASK is logic 0, K28.5 characters remain in the DataStream.

Register: MN04H Port #1 - #65 RSEF Control #3

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	SWAP_INPUTB	1
Bit 12	R/W	Reserved [11]	0
Bit 11	R/W	Reserved [10]	0
Bit 10	R/W	Reserved [9]	0
Bit 9	R/W	Reserved [8]	0
Bit 8	R/W	Reserved [7]	0
Bit 7	R/W	Reserved [6]	0
Bit 6	R/W	LCVP	0
Bit 5	R/W	Reserved [5]	0
Bit 4	R/W	Reserved [4]	0
Bit 3	R/W	Reserved [3]	0
Bit 2	R/W	Reserved [2]	0
Bit 1	R/W	Reserved [1]	0
Bit 0	R/W	Reserved [0]	1

The Reserved [11:0] bits should be written to their default value for correct operation of the device.

This register controls Line Code Violation propagation and input port replication for port #N.

LCVP

The Line Code Violation Propagation bit (LCVP) controls the propagation of line code violations in the DataStream. Line code violations occur on Serial TelecomBus links when an illegal 8B/10B character is received by the RSEF block. If the byte containing the LCV is transmitted on a Serial TelecomBus link, the device can optionally propagate the LCV by inserting an errored 8B/10B character at that position. If LCVP is logic 0, line code violations are not propagated, the value 0FH is inserted in place of the line code violation. If LCVP is logic 1, LCVs are propagated throughout the device, and either illegal 8B10B characters 04BH or 3B4H will be transmitted in the LCV byte position. Regardless of LCVP value, LCV bytes transmitted on scrambled links will be mapped to the 0FH value. Note: an RSEF receiving Serial TelecomBus data, while not aligned, will receive many LCVs. These will be transmitted on downstream Serial TelecomBus links provided LCVP is high.

Note: LCV propagation has the potential to disrupt character and frame alignment in a downstream device, potentially corrupting traffic from other sources. Most applications should not use LCV propagation.

SWAP_INPUTB

The swap input register bit (SWAP_INPUTB) provides input port replication functionality. This will allow a receive channel to receive data from two physical links. Odd channel I will be able to receive data from channel I or I+1. Even channel J will be able to receive data from channel J or J-1. SWAP_INPUTB has no effect for the receive test (65^{th}) port. When SWAP_INPUTB is 1, channel I takes data from physical link I and channel J from physical link J. When SWAP_INPUTB is 0 channel I takes data from physical link I+1 and channel J from physical link J-1. Note: Changing SWAP_INPUTB is an asynchronous event that may result in loss of data.

Register: MN10H Port Set #1 - #65 RTSI Indirect Access Configuration Register

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	RWB	0
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	PAGE	1
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	OTS_IDX[4]	0
Bit 3	R/W	OTS_IDX[3]	0
Bit 2	R/W	OTS_IDX[2]	0
Bit 1	R/W	OTS_IDX[1]	0
Bit 0	R/W	OTS_IDX[0]	0

This register provides the outgoing timeslot number and the control page select used to access the control pages for the RTSI block for input port #N. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is already in progress, as indicated by the BUSY bit.

OTS_IDX[4:0]

The STS-1 outgoing timeslot index (OTS_IDX[4:0]) bits select the word in the control memory corresponding to 2 output timeslots in the DataStream from the RTSI. An OTS_IDX value of *n* selects the connection memory word for timeslots $2*n+1$ and $2*n+2$. The valid and invalid OTS_IDX settings vary with the core timeslot mode. The valid OTS_IDX settings are 0 to 5 when CTSS[1:0] is "00" (core timeslot mode of 12). The valid OTS_IDX settings are 0 to 23 when CTSS[1:0] is "01" (core timeslot mode of 48).

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the RTSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the RTSI Indirect Data register after the BUSY bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the Indirect Data Register or when another write access can be initiated.

Note: This bit may be stuck high following reset. If the bit is used, performing a normal indirect write, by writing to the RTSI Indirect Access Configuration Register will result in the bit being cleared. Allow 150 ns following reset before sampling the BUSY bit. This action is unnecessary for disabled RTSI blocks.

Register: MN11H Port Set #1 - #65 RTSI Indirect Access Data Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	R/W	ETD_SEL[5]	0
Bit 12	R/W	ETD_SEL[4]	0
Bit 11	R/W	ETD_SEL[3]	0
Bit 10	R/W	ETD_SEL[2]	0
Bit 9	R/W	ETD_SEL[1]	0
Bit 8	R/W	ETD_SEL[0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	OTD_SEL[5]	0
Bit 4	R/W	OTD_SEL[4]	0
Bit 3	R/W	OTD_SEL[3]	0
Bit 2	R/W	OTD_SEL[2]	0
Bit 1	R/W	OTD_SEL[1]	0
Bit 0	R/W	OTD_SEL[0]	0

This register contains the data read from the control pages after an indirect read operation or the data to be written to the control pages in an indirect write operation for the RTSI block for input port #N. The data to be written to the control pages must be set up in this register before triggering a write. The RTSI Indirect Data register reflects the last value read or written until the completion of a subsequent indirect read operation. This register cannot be written to when an indirect register access is already in progress, as indicated by the BUSY bit. Note: Prior to any indirect write the RTSI Indirect Access Data register must be written to update its contents, regardless of the data read from it. Note that the used bits in this register default to 0, but words in the control memory do not have any default.

OTD_SEL[5:0]

The Odd Timeslot Data Select (OTD_SEL[5:0]) fields report the input DataStream (RP[*n*]/RN[*n*]) timeslot number read from or written to the control memory. An individual OTD_SEL value represents the input timeslot whose data is placed in the DataStream received by the SSWE, at the output timeslot given by 2 x OTS_IDX + 1. Table 16 shows the valid OTD_SEL values for various operating modes.

ETD_SEL[5:0]

The Even Timeslot Data Select (ETD_SEL[5:0]) fields report the input DataStream (RP[*n*]/RN[*n*]) timeslot number read from or written to the control memory. An individual ETD_SEL value represents the input timeslot whose data is placed in the DataStream received by the SSWE at the output timeslot given by 2 x OTD_IDX + 2. Table 16 shows the valid ETD_SEL values for various operating modes.

Table 16 Ld ETD_SEL, OTD_SEL Values

Core Timeslot Mode	Link Data Format	Valid ETD_SEL, OTD_SEL Values
12	STS-12	1-12
48	STS-12	1,5,9,13,17,21, 25,29,33,37,41,45
	STS-48	1-48

Register: MN12H Port Set #1 - #65 RTSI Configuration Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved [1]	0
Bit 14	R/W	RTSI_ENB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R	ACTIVE	X
Bit 9	R/W	PSEL	0
Bit 8	R/W	Reserved [0]	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	LOAE	0
Bit 1	R/W	FIFOERRE	0
Bit 0	R/W	COAPE	0

The Reserved [1] bit should be written to its default value for correct operation of the device.

The Reserved [0] bit must be set to logic 1 following a hardware or software reset for correct operation of the device. Note that the default value following a device reset is not correct.

COAPE

The change of active page interrupt enable (COAPE) bit controls the generation of change of page interrupt. When the COAPE bit is set to logic 1, an interrupt is generated when the active page changes from page 0 to page 1 or from page 1 to page 0. When COAPE is set to logic 0, no interrupt is generated as a result of a change of page.

FIFOERRE

The FIFO overrun/underrun error interrupt enable (FIFOERRE) bit controls the generation of change of overrun/underrun interrupt. When the FIFOERRE bit is set to logic 1, an interrupt is generated when FIFO underrun/overrun events occur. When FIFOERRE is set to logic 0, no interrupt is generated as a result of a FIFO underrun/overrun event.

LOAE

The loss of alignment interrupt enable (LOAE) bit controls the generation of the loss of alignment interrupt. When the LOAE bit is set to logic 1, an interrupt is generated when a loss of alignment event occurs. When LOAE is set to logic 0, no interrupt is generated as a result of any loss of alignment events that occur.

PSEL

The page select (PSEL) bit is used in the selection of the current active page in connection memory. This bit is logically XORed with the values of the external CMP_A and CMP_B signal to determine which control page is currently active for the respective timing plane. The delay between a PSEL change and the resulting change of page will be greater than 1 and less than 2 frame times.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0, then page 0 is used to reorder timeslots. When this bit is logic 1, then page 1 is used to reorder timeslots.

RTSI_ENB

The active-low RTSI enable bit (RTSI_ENB) allows the logic of the RTSI to be placed into a low power mode. When RTSI_ENB is low, the RTSI logic and registers operate normally. When RTSI_ENB is high, the RTSI logic is disabled and placed in a low power mode. In this mode, the RTSI configuration register bits operate normally, except for the ACTIVE bit which should be considered invalid. All other RTSI register bits should be considered invalid in this mode.

Register: MN13H Port Set #1 - #65 RTSI Interrupt Status Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	LOAI	X
Bit 1	R	FIFOERRI	X
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt statue bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. COAPI is cleared immediately following a read to this register when WCIMODE is logic 0. When WCIMODE is logic 1, COAPI is cleared immediately following a write of logic 1 to this register. COAPI remains valid when the interrupt is not enabled (COAPE or Register 0009H: Master Interrupt Enable RTSIE bits set to logic 0) and may be polled to detect change of active control page events.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. When WCIMODE is logic 1, the interrupt is cleared on a write of logic 1 to the register. When WCIMODE is logic 0, the interrupt is cleared on a read of the register. FIFOERRI remains valid when the interrupt is not enabled (FIFOERRE or Register 0009H: Master Interrupt Enable RTSIE bits set to logic 0) and may be polled to detect change of active control page events.

LOAI

The loss of alignment interrupt indication bit (LOAI) reports a loss of alignment event. A loss of alignment event occurs when the RJ0DLY_A/RJ0DLY_B registers are set such that the J0 byte is not in the FIFO when the data for the outgoing J0 byte position is read from the FIFO. LOAI is set to logic 1 on a loss of alignment event. The loss of alignment event can occur during a change to RJ0DLY or frame pulse position and not necessarily indicate an erroneous RJ0DLY_A/B setting. An erroneous RJ0DLY_A/B setting will result in a LOAI being asserted for every frame. When WCIMODE is logic 1, the interrupt is cleared on a write of logic 1 to the register. When WCIMODE is logic 0, The interrupt is cleared on a read of the register. LOAI remains valid when the interrupt is not enabled (LOAE or Register 0009H: Master Interrupt Enable RTSIE bits set to logic 0) and may be polled to detect change of active control page events.

Register: MN20H Port Set #1 - #65 TTSI Indirect Access Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	PAGE	0
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	OTS_SEL[5]	0
Bit 4	R/W	OTS_SEL[4]	0
Bit 3	R/W	OTS_SEL[3]	0
Bit 2	R/W	OTS_SEL[2]	0
Bit 1	R/W	OTS_SEL[1]	0
Bit 0	R/W	OTS_SEL[0]	0

This register provides the outgoing timeslot number and the control page select used to access the control pages for the TTSI block for output port #N. Writing to this register triggers an indirect register access. This register cannot be written to when an indirect register access is already in progress, as indicated by the BUSY bit.

OTS_SEL[5:0]

The indirect STS-1/STM-0 outgoing timeslot select (OTS_SEL[5:0]) bits indicate the STS-1/STM-0 output time slot accessed in the current indirect access. OTS_SEL represents the timeslot within the outgoing STS-N signal on transmit channel TN[N]/RP[N]. Valid settings depend on the line rate of the associated output port as configured by the STSLR*n*[1:0] bits (register 0002H) . The table below indicates the correspondence between the OTS_SEL value and the logic timeslot.

Note : All output timeslots of the TTSI should be mapped to a valid source/input timeslot for Serial TelecomBus output links.

STSLR*n*	Time Slots	OTS_SEL[5:0]	Timeslot
00	12	000001-001100	#1-12
		000000, 001101-111111	Invalid
01	48	000001 – 110000	#1- #48
		000000, 110001 – 111111	Invalid

PAGE

The page (PAGE) bit selects which control page is accessed in the current indirect transfer. Two pages are defined: page 0 and page 1.

PAGE	Control Page
0	Page 0
1	Page 1

RWB

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the control pages. Writing logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the TTSI Indirect Data register. Writing logic 1 to RWB triggers an indirect read operation. The data read from the control pages is stored in the TTSI Indirect Data register after the BUSY_IND bit has cleared.

BUSY

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set to logic 1 when this register is written, triggering an access. It remains logic 1 until the access is complete at which time it is set to logic 0. This register should be polled to determine when new data is available in the TTSI Control Page Indirect Data register or when another write access can be initiated.

Register: MN21H Port Set #1 - #65 TTSI Indirect Access Data #1

Bit	Type	Function	Default
Bit 15	R/W	MCID[8]	0
Bit 14	R/W	MCID[7]	0
Bit 13	R/W	MCID[6]	0
Bit 12	R/W	MCID[5]	0
Bit 11	R/W	MCID[4]	0
Bit 10	R/W	MCID[3]	0
Bit 9	R/W	MCID[2]	0
Bit 8	R/W	MCID[1]	0
Bit 7	R/W	MCID[0]	0
Bit 6	R/W	TXCHAN_SEL	0
Bit 5	R/W	ITS_SEL[5]	0
Bit 4	R/W	ITS_SEL[4]	0
Bit 3	R/W	ITS_SEL[3]	0
Bit 2	R/W	ITS_SEL[2]	0
Bit 1	R/W	ITS_SEL[1]	0
Bit 0	R/W	ITS_SEL[0]	0

This register support control page access for TTSI #n. The data to be written to the control pages must be set up in this register before triggering a write through the TTSI Indirect Access Configuration register (MN20H). Note: prior to any indirect write, this register must be written to update its contents, regardless of the data read from it. Note that the used bits in this register default to 0, but words in the control memory do not have any default.

ITS_SEL[5:0]

The Input Timeslot Select (ITS_SEL[5:0]) field selects the input timeslot that is used as the data source for the TTSI #n output timeslot selected by OTS_SEL. Valid ITS_SEL values depend on the core timeslot setting as shown in Table 17.

Table 17 Valid ITS_SEL Values

Core Timeslot Setting	Valid ITS_SEL Values
12	1-12
48	1-48

TXCHAN_SEL

The timesliced TX Channel selection bit (TXCHAN_SEL) selects output data from the paired transmit channels when TTSIs are paired and transmit channel multiplexing is enabled (using the SLAVE bit from even TTSI of pair). TXCHAN_SEL will select from the odd TTSI from the pair of TTSIs when set to logic 0. TXCHAN_SEL will select from the even TTSI from the pair of TTSIs when set to logic 1,

MCID[17:0]

The monitored connection identification register bits (MCID[17:0]) are used for per STS-1 CID insertion and monitoring in the SONET stream. The outgoing timeslot which is the target for CID monitoring/insertion is selected by the OTS_SEL bits in TTSI Indirect Access Configuration register (Register MN20H). The MCID represents one of the fields in the CID structure to be inserted into the Z2 bytes when CID insertion is enabled. In CID monitoring, the MCID is compared with the corresponding bits in the incoming CID structure. For a particular STS-1, if the incoming MCID bits fail to match against the MCID in memory then an interrupt is raised. Monitoring cannot be disabled but the interrupt indications that result can be masked.

The remainder of this field is contained in Register MN22H TTSI Indirect Access Data #2 register.

Register: MN22H TTSI Indirect Access Data #2

Bit	Type	Function	Default
Bit 15	R/W	UDCID[5]	0
Bit 14	R/W	UDCID[4]	0
Bit 13	R/W	UDCID[3]	0
Bit 12	R/W	UDCID[2]	0
Bit 11	R/W	UDCID[1]	0
Bit 10	R/W	UDCID[0]	0
Bit 9	R/W	CID_GEN	0
Bit 8	R/W	MCID[17]	0
Bit 7	R/W	MCID[16]	0
Bit 6	R/W	MCID[15]	0
Bit 5	R/W	MCID[14]	0
Bit 4	R/W	MCID[13]	0
Bit 3	R/W	MCID[12]	0
Bit 2	R/W	MCID[11]	0
Bit 1	R/W	MCID[10]	0
Bit 0	R/W	MCID[9]	0

This register support control page access for TTSI #n. The data to be written to the control pages must be set up in this register before triggering a write through the TTSI Indirect Access Configuration register (MN20H). Note: prior to any indirect write the TTSI Indirect Access Data #2 register must be written to update its contents, regardless of the data read from it. Note that the used bits in this register default to 0, but words in the control memory do not have any default.

MCID[17:9]

The monitored connection identification register bits (MCID[17:9]) are part of the MCID[17:0] bits and are explained in the TTSI Indirect Access Data #1 register

CID_GEN

The connection identification generate (CID_GEN) bit is part of the register interface to the connection ID memory inside the TTSI. When CID_GEN is logic 1, the TTSI continuously inserts the CID structure across the Z2 bytes for the timeslot selected by OTS_SEL[5:0] (TTSI Indirect Access Configuration Register MN20H). When CID_GEN is logic 0, CID insertion is disabled and the Z2 byte is passed transparently. The CID structure is shown in Table 18. Bit 7 is the framing bit, it is set to one to indicate the first byte of the CID. Bit 6 is always zeroed. Byte 1 carries the UDCID[5:0] bits. Bytes 2, 3, and 4 carry the MCID[17:0] bits. Bytes 5-8 (in eight byte CID mode) are zeroed. Note that when CID insertion is enabled, CID insertion has higher priority than AIS insertion. CID insertion overwrites the Z2/M1 byte positions

Table 18 CID Structure

CID_MODE	CID Byte	Bits [7:6]	Bits[5:0]
0: Four Byte CID	1	10	UDCID[5:0]
	2	00	MCID[5:0]
	3	00	MCID[11:6]
	4	00	MCID[17:12]
1: Eight Byte CID	1	10	UDCID[5:0]
	2	00	MCID[5:0]
	3	00	MCID[11:6]
	4	00	MCID[17:12]
	5-8	00	00000

UDCID[5:0]

The user defined CID bits (UDCID[5:0]) represent a user defined group of bits within the CID. When CID insertion is enabled, the UDCID value is inserted for bits 5-0 of CID byte 1. The UDCID field is not monitored, but can be captured using the CID capture mechanism.

Register: MN23H Port Set #1 - #65 TTSI Interrupt Enable #1

Bit	Type	Function	Default
Bit 15	R/W	Reserved [4]	0
Bit 14	R/W	TTSI_ENB	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	Reserved [3]	0
Bit 9	R/W	Reserved [2]	0
Bit 8	R/W	Reserved [1]	0
Bit 7	R/W	CID_MODE	0
Bit 6	R/W	SLAVE	0
Bit 5	R	ACTIVE	X
Bit 4	R/W	PSEL	0
Bit 3	R/W	Reserved [0]	0
Bit 2	R/W	CENTER	0
Bit 1	R/W	FAEE	0
Bit 0	R/W	COAPE	0

The Reserved [4:1] bits should be written to their default value for correct operation of the device.

The Reserved [0] bit must be set to logic 1 following a hardware or software reset for correct operation of the device. Note that the default value following a device reset is not correct.

COAPE

The change of active page interrupt enable (COAPE) bit controls the generation of change of page interrupt. When the COAPE bit is set to logic 1, an interrupt is generated whenever the active page changes from page 0 to page 1 or from page 1 to page 0. When COAPE is set to logic 0, there is no change as a result of a change of page.

FAEE

The FIFO alignment error interrupt enable (FAEE) bit controls the generation of the FIFO alignment error interrupt. When the FAEE bit is set to logic 1, an interrupt is generated when the read pointer drifts out of alignment with the write pointer. When FAEE is set to logic 0, there is no change as a result of a FIFO alignment error.

CENTER

The transmit FIFO pointer center (CENTER) bit forces the read pointer to the center location relative to the write pointer for the transmit FIFO. To force a pointer centering operation the user writes a 1 to the CENTER bit. The CENTER bit is a self-clearing register bit that clears to logic 0 once the read pointer has been centered. For proper operation in a CHESS™ system, the CENTER bit must be set to logic 1 after all the CSUs are locked. This is the only way to guarantee that all transmit FIFO depths are within 1 or 2 clock cycles of each other. This is required for frame alignment at the far end.

Note: re-centering the transmit FIFO in an operational system results in movement of the read pointer and can result in temporary data corruption. Subsequent re-center operations on a transmit FIFO after an initial re-center operation can still result in data corruption events.

PSEL

The page select (PSEL) bit is used in the selection of the current active page in connection memory. This bit is logically XORed with the value of the external CMP_A or CMP_B signal, depending on the group the to which the TTSI is assigned to determine which control page is currently active. The delay between a PSEL change and the resulting change of page will be greater than 1 and less than 2 frame times.

ACTIVE

The active page indication (ACTIVE) bit indicates which control page is currently active. When this bit is logic 0, then page 0 is controlling the time switch settings. When this bit is logic 1, then page 1 is controlling the time switch settings. After reset, page 0 is the active page.

SLAVE

The SLAVE enable bit enables the TTSI to be slaved to another TTSI block. This means that master and slave(s) TTSI blocks are all frame synchronous on their transmit interface using the master TTSI as a reference. For example the J0 byte will be emitted by each TTSI in the group on the same clock cycle. This allows for switching of data following the TTSIs. The SLAVE bit must be set to logic 0 for master TTSIs. The SLAVE bit must be set to logic 1 for slave TTSIs. The SLAVE function supports transmit channel multiplexing in which two adjacent transmit channels are paired as the source for a single output port and data is dynamically selected from the two. Transmit channel multiplexing

For transmit channel muxing the odd TTSI (MN odd) is the master (SLAVE logic 0) and the even TTSI (MN+1 even) is the slave (SLAVE logic 1). In this configuration, the TXCHAN_SEL bits of the odd TTSI are used to dynamically select the data source from the paired TTSIs. When this feature is enabled the output of TX[MN+1]/RP[MN+1] should be ignored.

CID_MODE

The Connection ID Mode Select bit (CID_MODE) selects the length of the CID structure. When CID_MODE is logic 0, the CID structure is four bytes in length. When CID_MODE is logic 1, the CID structure is eight bytes in length. The CID structure is defined in Table 18.

TTSI_ENB

The active-low TTSI enable bit (TTSI_ENB) allows the logic of the TTSI to be placed into a low power mode. When TTSI_ENB is low, the TTSI logic and registers operate normally. When TTSI_ENB is high, the TTSI logic is disabled and placed in a low power mode. In this mode, the TTSI Interrupt Enable register bits operate normally, except for the ACTIVE bit, which should be considered invalid. All other TTSI register bits should be considered invalid in this mode.

Register: MN24H Port Set #1 - #65 TTSI Interrupt Enable #2

Bit	Type	Function	Default
Bit 15	R/W	MCIDE[16]	0
Bit 14	R/W	MCIDE[15]	0
Bit 13	R/W	MCIDE[14]	0
Bit 12	R/W	MCIDE[13]	0
Bit 11	R/W	MCIDE[12]	0
Bit 10	R/W	MCIDE[11]	0
Bit 9	R/W	MCIDE[10]	0
Bit 8	R/W	MCIDE[9]	0
Bit 7	R/W	MCIDE[8]	0
Bit 6	R/W	MCIDE[7]	0
Bit 5	R/W	MCIDE[6]	0
Bit 4	R/W	MCIDE[5]	0
Bit 3	R/W	MCIDE[4]	0
Bit 2	R/W	MCIDE[3]	0
Bit 1	R/W	MCIDE[2]	0
Bit 0	R/W	MCIDE[1]	0

MCIDE[16:1]

The CID mismatch interrupt enable (MCIDE) bit controls the generation of the CID mismatch interrupt. When MCIDE[i] is set to logic 1, an interrupt is generated on a CID mismatch with the timeslot #i Z2 bytes. When MCIDE is set to logic 0, no interrupt is generated as a result of a CID mismatch error.

Register: MN25H Port Set #1 - #65 TTSI Interrupt Enable #3

Bit	Type	Function	Default
Bit 15	R/W	MCIDE[32]	0
Bit 14	R/W	MCIDE[31]	0
Bit 13	R/W	MCIDE[30]	0
Bit 12	R/W	MCIDE[29]	0
Bit 11	R/W	MCIDE[28]	0
Bit 10	R/W	MCIDE[27]	0
Bit 9	R/W	MCIDE[26]	0
Bit 8	R/W	MCIDE[25]	0
Bit 7	R/W	MCIDE[24]	0
Bit 6	R/W	MCIDE[23]	0
Bit 5	R/W	MCIDE[22]	0
Bit 4	R/W	MCIDE[21]	0
Bit 3	R/W	MCIDE[20]	0
Bit 2	R/W	MCIDE[19]	0
Bit 1	R/W	MCIDE[18]	0
Bit 0	R/W	MCIDE[17]	0

MCIDE[32:17]

The CID mismatch interrupt enable (MCIDE) bit controls the generation of the CID mismatch interrupt. When MCIDE[i] is set to logic 1, an interrupt is generated on a CID mismatch with the timeslot #i Z2 bytes. When MCIDE is set to logic 0, no interrupt is generated as a result of a CID mismatch error.

Register: MN26H Port Set #1 - #65 TTSI Interrupt Enable #4

Bit	Type	Function	Default
Bit 15	R/W	MCIDE[48]	0
Bit 14	R/W	MCIDE[47]	0
Bit 13	R/W	MCIDE[46]	0
Bit 12	R/W	MCIDE[45]	0
Bit 11	R/W	MCIDE[44]	0
Bit 10	R/W	MCIDE[43]	0
Bit 9	R/W	MCIDE[42]	0
Bit 8	R/W	MCIDE[41]	0
Bit 7	R/W	MCIDE[40]	0
Bit 6	R/W	MCIDE[39]	0
Bit 5	R/W	MCIDE[38]	0
Bit 4	R/W	MCIDE[37]	0
Bit 3	R/W	MCIDE[36]	0
Bit 2	R/W	MCIDE[35]	0
Bit 1	R/W	MCIDE[34]	0
Bit 0	R/W	MCIDE[33]	0

MCIDE[48:33]

The CID mismatch interrupt enable (MCIDE) bit controls the generation of the CID mismatch interrupt. When MCIDE[i] is set to logic 1, an interrupt is generated on a CID mismatch with the timeslot #i Z2 bytes. When MCIDE is set to logic 0, no interrupt is generated as a result of a CID mismatch error.

Register: MN27H Port Set #1 - #65 TTSI Interrupt Status #1

Bit	Type	Function	Default
Bit 15	R	Reserved[2]	X
Bit 14	R	Reserved[1]	X
Bit 13	R	Reserved[0]	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	FAEI	X
Bit 0	R	COAPI	X

COAPI

The change of active page interrupt state bit (COAPI) reports the status of the change of active page interrupt. COAPI is set to logic 1 when the active control page changes from page 0 to page 1 or from page 1 to page 0. When WCIMODE is logic 1, the interrupt is cleared immediately following a write of 1 to the interrupt register bit. When WCIMODE is logic 0, the interrupt is cleared immediately following a read of the register. The interrupt remains valid even when the interrupt is not enabled (COAPE or Register 0009H: Master Interrupt Enable TTSIE bits set to logic 0) and may be polled to detect events.

FAEI

The FIFO alignment error interrupt (FAEI) bit reports the status of the TX FIFO alignment error interrupt. FAEI set to logic 1 indicates that the read pointers and write pointers are too close to one another, This check is performed once per frame when the J0 byte reaches the TX FIFO. In the case of the TX FIFO alignment error, the read pointer then self-aligns to correct for the drift. When WCIMODE is logic 1, the interrupt is cleared immediately following a write of 1 to the interrupt register bit. When WCIMODE is logic 0, the interrupt is cleared immediately following a read of the register. The interrupt remains valid even when the interrupt is not enabled (FAEE or Register 0009H: Master Interrupt Enable TTSIE bits set to logic 0) and may be polled to detect events.

Note: read pointer self-alignment that accompanies the assertion of FAEI will result in the temporary loss/corruption of data. The user can best avoid this through asserting the CENTER bit on system startup.

Register: MN28H Port Set #1 - #65 TTSI Interrupt Status #2

Bit	Type	Function	Default
Bit 15	R	MCIDI[16]	X
Bit 14	R	MCIDI[15]	X
Bit 13	R	MCIDI[14]	X
Bit 12	R	MCIDI[13]	X
Bit 11	R	MCIDI[12]	X
Bit 10	R	MCIDI[11]	X
Bit 9	R	MCIDI[10]	X
Bit 8	R	MCIDI[9]	X
Bit 7	R	MCIDI[8]	X
Bit 6	R	MCIDI[7]	X
Bit 5	R	MCIDI[6]	X
Bit 4	R	MCIDI[5]	X
Bit 3	R	MCIDI[4]	X
Bit 2	R	MCIDI[3]	X
Bit 1	R	MCIDI[2]	X
Bit 0	R	MCIDI[1]	X

MCIDI[16:1]

The CID mismatch interrupt (MCIDI) bit reports the status of the CID monitoring function of the TTSI. A single mismatch of either the framing bit and/or the MCID bits between the expected and received CID structure for timeslot *j* will result in the assertion of the MCIDI[*j*]. Serial TelecomBus and RSEF inserted AIS characters occurring during the timeslot *j* Z2 byte will also result in the assertion of the MCIDI[*j*] bit. Comparison is disabled for 3 (CID_MODE logic 0) or 7 (CID_MODE logic 1) frames following a page switch either through the appropriate CMP_A/CMP_B pins or the PSEL register bit for this TTSI. This allows the monitor to reframe before reporting an error. Using PSEL bits in upstream blocks or devices, or using the RWSEL pin to change control pages will likely result in MCID mismatches. The interrupt is cleared immediately following a read of the register. The interrupt remains valid even when the interrupt is not enabled (MCIDE[16:1] or Register 0009H: Master Interrupt Enable TTSIE bits set to logic 0) and may be polled to detect events.

Register: MN29H Port Set #1 - #65 TTSI Interrupt Status #3

Bit	Type	Function	Default
Bit 15	R	MCIDI[32]	X
Bit 14	R	MCIDI[31]	X
Bit 13	R	MCIDI[30]	X
Bit 12	R	MCIDI[29]	X
Bit 11	R	MCIDI[28]	X
Bit 10	R	MCIDI[27]	X
Bit 9	R	MCIDI[26]	X
Bit 8	R	MCIDI[25]	X
Bit 7	R	MCIDI[24]	X
Bit 6	R	MCIDI[23]	X
Bit 5	R	MCIDI[22]	X
Bit 4	R	MCIDI[21]	X
Bit 3	R	MCIDI[20]	X
Bit 2	R	MCIDI[19]	X
Bit 1	R	MCIDI[18]	X
Bit 0	R	MCIDI[17]	X

MCIDI[32:17]

The CID mismatch interrupt (MCIDI) bit reports the status of the CID monitoring function of the TTSI. A single mismatch of either the framing bit and/or the MCID bits between the expected and received CID structure for timeslot *j* will result in the assertion of the MCIDI[*j*]. Serial TelecomBus and RSEF inserted AIS characters occurring during the timeslot *j* Z2 byte will also result in the assertion of the MCIDI[*j*] bit. Comparison is disabled for 3 (CID_MODE logic 0) or 7 (CID_MODE logic 1) frames following a page switch either through the appropriate CMP_A/CMP_B pins or the PSEL register bit for this TTSI. This allows the monitor to reframe before reporting an error. Using PSEL bits in upstream blocks or devices, or using the RWSEL pin to change control pages will likely result in MCID mismatches. The interrupt is cleared immediately following a read of the register. The interrupt remains valid even when the interrupt is not enabled (MCIDE[32:17] or Register 0009H: Master Interrupt Enable TTSIE bits set to logic 0) and may be polled to detect events.

Register: MN2AH Port Set #1 - #65 TTSI Interrupt Status #4

Bit	Type	Function	Default
Bit 15	R	MCIDI[48]	X
Bit 14	R	MCIDI[47]	X
Bit 13	R	MCIDI[46]	X
Bit 12	R	MCIDI[45]	X
Bit 11	R	MCIDI[44]	X
Bit 10	R	MCIDI[43]	X
Bit 9	R	MCIDI[42]	X
Bit 8	R	MCIDI[41]	X
Bit 7	R	MCIDI[40]	X
Bit 6	R	MCIDI[39]	X
Bit 5	R	MCIDI[38]	X
Bit 4	R	MCIDI[37]	X
Bit 3	R	MCIDI[36]	X
Bit 2	R	MCIDI[35]	X
Bit 1	R	MCIDI[34]	X
Bit 0	R	MCIDI[33]	X

MCIDI[48:33]

The CID mismatch interrupt (MCIDI) bit reports the status of the CID monitoring function of the TTSI. A single mismatch of either the framing bit and/or the MCID bits between the expected and received CID structure for timeslot *j* will result in the assertion of the MCIDI[*j*]. Serial TelecomBus and RSEF inserted AIS characters occurring during the timeslot *j* Z2 byte will also result in the assertion of the MCIDI[*j*] bit. Comparison is disabled for 3 (CID_MODE logic 0) or 7 (CID_MODE logic 1) frames following a page switch either through the appropriate CMP_A/CMP_B pins or the PSEL register bit for this TTSI. This allows the monitor to reframe before reporting an error. Using PSEL bits in upstream blocks or devices, or using the RWSEL pin to change control pages will likely result in MCID mismatches. The interrupt is cleared immediately following a read of the register. The interrupt remains valid even when the interrupt is not enabled (MCIDE[48:33] or Register 0009H: Master Interrupt Enable TTSIE bits set to logic 0) and may be polled to detect events.

Register: MN2BH TTSI Connection ID Capture Register #1

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	CAPCIDV	X
Bit 6	R	BUSY_CID	X
Bit 5	R/W	CID_SEL[5]	0
Bit 4	R/W	CID_SEL[4]	0
Bit 3	R/W	CID_SEL[3]	0
Bit 2	R/W	CID_SEL[2]	0
Bit 1	R/W	CID_SEL[1]	0
Bit 0	R/W	CID_SEL[0]	0

This register controls the CID capture operation. Writing to this register will trigger a CID capture operation. The BUSY_CID should be polled to determine when the capture operation is complete. The register should not be written to while BUSY_CID is high.

CID_SEL[5:0]

The CID select (CID_SEL[5:0]) bits allow the capture of a connection ID structure from the Z2 bytes in the SONET/SDH data stream. The ID to be captured is referenced by its timeslot number which is written to CID_SEL[5:0] to start the capture process.

BUSY_CID

The CID capture busy (BUSY_CID) bit is set to logic 1 when CID_SEL[5:0] is written, triggering a CID capture operation. This bit is reset internally to logic 0 when either the transfer has completed or the transfer operation has been terminated. The CAPCIDV bit will indicate this capture operation status. The result of the capture operation is stored in registers MN2CH and MN2DH.

CAPCIDV

The CID capture status bit (CAPCIDV) indicates whether the last initiated CID capture has completed successfully. CAPCIDV will be read as a logic 1, when the CID capture completes successfully. CAPCIDV will read as logic 0 when the CID capture is abnormally terminated. Abnormal termination of CID capture occurs when either the incoming CID_SEL selected Z2 bytes carry a Serial TelecomBus control character (noted in Table 2) character, or the capture operation times out. The CID capture begins capturing bytes it encounters a Z2 byte with a frame bit of 1. The capture operation will complete 4 frames later. A timer circuit is set with the trigger of the capture operation. Timeout occurs after 7 frames for four byte CID, and 15 frames for 8 byte CID.

Note: If CAPCIDV is set to 1, this does not indicate the contents of CAPCID[31:0] match the expected the CID structure described in Table 18. It merely indicates the device has captured 4 Z2 bytes for the selected timeslot, starting with a Z2 byte with a frame bit of 1.

Register: MN2CH TTSI Connection ID Capture Register #2

Bit	Type	Function	Default
Bit 15	R	CAPCID[15]	0
Bit 14	R	CAPCID[14]	0
Bit 13	R	CAPCID[13]	0
Bit 12	R	CAPCID[12]	0
Bit 11	R	CAPCID[11]	0
Bit 10	R	CAPCID[10]	0
Bit 9	R	CAPCID[9]	0
Bit 8	R	CAPCID[8]	0
Bit 7	R	CAPCID[7]	0
Bit 6	R	CAPCID[6]	0
Bit 5	R	CAPCID[5]	0
Bit 4	R	CAPCID[4]	0
Bit 3	R	CAPCID[3]	0
Bit 2	R	CAPCID[2]	0
Bit 1	R	CAPCID[1]	0
Bit 0	R	CAPCID[0]	0

CAPCID[31:0]

The captured connection ID (CAPCID[31:0]) field holds the result of a connection ID capture process. The process captures the CID for the selected timeslot (CID_SEL) from the Z2 bytes and writes them to CAPCID[31:0]. CID bytes 1, 2, 3, and 4 are written to CAPCID[31:24], CAPCID[23:16], CAPCID[15:8] and CAPCID[7:0] respectively. The remainder of this field is stored in Register MN2DH TTSI Stream Capture Register #3.

Register: MN2DH TTSI Connection ID Capture Register #3

Bit	Type	Function	Default
Bit 15	R	CAPCID[31]	0
Bit 14	R	CAPCID[30]	0
Bit 13	R	CAPCID[29]	0
Bit 12	R	CAPCID[28]	0
Bit 11	R	CAPCID[27]	0
Bit 10	R	CAPCID[26]	0
Bit 9	R	CAPCID[25]	0
Bit 8	R	CAPCID[24]	0
Bit 7	R	CAPCID[23]	0
Bit 6	R	CAPCID[22]	0
Bit 5	R	CAPCID[21]	0
Bit 4	R	CAPCID[20]	0
Bit 3	R	CAPCID[19]	0
Bit 2	R	CAPCID[18]	0
Bit 1	R	CAPCID[17]	0
Bit 0	R	CAPCID[16]	0

CAPCID[31:16]

The captured connection ID (CAPCID[31:0]) field holds the result of a connect ID capture process. The remainder of this field is stored in Register MN2CH TTSI Stream Capture Register #2.

Register: MN30H Port Set #1 - #65 TSEC Control and Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	OD_INV	0
Bit 4	R/W	B1_EN	0
Bit 3	R/W	INV_PRBS	0
Bit 2	R/W	PRBS_EN	0
Bit 1	R/W	J0INS	0
Bit 0	R/W	AINS	0

This register provides control and reports the status of TSEC #*N*.

AINS

The A1/A2 insertion bit (AINS) controls the insertion of valid A1/A2 bytes in the outgoing transport frame on TP[*N*]/TN[*N*]. When AINS is logic 1, the A1/A2 bytes are written with the SONET/SDH specified value of F628 hex. Otherwise the A1/A2 bytes are not affected. A1/A2 insertion must be enabled for A1/A2 error insertion with bits A1ES and A1EC.

J0INS

The J0 byte Insertion bit (J0INS) controls the insertion of the J0 byte in the outgoing transport frame on TP[*N*]/TN[*N*]. When this bit is logic 1, and the link is enabled for 8B/10B encoding, an 8B/10B K28.5 character is inserted at the J0 byte. When J0INS is logic 0, the J0 byte is not overwritten. For most applications, J0 insertion should be enabled for Serial TelecomBus 8B/10B encoded transmit links. This would include any cases where J0 masking is occurring, or the transmit data is sourced from non-Serial TelecomBus links. J0INS must be disabled for non-Serial TelecomBus links.

PRBS_EN

The Pseudo-Random Bit Sequence Enable (PRBS_EN) enables the insertion of a PRBS sequence into the outgoing DataStream. When this bit is logic 1 a PRBS sequence is generated over the outgoing DataStream. When PRBS_EN is logic 0, the PRBS generation is disabled. Only the SONET payload bytes (minus the path overhead and stuff bytes) are overwritten with the PRBS sequence. The outgoing SONET stream is treated as a concatenated stream for the purposes of PRBS generation.

INV_PRBS

The PRBS Invert (INV_PRBS) bit enables the inversion of the PRBS sequence. When this bit is logic 1, the PRBS sequence is inverted. When this bit is logic 0, the PRBS stream is not inverted. Only those bytes carrying SONET/SDH payload bytes are PRBSed, therefore those are the only bytes inverted when INV_PRBS is enabled.

B1_EN

The B1 Enable (B1_EN) bit enables the insertion of the BIP-8 calculated byte from the previous SONET STS-N frame into the B1 position of the first STS-1 of the current SONET STS-N frame. When this bit is logic 1, B1 insertion is enabled. When this bit is logic 0, B1 insertion is disabled. B1 insertion should be disabled for 8B/10B encoded links. When B1 insertion is enabled or disabled – there may be a BIP-8 error on the monitoring device for the first frame following the enable/disable event.

OD_INV

The OD_INV (OD_INV) bit enables the inversion of the outgoing data stream for TP[*N*]/TN[*N*]. When this bit is set high, the outgoing data stream is inverted. When this bit is set low, the outgoing data stream is not inverted.

Register: MN31H Port Set #1 - #65 TSEC Test Pattern

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	A1EC	0
Bit 13	R/W	A1ES	X
Bit 12	R/W	B1ERR	X
Bit 11	R/W	TPS	0
Bit 10	R/W	TPC	0
Bit 9	R/W	TP[9]	0
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	0
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	0
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	0
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	0
Bit 0	R/W	TP[0]	0

This register controls test pattern insertion into DataStream for link #*N*.

TP[9:0]

The Test Pattern registers (TP[9:0]) contain the test pattern that is inserted into the outgoing DataStream on TP[*N*]/TN[*N*], when test pattern insertion is invoked either through the TPS, TPC, or Register MN32H: J0Z0TPINS bits. On 8B/10B configured links, all of TP[9:0] is placed into the output DataStream. On non-encoded links TP[9:8] bits are invalid and only TP[7:0] is placed into the output DataStream. TP[0] is the least significant bit and is the last bit transmitted. Note the recommended TP[7:0] settings in the Register MN32H: J0Z0TPINS bit description when J0/Z0 test pattern insertion is enabled.

TPC

The Test Pattern Continuous (TPC) bit controls continuous test pattern insertion on the outgoing DataStream on TP[*N*]/TN[*N*]. A logic 0 in this bit disables continuous insertion of the test pattern. A logic 1 enables continuous insertion.

TPS

The Test Pattern Single (TPS) bit controls single test pattern insertion on the outgoing DataStream on TP[*N*]/TN[*N*]. A logic 0 to logic 1 transition on the TPS bit results in a single instance of the test pattern stored in TP[9:0] being inserted on the outgoing DataStream. After insertion of the single test pattern on the outgoing DataStream, the TPS bit is cleared and may be re-written with a logic 1 to initiate another single test pattern insertion.

B1ERR

The B1 Error (B1ERR) bit inverts the BIP-8 calculated byte from the previous SONET STS-N frame. A logic 0 to logic 1 transition on this bit enables inversion of the BIP-8 calculated byte that is inserted at the B1 byte position of the current SONET STS-N frame. The B1ERR bit is cleared after inversion of the B1 error byte at which point the B1ERR bit may be re-written to initiate another B1 error. B1 error insertion is valid only when the B1_EN bit is a logic 1. B1ERR will not self clear if B1 byte insertion is not enabled when B1ERR is set. In this case B1ERR must be manually cleared before B1 byte errors can be inserted in the future.

A1ES

The A1/A2 Error Single (A1ES) bit inverts the SONET standard A1 and A2 byte values when they are inserted in the A1 and A2 byte positions. A1/A2 insertion must be enabled for A1ES to take effect. A logic zero to logic one transition on this bit enables inversion of the A1 and A2 bytes for the next SONET STS-N frame. The A1ES bit is cleared after insertion of the inverted A1 and A2 bytes at which point the A1ES bit may be re-written to initiate another A1/A2 error. A1ES will not self clear if A1/A2 byte insertion is not enabled when A1ES is set. In this case A1ES must be manually cleared before A1/A2 byte errors can be inserted in the future.

A1EC

The A1/A2 Error Continuous (A1EC) bit inverts the SONET standard A1 and A2 byte values when they are inserted in the A1 and A2 byte positions. A1/A2 insertion must be enabled for A1EC to take effect. A logic one in this bit enables inversion of the A1 and A2 bytes for all SONET STS-N frames. Writing to the A1ES bit while A1EC is a logic one has no effect, though the A1ES bit will be cleared once the A1 and A2 errors have been inserted on the next SONET STS-N frame. To terminate A1 and A2 continuous error insertion, a logic zero must be written to the A1EC bit.

Register: MN32H Port #1 - #65 TSEC Enable Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	PREEMPH_EN	0
Bit 7	R/W	J0Z0TPINS	0
Bit 6	R/W	Reserved [5]	0
Bit 5	R/W	Reserved [4]	0
Bit 4	R/W	Reserved [3]	1
Bit 3	R/W	Reserved [2]	1
Bit 2	R/W	Reserved [1]	1
Bit 1	R/W	Reserved [0]	0
Bit 0	R/W	TSEC_ENB	0

The Reserved [5:0] bits should be written to their default value for correct operation of the device.

This register provides disable access for the TSEC on link #*N,* J0/Z0 pattern insertion control.

TSEC_ENB

The active-low TSEC enable bit (TSEC_ENB) allows the core logic of the TSEC to be placed into a low power mode. When TSEC_ENB is low, the TSEC core logic and registers operate normally. When TSEC_ENB is high, the TSEC core logic is disabled and placed in a low power mode. In low power mode, the TSEC control bits operate normally. All other TSEC register bits should be considered invalid in low power mode.

J0Z0TPINS

The J0/Z0 pattern insertion bit (J0Z0TPINS) controls the overwriting of the J0/Z0 byte positions in the DataStream with the contents of register MN31H: TP[7:0]. When J0Z0TPINS is logic 0, the J0/Z0 bytes are not overwritten. When J0Z0TPINS is logic 1, the J0/Z0 bytes are overwritten. J0Z0TPINS must be set to the default logic 0 for Serial TelecomBus configured links. J0Z0TPINS should be set to logic 1 for scrambled links to ensure bit transitions in the J0/Z0 byte positions. Additionally, when J0Z0TPINS is logic 1, it is recommended that TP[7:0] be set to CCH or some other transition rich balanced code. For transparent operation in scrambled mode, J0Z0TPINS should be set to logic 0. However, the system designer must ensure that J0/Z0 bytes have transitions.

Note: if AIS insertion during loss of frame alignment is enabled in upstream blocks or devices, it is difficult to guarantee transitions during the J0/Z0 bytes without the use of J0Z0TPINS.

PREEMPH_EN

The PISO pre-emphasis enable bit (PREEMPH_EN) controls symbol pre-emphasis on the Transmit channel #*N*. When pre-emphasis is applied on sequences of contiguous 1s or 0s, the first bit is emphasized to normal levels relative to the successive bits. In pre-emphasis mode, signal is pre-distorted to compensate for jitter introduced on longer channels. When PREEMPH_EN is logic 0, pre-emphasis is disabled on the channel. When PREEMPH_EN is logic 1, pre-emphasis is enabled on the channel. For Normal Operation PREEMPH_EN must be set to logic 0. For Pre-emphasis mode, both the appropriate HICUR bit in Registers 0036H, 003E, 0046H, 004EH and PREEMPH_EN must be set to logic 1. Pre-emphasis mode is intended for 2.488 Gbit/s links only. Use on 777.6 Mbit/s or 622 Mbit/s links is not supported.

Register: MN40H Port Set #1 - #65 PIPM Configuration and Status

Bit	Type	Function	Default
Bit 15	R/W	Reserved[1]	0
Bit 14	R/W	PIPM_EN	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	RESYNC	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	SYNCV	0
Bit 5	R/W	SYNCE	0
Bit 4	R/W	ERRE	0
Bit 3	—	Unused	X
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved[0]	1
Bit 0	R/W	MON_MODE	1

The Reserved[1:0] bits should be written to their default value for correct operation of the device.

This register configures and provides status for the PIPM #*N* PRBS monitor block.

MON_MODE

The monitor mode bit (MON_MODE) determines the operating mode of the PRBS monitor. The two modes are listed in Table 19 and described below.

Table 19 Monitor Modes

Desired Mode	MON_MODE
HPT Encoded SONET/SDH mode	0
Pointer Interpreter SONET/SDH mode	1

In SONET/SDH modes, the incoming data is considered as proper SONET/SDH concatenated frames (STS-12/VC-4-4c, STS-48/VC-4-16c). The PIPM expects that the path overhead and stuff bytes of the incoming transport frame are not overwritten with the PRBS sequence. The SONET/SDH modes differ in determining J1 position and pointer adjustments.

In Pointer Interpreter SONET/SDH mode (MON_MODE is 'b1), a pointer interpreter block will perform high-order pointer processing on the H1 and H2 bytes. This mode is valid for all SONET/SDH data, whether the source is scrambled or is any level of Serial TelecomBus, as long as the H1 and H2 bytes have not been overwritten.

At the High Order Path (HPT) level of Serial TelecomBus mode (MON_MODE is 'b0), control bytes encoded in the DataStream are used, and the pointer interpreter block is bypassed. This mode can only be used if the data was originally encoded as HPT STCB data. Low Order Path Level (LPT) Serial TelecomBus data is not supported since the PIPM is a high-order path PRBS monitor.

INV_PRBS

The invert PRBS bit (INV_PRBS) controls the inversion of the incoming data. When INV_PRBS is set to logic 1, the SONET/SDH payload bytes of the input data is inverted before it is loaded in the LFSR or compared with the expected value. When INV_PRBS is logic 0, the data is used unmodified.

ERRE

The word error interrupt enable bit (ERRE) controls the assertion of word error interrupts by the PIPM. When ERRE is set to logic 1, an interrupt is generated when a word error is detected. Interrupts due to word errors are masked when ERRE is set to logic 0. Note that ERRE only affects the corresponding PIPMI bit; the ERRI bit remains valid at all times.

SYNCE

The synchronization interrupt enable bit (SYNCE) controls the assertion of change of synchronization state interrupts by the PIPM. When SYNCE is set to logic 1, an interrupt is generated when the PRBS monitor synchronizes to the input data and when the PRBS monitor loses synchronization. Interrupts due to a change of synchronization state are masked when SYNCE is set to logic 0. Note that SYNCE only affects the corresponding PIPMI bit; the SYNCI bit remains valid at all times.

SYNCV

The synchronization status bit (SYNCV) indicates whether the PRBS monitor is currently synchronized with the incoming data. SYNCV is set to logic 0 when the monitor is not synchronized. SYNCV is set to logic 1 when the monitor is synchronized.

RESYNC

The resynchronization bit (RESYNC) forces the PRBS monitor to lose synchronization when a transition from logic 0 to logic 1 occurs in this bit. The monitor will then attempt to resynchronize with the incoming data. This bit must be manually set to logic 0 before it can be used again. Note that RESYNC does not hold the monitor in the unsynchronized state.

PIPM_EN

The PIPM enable bit (PIPM_EN) controls the activity of the PIPM and allows for power saving when PRBS monitoring is not required. When PIPM_EN is high, the PRBS monitor and pointer interpreter are active and all PIPM registers work normally. When PIPM_EN is low, the PRBS monitor and pointer interpreter are put into a low power mode. Register accesses to the PIPM block will still be carried out as normal but will have no effect until the block is enabled. As well, all PIPM status bits (SYNCI, ERRI, SYNCV, TIP) should be considered invalid and performance monitor counter transfers are ignored. As well, all status bits should be considered invalid for the first 750 us (i.e. 6 frames) after the PIPM is enabled and cleared by software after that time. Note, all TSEC blocks have their PRBS circuit initialized to the same value following reset, so the user can expect identical PRBS sequences from each TSEC block brought out of reset at the same time.

Register: MN41H Port Set #1 - #65 PIPM Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	SYNCI	0
Bit 4	R	ERRI	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register reports the interrupt status of the PIPM block.

ERRI

The word error interrupt status bit (ERRI) responds to PRBS word errors. Interrupts are generated when the PRBS monitor is synchronized and a word error is detected. ERRI is set to logic 1 when a word error event is detected. When ERRE is set to logic 1, ERRI is included to produce the corresponding interrupt bit (PIPMI). Whether or not the interrupt is masked by the ERRE or Register 0009H: Master Interrupt Enable PIPME bits, the ERRI bit remains valid and may be polled to detect word errors. If WCIMODE is high, the interrupt status bit is cleared when written with a logic 1. If WCIMODE is low, the interrupt status bit is cleared when the register is read.

SYNCI

The synchronization interrupt status bit (SYNCI) responds to changes in the PRBS monitor synchronization state. Interrupts are generated when the monitor gains synchronization with the DataStream or loses synchronization with the DataStream. SYNCI is set to logic 1 when a change of state occurs. When SYNCE is set to logic 1, SYNCI is included to produce the corresponding interrupt bit (PIPMI). Whether or not the interrupt is masked by the SYNCE or Register 0009H: Master Interrupt Enable PIPME bits, the SYNCI bit remains valid and may be polled to detect change of synchronization events. If WCIMODE is high, the interrupt status bit is cleared when written with a logic 1. If WCIMODE is low, the interrupt status bit is cleared when the register is read.

Register: MN42H Port Set #1 - #65 PIPM Error Count

Bit	Type	Function	Default
Bit 15	R	PIPM_TIP	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	ERR_CNT[7]	0
Bit 6	R	ERR_CNT[6]	0
Bit 5	R	ERR_CNT[5]	0
Bit 4	R	ERR_CNT[4]	0
Bit 3	R	ERR_CNT[3]	0
Bit 2	R	ERR_CNT[2]	0
Bit 1	R	ERR_CNT[1]	0
Bit 0	R	ERR_CNT[0]	0

This register is used both to trigger a transfer of the word error counter and to report the transferred counter value.

ERR_CNT[7:0]

The word error count (ERR_CNT[7:0]) is the number of word errors detected by the PRBS monitor. Errors are only accumulated while the monitor is synchronized. If there are multiple errors within one PRBS word (8-bit or 10-bit), only one error is counted. This register is actually a holding register for the error count; the error count must be transferred from the internal counter to this holding register in order to obtain the current value. This transfer is initiated by a write to the accumulation trigger register (0001H) or by writing to this register. Both the PIPM_TIP and TIP registers bit will be set to logic 1 while the transfer is in progress and will be set to logic 0 when the transfer is completed. At that time, this register will hold the updated counter value. When the value is transferred, the internal counter is cleared. The error counter saturates at ‘hFF.

PIPM_TIP

The PIPM Transfer In Progress bit (PIPM_TIP) reflects the state of the ERR_CNT transfer. When PIPM_TIP is high, the transfer of the error counter to the holding register has been initiated, but is not complete. When PIPM_TIP becomes low, the value of the error counter is available in the holding register. This bit can be polled after an error counter transfer request to determine if the counter value has been updated.

Note: The bit may be stuck high following reset. If the bit is used, initiating a normal PRBS error counter transfer, by writing either to Register 0001H Master Clock Activity and Accumulation Trigger or to Register MN42H Port Set #1 - #65 PIPM Error Count will result in the bit being cleared. This action is unnecessary for disabled PIPM blocks.

11 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the device. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[15]) is high.

Test mode registers may also be used for board testing. When all of the blocks within the device are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface.

In addition, the device also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All device inputs may be read and all device outputs may be forced via the JTAG test port.

Table 20 Test Mode Register Memory Map

Address	Register
0000	Master Reset
8000	Master Test
8001	Master Test Mode Address Force Enable
8002	Master Test Mode Address Force Value
8003	Master TMO and Scan
8004	SERDES Glue Scan
8005-801F	Reserved
8030-8037	CSUI #1 Test
8038 – 803F	CSUI #2 Test
8040 – 8047	CSUI #3 Test
8048-804F	CSUI #4 Test
8050-805F	Reserved
8060-806F	SSWE Test
8070-80FF	Reserved
8100-811F	**Port Register Set 1**
8100 – 810F	Port Register Set 1: RSEF Test
8110 – 811F	Port Register Set 1: RTSI Test
8120 – 812F	Port Register Set 1: TTSI Test
8130 – 813F	Port Register Set 1: TSEC Test
8140 – 814F	Port Register Set 1: PIPM Test
8150-81FF	Port Register Set 1: Reserved
8200 – 82FF	**Port Register Set 2**
8300 – 83FF	**Port Register Set 3**

Address	Register
0000	Master Reset
8000	Master Test
8001	Master Test Mode Address Force Enable
8002	Master Test Mode Address Force Value
8003	Master TMO and Scan
8004	SERDES Glue Scan
8005-801F	Reserved
8030-8037	CSUI #1 Test
8038 – 803F	CSUI #2 Test
8040 – 8047	CSUI #3 Test
8048-804F	CSUI #4 Test
8050-805F	Reserved
8400 – 84FF	**Port Register Set 4**
8500 – 85FF	**Port Register Set 5**
8600 – 86FF	**Port Register Set 6**
8700 – 87FF	**Port Register Set 7**
8800 – 8FFF	**Port Register Set 8 – 15**
9000 – BFFF	**Port Register Set 16 – 63**
C000 – C0FF	**Port Register Set 64**
C100 – C1FF	**Port Register Set 65**

11.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register: 8000H Master Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable device test features. All bits, except PMCTST and PMCATST are reset to zero by a reset of the device using the RSTB input. PMCTST and PMCATST are reset when CSB is logic 1. PMCTST and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Access to this register is not affected by the Test Mode Address Force functions in registers 8001H and 8002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the device. When the HIZIO bit is a logic one, all output pins of the device, except the data bus and output TDO, are held tri-state. The microprocessor interface is still active. When the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles but has no effect on write cycles. The HIZDATA bit is over-ridden by the DBCTRL bit.

IOTST

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the device for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and IO TST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the device to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the device for PMC-Sierra's manufacturing tests. When PMCTST is set to logic one, the device microprocessor port becomes the test access port used to run "canned" manufacturing test vectors. The PMCTST bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCTST bit is used to configure the device for PMC-Sierra's analog manufacturing tests. When PMCATST is set to logic one, the device microprocessor port becomes the test access port used to run analog manufacturing test vectors. The PMCATST bit can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Register: 8001H Master Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	TM_A_EN[14]	X
Bit 13	R/W	TM_A_EN[13]	X
Bit 12	R/W	TM_A_EN[12]	X
Bit 11	R/W	TM_A_EN[11]	X
Bit 10	R/W	TM_A_EN[10]	X
Bit 9	R/W	TM_A_EN[9]	X
Bit 8	R/W	TM_A_EN[8]	X
Bit 7	R/W	TM_A_EN[7]	X
Bit 6	R/W	TM_A_EN[6]	X
Bit 5	R/W	TM_A_EN[5]	X
Bit 4	R/W	TM_A_EN[4]	X
Bit 3	R/W	TM_A_EN[3]	X
Bit 1	R/W	TM_A_EN[2]	X
Bit 1	R/W	TM_A_EN[1]	X
Bit 0	R/W	TM_A_EN[0]	X

This register is used to internally force the address, or part of the address, to a certain value. These bits are valid when PMCTST or PMCATST is set to logic 1 and provided A[14:5] is not "0H" (within the device master register address range). The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

TM_A_EN[14:0]

When TM_A_EN[X] is logic 1 and PMCTST or PMCATST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN[14:0] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register: 8002H Master Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	R/W	TM_A[14]	X
Bit 13	R/W	TM_A[13]	X
Bit 12	R/W	TM_A[12]	X
Bit 11	R/W	TM_A[11]	X
Bit 10	R/W	TM_A[10]	X
Bit 9	R/W	TM_A[9]	X
Bit 8	R/W	TM_A[8]	X
Bit 7	R/W	TM_A[7]	X
Bit 6	R/W	TM_A[6]	X
Bit 5	R/W	TM_A[5]	X
Bit 4	R/W	TM_A[4]	X
Bit 3	R/W	TM_A[3]	X
Bit 1	R/W	TM_A[2]	X
Bit 1	R/W	TM_A[1]	X
Bit 0	R/W	TM_A[0]	X

This register is used to force the address pins to a certain value. These bits are valid when PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

TM_A[14:0]

When TM_A_EN[X] is logic 1 and PMCTST or PMCATST is logic 1, the TM_A[X] bit replaces the input pin A[X]. The TM_A[X] bits cannot be reset except by writing a new value to the register.

Register: 8003H Master TM0 and Scan

Bit	Type	Function	Default
Bit 15	R/W	SCAN_SEL[3]	0
Bit 14	R/W	SCAN_SEL[2]	0
Bit 13	R/W	SCAN_SEL[1]	0
Bit 12	R/W	SCAN_SEL[0]	0
Bit 11	R/W	TJ0FP_EN	0
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	TJ0FPA	0
Bit 7	R/W	TJ0FPB	0
Bit 6	R	RJ0FP	X
Bit 5	R	RWSEL_A	X
Bit 4	R	RWSEL_B	X
Bit 3	R	CMP_A	X
Bit 2	R	CMP_B	X
Bit 1	R/W	SCAN_EN	0
Bit 0	R/W	SCLKE	0

This register allows the enabling of PMC-Sierra manufacturing test of the ELVDS digital glue blocks in the device.

SCLKE

The scan clock enable (SCKLKE) selects the SYSCLK as clock input for all blocks in the device. This enables manufacturing testing using a controllable clock. When this bit is high and PMC_TST in register 8000H is high, then the ELVDS digital glue logic is clocked by SYSCLK. When this bit is low OR PMC_TST is low, then the SERDES glue logic is clocked by REFCLK from related the MABC.

SCAN_EN

The scan shift enable bit (SCAN_EN) enables scan testing of the SERDES glue logic blocks. When '1', the scan chains are performing a shift operation. When '0', the scan chains are performing a normal clock operation. This bit is only clearable by a hardware reset.

CMP_B

The CMP_B bit simplifies observability of the CMP_B device ball. The CMP_B bit is the output of the first sampling flop on CMP_B, so the SYSCLK must be toggled before the value at the ball is seen in this bit.

CMP_A

The CMP_A bit simplifies observability of the CMP_A device ball. The CMP_A bit is the output of the first sampling flop on CMP_A, so the SYSCLK must be toggled before the value at the ball is seen in this bit.

RWSEL_B

The RWSEL_B bit simplifies observability of the RWSEL_B device ball. The RWSEL_B bit is the output of the first sampling flop on RWSEL_B, so the SYSCLK must be toggled before the value at the ball is seen in this bit.

RWSEL_A

The RWSEL_A bit simplifies observability of the RWSEL_A device ball. The RWSEL_A bit is the output of the first sampling flop on RWSEL_A, so the SYSCLK must be toggled before the value at the ball is seen in this bit.

RJ0FP

The RJ0FP bit simplifies observability of the RJ0FP device ball. The RJ0FP bit is the output of the first sampling flop on RJ0FP, so the SYSCLK must be toggled before the value at the ball is seen in this bit.

TJ0FPA

The TJ0FPA bit simplifies controllability of the TJ0FPA device ball. The TJ0FPA bit is driven onto the TJ0FPA ball when its test mux is enabled by the TJ0FPE bit. There is no intermediate sampling flop between the TJ0FPA bit and the TJ0FPA ball.

TJ0FPB

The TJ0FPB bit simplifies controllability of the TJ0FPB device ball. The TJ0FPB bit is driven onto the TJ0FPB ball when its test mux is enabled by the TJ0FPE bit. There is no intermediate sampling flop between the TJ0FPB bit and the TJ0FPB ball.

TJ0FP_EN

The transmit J0 frame pulse enable (TJ0FP_EN) selects whether the TJ0FP*n* ball is controlled by the TJ0FP*n* register bit or the regular logic. When TJ0FP_EN is logic 1 and either PMCTST or IOTST are logic 1, the TJ0FP*n* ball is driven by the TJ0FP*n* register bit. When TJ0FP_EN is logic 0, the TJ0FP*n* ball is driven normally as defined by the ball description. TJ0FP_EN is clearable only by a hardware reset.

SCAN_SEL[3:0]

The scan selection bits (SCAN_SEL[3:0]) selects the ELVDS glue block to be scanned. When SCAN_SEL[J] = '1' and the other three SCAN_SEL bits are '0', the ELVDS digital glue logic scan_out on face J is readable in register 8004H. When SCAN_SEL[3:0] = "0000", or more than one bit of SCAN_SEL[3:0] = '1', then register 8004H will read back 0000H.

Register: 8004H Master Scan Data

Bit	Type	Read Function	Write Function	Default
Bit 15	R	SCAN_OUT[15]	SCAN_IN[15]	X
Bit 14	R	SCAN_OUT[14]	SCAN_IN[14]	X
Bit 13	R	SCAN_OUT[13]	SCAN_IN[13]	X
Bit 12	R	SCAN_OUT[12]	SCAN_IN[12]	X
Bit 11	R	SCAN_OUT[11]	SCAN_IN[11]	X
Bit 10	R/W	SCAN_OUT[10]	SCAN_IN[10]	X
Bit 9	R/W	SCAN_OUT[9]	SCAN_IN[9]	X
Bit 8	R/W	SCAN_OUT[8]	SCAN_IN[8]	X
Bit 7	R/W	SCAN_OUT[7]	SCAN_IN[7]	X
Bit 6	R/W	SCAN_OUT[6]	SCAN_IN[6]	X
Bit 5	R/W	SCAN_OUT[5]	SCAN_IN[5]	X
Bit 4	R/W	SCAN_OUT[4]	SCAN_IN[4]	X
Bit 3	R/W	SCAN_OUT[3]	SCAN_IN[3]	X
Bit 2	R/W	SCAN_OUT[2]	SCAN_IN[2]	X
Bit 1	R/W	SCAN_OUT[1]	SCAN_IN[1]	X
Bit 0	R/W	SCAN_OUT[0]	SCAN_IN[0]	X

SCAN_OUT[15:0]

The scan data out (SCAN_OUT[15:0]) bits are the scan output data from the ELVDS digital glue block selected by SCAN_SEL[3:0] in register 8003H.

SCAN_IN[15:0]

The scan data in (SCAN_OUT[15:0]) bits are the scan input data broadcast to the four ELVDS digital glue blocks.

11.2 JTAG Test Port

The TSE JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

Table 21 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 22 Identification Register

Length	32 bits
Version Number	1H
Part Number	5307H
Manufacturer's Identification Code	0CDH
Device Identification	153070CDH

Table 23 Boundary Scan Register Length - 197 bits

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
RX_JTAG_R15	196	IN_CELL	0	RX_JTAG_R37	97	IN_CELL	
RX_JTAG_R13	195	IN_CELL	0	RX_JTAG_R35	96	IN_CELL	
RX_JTAG_R11	194	IN_CELL	0	RX_JTAG_R33	95	IN_CELL	
RX_JTAG_R9	193	IN_CELL	1	TX_JTAG_T47	94	OUT_CELL	
RX_JTAG_R7	192	IN_CELL	0	TX_JTAG_T45	93	OUT_CELL	
RX_JTAG_R5	191	IN_CELL	1	TX_JTAG_T43	92	OUT_CELL	
RX_JTAG_R3	190	IN_CELL	0	TX_JTAG_T41	91	OUT_CELL	
RX_JTAG_R1	189	IN_CELL	1	TX_JTAG_T39	90	OUT_CELL	
TX_JTAG_T15	188	OUT_CELL	0	TX_JTAG_T37	89	OUT_CELL	
TX_JTAG_T13	187	OUT_CELL	0	TX_JTAG_T35	88	OUT_CELL	
TX_JTAG_T11	186	OUT_CELL	1	TX_JTAG_T33	87	OUT_CELL	

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
TX_JTAG_T9	185	OUT_CELL	1	RX_JTAG_R48	86	IN_CELL	
TX_JTAG_T7	184	OUT_CELL	0	RX_JTAG_R46	85	IN_CELL	
TX_JTAG_T5	183	OUT_CELL	0	RX_JTAG_R44	84	IN_CELL	
TX_JTAG_T3	182	OUT_CELL	0	RX_JTAG_R42	83	IN_CELL	
TX_JTAG_T1	181	OUT_CELL	0	RX_JTAG_R40	82	IN_CELL	
RX_JTAG_R16	180	IN_CELL	0	RX_JTAG_R38	81	IN_CELL	
RX_JTAG_R14	179	IN_CELL	1	RX_JTAG_R36	80	IN_CELL	
RX_JTAG_R12	178	IN_CELL	1	RX_JTAG_R34	79	IN_CELL	
RX_JTAG_R10	177	IN_CELL	1	TX_JTAG_T48	78	OUT_CELL	
RX_JTAG_R8	176	IN_CELL	0	TX_JTAG_T46	77	OUT_CELL	
RX_JTAG_R6	175	IN_CELL	0	TX_JTAG_T44	76	OUT_CELL	
RX_JTAG_R4	174	IN_CELL	0	TX_JTAG_T42	75	OUT_CELL	
RX_JTAG_R2	173	IN_CELL	0	TX_JTAG_T40	74	OUT_CELL	
TX_JTAG_T16	172	OUT_CELL	1	TX_JTAG_T38	73	OUT_CELL	
TX_JTAG_T14	171	OUT_CELL	1	TX_JTAG_T36	72	OUT_CELL	
TX_JTAG_T12	170	OUT_CELL	0	TX_JTAG_T34	71	OUT_CELL	
TX_JTAG_T10	169	OUT_CELL	0	OEB_TJ0FPA	70	OUT_CELL	
TX_JTAG_T8	168	OUT_CELL	1	TJ0FPA	69	IO_CELL	
TX_JTAG_T6	167	OUT_CELL	1	CSB	68	IN_CELL	
TX_JTAG_T4	166	OUT_CELL	0	RDB	67	IN_CELL	
TX_JTAG_T2	165	OUT_CELL	1	WRB	66	IN_CELL	
A0	164	IN_CELL		RX_JTAG_R65	65	IN_CELL	
A1	163	IN_CELL		RX_JTAG_R63	64	IN_CELL	
A2	162	IN_CELL		RX_JTAG_R61	63	IN_CELL	
A3	161	IN_CELL		RX_JTAG_R59	62	IN_CELL	
A4	160	IN_CELL		RX_JTAG_R57	61	IN_CELL	
A5	159	IN_CELL		RX_JTAG_R55	60	IN_CELL	
A6	158	IN_CELL		RX_JTAG_R53	59	IN_CELL	
A7	157	IN_CELL		RX_JTAG_R51	58	IN_CELL	
A8	156	IN_CELL		RX_JTAG_R49	57	IN_CELL	
A9	155	IN_CELL		TX_JTAG_T65	56	OUT_CELL	
A10	154	IN_CELL		TX_JTAG_T63	55	OUT_CELL	
A11	153	IN_CELL		TX_JTAG_T61	54	OUT_CELL	
A12	152	IN_CELL		TX_JTAG_T59	53	OUT_CELL	
A13	151	IN_CELL		TX_JTAG_T57	52	OUT_CELL	
A14	150	IN_CELL		TX_JTAG_T55	51	OUT_CELL	
A15	149	IN_CELL		TX_JTAG_T53	50	OUT_CELL	
RX_JTAG_R31	148	IN_CELL		TX_JTAG_T51	49	OUT_CELL	
RX_JTAG_R29	147	IN_CELL		TX_JTAG_T49	48	OUT_CELL	

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
RX_JTAG_R27	146	IN_CELL		RX_JTAG_R64	47	IN_CELL	
RX_JTAG_R25	145	IN_CELL		RX_JTAG_R62	46	IN_CELL	
RX_JTAG_R23	144	IN_CELL		RX_JTAG_R60	45	IN_CELL	
RX_JTAG_R21	143	IN_CELL		RX_JTAG_R58	44	IN_CELL	
RX_JTAG_R19	142	IN_CELL		RX_JTAG_R56	43	IN_CELL	
RX_JTAG_R17	141	IN_CELL		RX_JTAG_R54	42	IN_CELL	
TX_JTAG_T31	140	OUT_CELL		RX_JTAG_R52	41	IN_CELL	
TX_JTAG_T29	139	OUT_CELL		RX_JTAG_R50	40	IN_CELL	
TX_JTAG_T27	138	OUT_CELL		TX_JTAG_T64	39	OUT_CELL	
TX_JTAG_T25	137	OUT_CELL		TX_JTAG_T62	38	OUT_CELL	
TX_JTAG_T23	136	OUT_CELL		TX_JTAG_T60	37	OUT_CELL	
TX_JTAG_T21	135	OUT_CELL		TX_JTAG_T58	36	OUT_CELL	
TX_JTAG_T19	134	OUT_CELL		TX_JTAG_T56	35	OUT_CELL	
TX_JTAG_T17	133	OUT_CELL		TX_JTAG_T54	34	OUT_CELL	
RX_JTAG_R32	132	IN_CELL		TX_JTAG_T52	33	OUT_CELL	
RX_JTAG_R30	131	IN_CELL		TX_JTAG_T50	32	OUT_CELL	
RX_JTAG_R28	130	IN_CELL		OEB_D0	31	OUT_CELL	
RX_JTAG_R26	129	IN_CELL		D0	30	IO_CELL	
RX_JTAG_R24	128	IN_CELL		OEB_D1	29	OUT_CELL	
RX_JTAG_R22	127	IN_CELL		D1	28	IO_CELL	
RX_JTAG_R20	126	IN_CELL		OEB_D2	27	OUT_CELL	
RX_JTAG_R18	125	IN_CELL		D2	26	IO_CELL	
TX_JTAG_T32	124	OUT_CELL		OEB_D3	25	OUT_CELL	
TX_JTAG_T30	123	OUT_CELL		D3	24	IO_CELL	
TX_JTAG_T28	122	OUT_CELL		OEB_D4	23	OUT_CELL	
TX_JTAG_T26	121	OUT_CELL		D4	22	IO_CELL	
TX_JTAG_T24	120	OUT_CELL		OEB_D5	21	OUT_CELL	
TX_JTAG_T22	119	OUT_CELL		D5	20	IO_CELL	
TX_JTAG_T20	118	OUT_CELL		OEB_D6	19	OUT_CELL	
TX_JTAG_T18	117	OUT_CELL		D6	18	IO_CELL	
RWSEL_B	116	IN_CELL		OEB_D7	17	OUT_CELL	
RWSEL_A	115	IN_CELL		D7	16	IO_CELL	
CMP_B	114	IN_CELL		OEB_D8	15	OUT_CELL	
CMP_A	113	IN_CELL		D8	14	IO_CELL	
RJ0FP	112	IN_CELL		OEB_D9	13	OUT_CELL	
OEB_OSYSCLK	111	OUT_CELL		D9	12	IO_CELL	
OSYSCLK	110	IO_CELL		OEB_D10	11	OUT_CELL	
SYSCLK	109	IN_CELL		D10	10	IO_CELL	
RSTB	108	IN_CELL		OEB_D11	9	OUT_CELL	

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
OEB_INTB	107	OUT_CELL		D11	8	IO_CELL	
INTB	106	IO_CELL		OEB_D12	7	OUT_CELL	
ALE	105	IN_CELL		D12	6	IO_CELL	
OEB_TJ0FPB	104	OUT_CELL		OEB_D13	5	OUT_CELL	
TJ0FPB	103	IO_CELL		D13	4	IO_CELL	
RX_JTAG_R47	102	IN_CELL		OEB_D14	3	OUT_CELL	
RX_JTAG_R45	101	IN_CELL		D14	2	IO_CELL	
RX_JTAG_R43	100	IN_CELL		OEB_D15	1	OUT_CELL	
RX_JTAG_R41	99	IN_CELL		D15	0	IO_CELL	
RX_JTAG_R39	98	IN_CELL					

Notes

1. OEB_D[15:0] is the active low output enable for D[15:0].
2. When set high, INTB will be set to high impedance.
3. Register bit 196 is the boundary scan cell closest to TDI (bit 0 is closest to TDO).
4. D15 will be the first bit to appear on TDO when the scan chain is shifted out.

Figure 8 Output Cell (OUT_CELL)

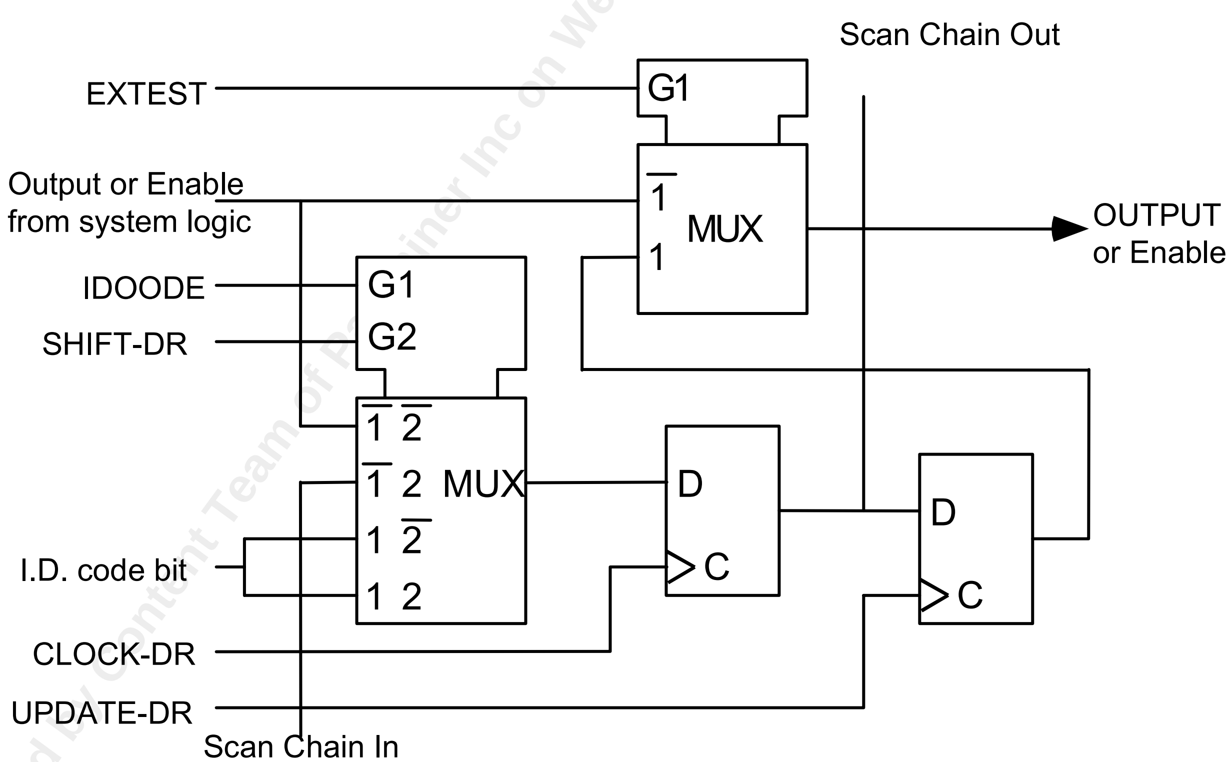
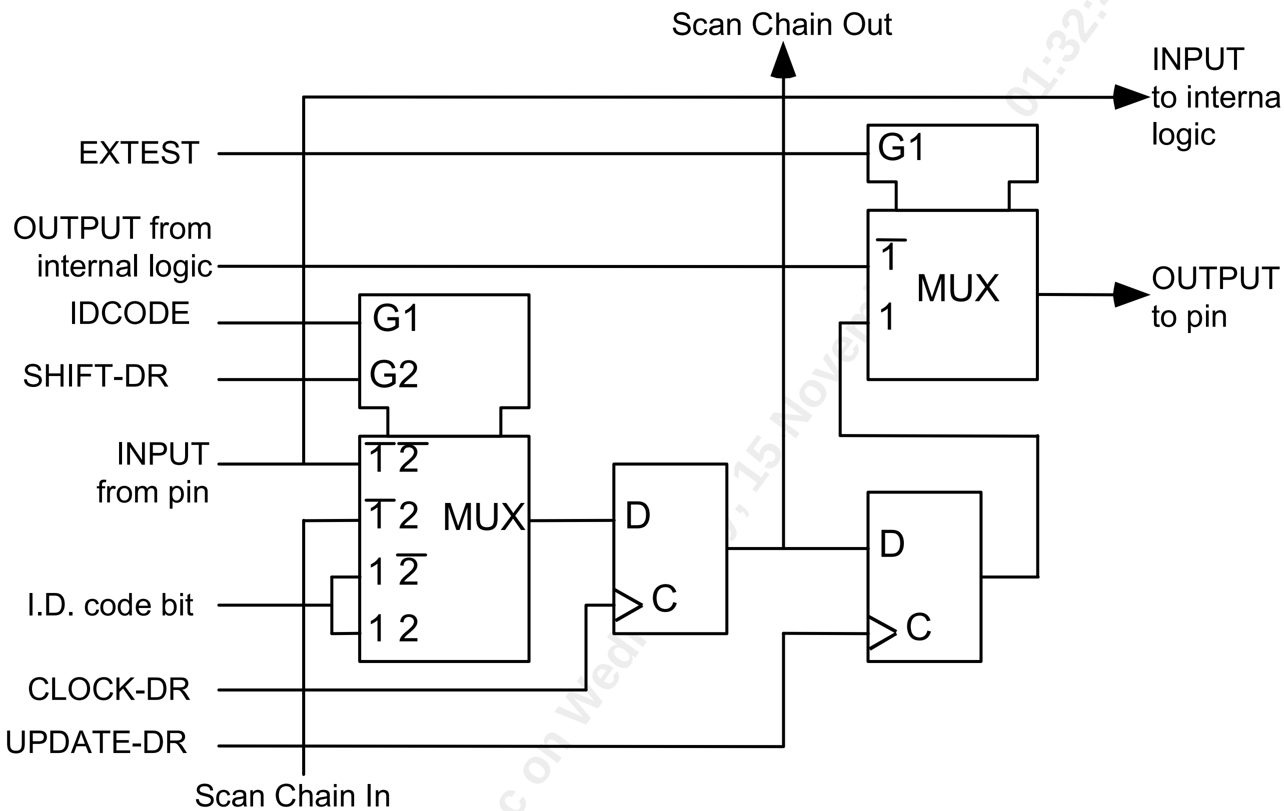


Figure 9 Bidirectional Cell (IO_CELL)



12 Operation

There are several important aspects regarding the operation of device based switch fabrics; these are dealt with in the following sections.

12.1 Initialization Procedure

The device can be configured to perform a wide variety of cross-connect functions. The function is usually system specific and will be set at device power-up by performing register accesses. After initial setup the only additional configuration normally required is for switch settings to be altered. Switch settings will be discussed in a separate section.

12.1.1 General Device Initialization for 65 8B/10B STS-12 Links

By default the device is in a low-power mode of operation at power up, but all registers are still accessible in this state. An appropriate initialization sequence follows but of course other sequences which result in the same end state may be more appropriate for the individual user.

1. Reset the device to put all bits in default state.
2. Write 0000H to register 0006H to power up the entire device. Some users may wish to do this in stages, or perform this step before the previous step to have a more controlled increase in power demand.
3. Write C001H to registers 0033H, 003BH, 0043H, 004BH to allow the CSU to be powered up under master register control.
4. Write the appropriate value to the Master Frame Pulse Delay A/B registers 0007H, 0008H. By default all links belong to group B unless the RGRPASEL, RTPGRPASEL, TGRPASEL and TTGRPASEL register bits are changes from their default.
5. Write 0000H to registers MN03H, where MN ranges between 01H to 41H inclusive, to enable each ELVDS channel.
6. Write 0100H to registers MN12H, where MN ranges between 01H to 41H inclusive.
7. Write 0008H to registers MN23H, where MN ranges between 01H to 41H inclusive.
8. Write 0002H to register MN30H, where MN ranges from 01H to 41H inclusive, to enable K28.5 J0 insertion on transmit links 1-32.
9. Configure the TTSI and RTSI for switching according to Section 12.2.
10. Configure the SSWE for switching according to Section 12.2.

11. Poll PLL lock status bit PLL_LOCKV in registers 0030H, 0038H, 0040H, 0048H CSUI #1 – #4 Interrupt Enable and CSU Lock Status to ensure PLL is locked to reference clock. Read to clear PLL lock indication bit in registers 0031H, 0039H, 0041H, 0049H CSUI #1 - #4 Interrupt Status. Read again to confirm PLL lock status not changing.

12. Write 2000H to register 0003H to force internal frame counter to align to received frame pulse position. Wait until external frame pulse applied. Write 0000H to register 0003H.

13. Write 000CH to register MN23H Port Set #1 - #65 TTSI Interrupt Enable #1 to force centering of the Transmit FIFO, where MN ranges between 01H to 41H inclusive.

The device will now be initialized as a 65 port X 12 Timeslot STS-1 cross-connect. Incoming and outgoing data will be 777.6 Mbit/s 8B/10B encoded. This startup sequence assumes the device:

- Uses a 77.76 MHz frame pulse signal (Register: 0003H Master Configuration #2 R8KCLK)
- Is not externally AC coupled (Register: 0034H, 003CH, 0044H, 004CH CSUI #1 - #4 AC Coupling Control ACCOUPLE[4:0])
- The links are used in low current mode (Register: 0036H, 003E, 0046H, 004EH FACE #1 - #4 Configuration HICUR).

12.1.2 General Device Initialization for 65 SNRZ STS-12 Links

The procedure is the same as outlined in Section 12.1.1, with the following additional steps. These steps can be performed **before** the procedure in Section 12.1.1 if desired.

1. Write 000FH to register 0002H to enable scramble/descramble functions on all links.

2. Write the appropriate value 8608H to Register 0032H, 003AH, 0042H, 004AH to configure the CSU to generate the appropriate link rate clock.

3. Write 0800H to Registers 0036H, 003EH, 0046H, 004EH to configure the device for 8-bits per data-word, instead of 10, at the STS-12 rate.

4. Write 009CH to registers MN32H, where MN ranges between 01H to 41H inclusive, to enable J0/Z0 test pattern insertion to ensure transitions/balance on the J0/Z0 bytes for SNRZ links.

5. Write 00CCH to registers MN31H, where MN ranges between 01H to 41H inclusive, to configure an appropriate pattern for J0/Z0 test pattern insertion..

6. Write 0001H to register MN30H, where MN ranges from 01 to 41H inclusive, to enable A1 A2 insertion.

The device will now be initialized as a 65 port X 12 Timeslot STS-1 cross-connect. Incoming and outgoing data will be 622 Mbit/s SNRZ.

12.1.3 General Device Initialization for TBS 9953 Mode 3 Operation

TBS 9953 Mode 3: Dual TBS (2x(16x777.6) Mbit/s to 2x(2x4x2.488) Gbit/s (W, P)) requires two faces configured for 777.6 Mbit/s 8B/10B operation and 2 faces configured for 2.488 Gbit/s SNRZ operation. Let line interface 1 (16x777) be mapped to face 1, links 1-16. Let line interface 2 be mapped to face 2, links 17-32. Let working interfaces (2x4x2.488) be mapped to face 3, links 33-40, and protect interfaces be mapped to face 3, links 41-48. Face 4 is unused and can be left powered down.

1. Reset the device to put all bits in default state.
2. Write 0008H to register 0006H to power up the entire device. Some users may wish to do this in stages, or perform this step before the previous step to have a more controlled increase in power demand.
3. Write C001H to registers 0033H, 003BH, 0043H to allow the CSU to be powered up under master register control.
4. Write the appropriate value to the Master Frame Pulse Delay A/B registers 0007H, 0008H. RJ0DLY_A is assigned for the line to system side data flow. RJ0DLY_B is assigned for the system to line side data flow.
5. Write 010CH to register 0002H to enable scramble/descramble function, and to set the link rates to STS-48, for face 3.
6. Write 4000H to register 0003H to put the core into 48 core timeslot mode.
7. Write 00FFH to register 0004H to designate line side receive blocks as belonging to timing plane A, and system side receive blocks as belonging to timing plane B.
8. Write FF00H to register 0005H to designate system side transmit blocks as belonging to timing plane A, and line side receive blocks as belonging to timing plane B.
9. Write 0002H to register 0065H to create a working protect mask offset of 8.
10. Write FFFFH to registers 0068H, 0069H to enabled line side ports to switch between working and protect interfaces using the RWSEL pin.
11. Write 0100H to registers MN12H, where MN ranges between 01H to 30H inclusive.
12. Write 0008H to registers MN23H, where MN ranges between 01H to 30H inclusive.
13. Write 009CH to registers MN32H, where MN ranges between 21H to 30H inclusive, to enable J0/Z0 test pattern insertion to ensure transitions/balance on the J0/Z0 bytes for SNRZ links.
14. Write 0C00H to Registers 0046H to configure face 3 of the device for 8-bits per data-word, at the 2.488 Gbit/s rate.

15. Write 0002H to register MN30H, where MN ranges from 01 to 20H inclusive, to enable K28.5 J0 insertion on transmit links 1-32.

16. Write 0001H to register MN30H, where MN ranges from 21 to 30H inclusive, to enable A1 A2 insertion on transmit links 33-48.

17. Write 00CCH to registers MN31H, where MN ranges between 21H to 30H inclusive, to configure an appropriate pattern for J0/Z0 test pattern insertion.

18. Write 0000H to registers MN03H, where MN ranges between 01H to 30H inclusive, to enable each ELVDS channel on faces 1 to 3.

19. Configure to the TTSI, RTSI and SSWE for switching. Refer to Section 12.2.2 for one method to configure these blocks. Keep in mind that for the line side ports of the SSWE, the Working Protect mask of "010", means bit 3 of the connection memory setting will be replaced with the inverse of RWSEL.

14. Poll PLL lock status bit PLL_LOCKV in registers 0030H, 0038H, 0040H CSUI #1 – #4 Interrupt Enable and CSU Lock Status to ensure PLL is locked to reference clock. Read to clear PLL lock indication bit in registers 0031H, 0039H, 0041H, 0049H CSUI #1 - #4 Interrupt Status. Read again to confirm PLL lock status not changing.

20. Write 6000H to register 0003H to force internal frame counter to align to received frame pulse position. Wait until external frame pulse applied. Write 4000H to register 0003H.

21. Write 000C to register MN23H Port Set #1 - #65 TTSI Interrupt Enable #1 to force centering of the Transmit FIFO.

12.2 Initialization of Switch Settings

Each active TTSI and RTSI must be initialized before correct switching can occur. The SSWE must also be initialized.

12.2.1 Simple Pass-Through Switch Settings

Simple Pass-Through ports exists when Incoming Timeslot N Port M maps to Outgoing Timeslot N Port M. Configuring the device such that every port is a simple Pass-Through port is a relatively easy procedure. Every RTSI and TTSI must be placed in Pass-Through mode and the SSWE switch settings must be configured. The procedure is:

1. Initialize the device for operation according to the relevant portion of Section 12.1.

2. Write a '1' to bits 2-5 of register 0003H. For example, if all other bits are at the default value, writing 003CH to register 0003H will put all RTSI and TTSI blocks in pass-through mode. This means that no timeslot interchange will be performed.

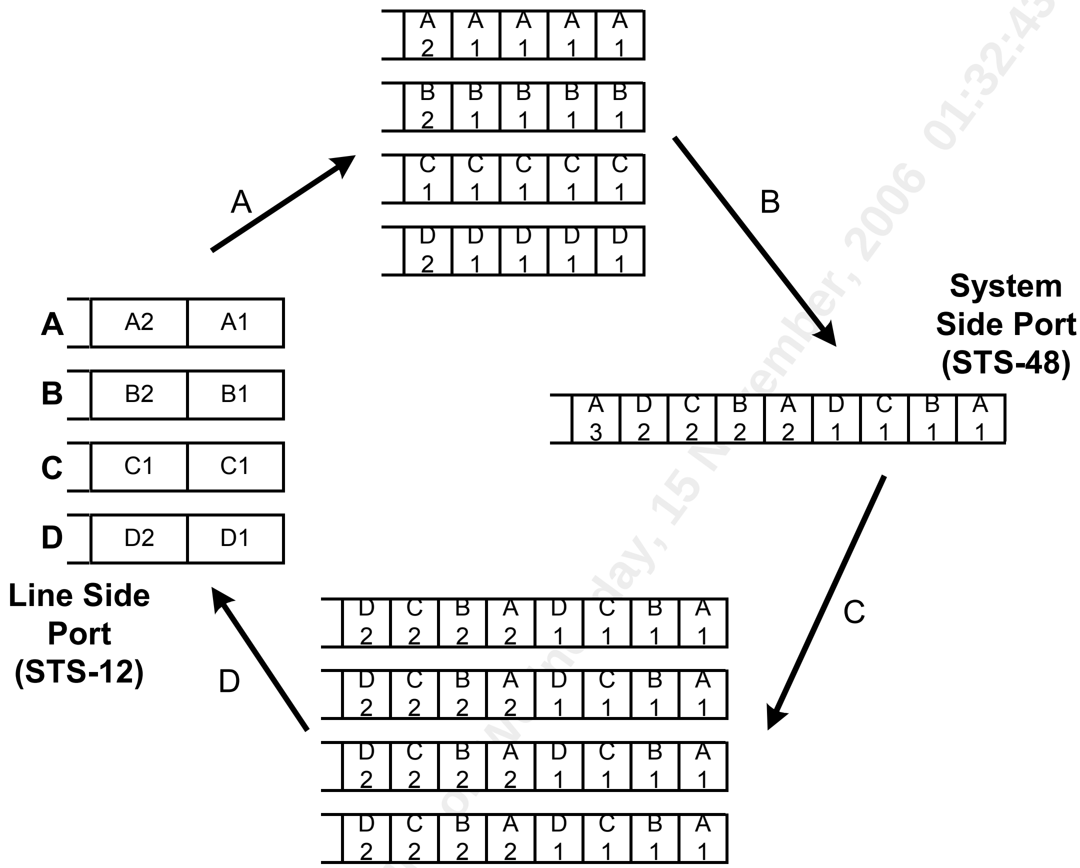
3. To configure the SSWE such that no space switching is done, set each output port to take data from the corresponding input port. The algorithm is:

```
For (I=0..16) {
    Write (4*I+2)<<8 + (4*I+1) to register 0061H
    Write (4*I+4)<<8 + (4*I+3) to register 0062H
    For (J=1..48) {  # assuming 48 timeslots
        Write (J<<7) + I to register 0060H
        Read register 0060H until bit 15 = 0
    }
}
```

12.2.2 TBS 9953 Switch Settings

An approach for the TBS 9953 switch settings to multiplex/demultiplex data between STS-12 line side links and STS-48 system side links is discussed. Figure 10 shows one simplistic way to multiplex/demultiplex data streams together when switching between STS-12 links on the line face and STS-48 links on the system face. The leftmost entity in the figure represents four STS-12 data streams received/transmitted on 4 line side 777.6 Mbit/s or 622.08 Mbit/s links. The rightmost entity in the figure represents a single STS-48 DataStream on the system side received/transmitted on 1 system side 2.488 Gbit/s link..

Figure 10 Timeslot Muxing/Demuxing between STS-12 and STS-48 Links



In the Line Interface (STS-12) to System Interface (STS-48) data flow, the switch blocks settings should be configured as follows:

- RTSI: For all RTSIs on the line interface, they can be uniformly configured to multicast each ingress timeslot to 4 egress timeslots Recall that for core timeslot mode of 48, the ingress timeslots will appear at 1, 5, 9, . . ., 45. For example map timeslot 1 to timeslots 1-4, and ingress timeslot 5 to egress timeslots 5 to 8. This transformation is represented by arrow A in Figure 10.
- SSWE: Four each output port of the SSWE, round robin between the four line interface ports that are being multiplexed. For example, if the line side ports being muxed are ports 1, 2, 3, and 4, then the settings for the system side port for timeslots 1, 2, 3, 4, 5, 6,…,48 would be ports 1, 2, 3, 4, 1 2,…,4 respectively. This transformation is represented by arrow B in Figure 10.
- TTSI: For each TTSI on the System side interface, rearrange timeslots as desired.

In the System Interface (STS-48) to Line Interface (STS-12) data flow, the switch block settings should be configured as follows:

- RTSI: All RTSIs on the line interface can be uniformly configured for passthrough operation (RPASSTHRU_A or RPASSTHRU_B depending which timing plane the system interface RTSIs are designated as), or the switch settings can be configured to mimic passthrough.
- SSWE: The four line side outputs corresponding to the system side input each employ a static setting that copies the data on the system side to the TTSI block. This is represented by arrow C in Figure 10.
- TTSI: Each TTSI is independently configured to select 12 output timeslots from the 48 input timeslots. This is represented by arrow D in Figure 10.

12.3 Interrupt Service Routine

The device will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. The device provides a three level interrupt tree for locating the source of interrupts. This limits the maximum number of register reads to determine the source of an interrupt to seven. To find which condition caused the interrupt or interrupts to occur, follow the procedure outlined below:

1. Read the register 000AH to find which of the functional block groups caused the interrupt. For instance, if the ID_RSEFI bit is asserted, then the interrupt is from one of the RSEF functional blocks. Interrupts may be pending from multiple functional groups at the same time, so more than one bit in register 000AH may be asserted. The bits will stay asserted until all pending interrupts in a functional block group have been cleared.

2. If appropriate, read the Master block Interrupt Source registers to determine which block(s) in the functional group have interrupts pending. This is appropriate for all functional groups except the SSWE as there is only one SSWE.

3. Find the register address space of the corresponding block that caused the interrupt and read its Interrupt Status registers. The Master block Interrupt Source and Master Interrupt Block Identifier register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) cleared.

4. Service the interrupt(s).

5. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 through 4 need to be repeated. Otherwise, no interrupts are pending. Wait for the next assertion of INTB.

12.4 Accessing Indirect Registers

Indirect registers are used to conserve address space in the device. Writing the indirect address register triggers an access to indirect registers.

Separate registers contain the write and read data for the indirect registers. A write to the indirect data register will force future reads to that address to access the contents of the write register. An indirect read operation will force future reads to that address to access the contents of the read register. The contents of the write register at that address are unmodified by an indirect read operation affecting that indirect data register. The user is advised to always write to the indirect data register prior to an indirect write operation if an indirect read operation has occurred since the last indirect read operation to that address.

The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit, or take appropriate steps to clear the BUSY bit. For example, if the clocks are not running, the BUSY bit will not clear.
2. Write the desired configurations for the channel into the indirect data registers.
3. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.
4. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit, or take appropriate steps to clear the BUSY bit. For example, if the clocks are not running, the BUSY bit will not clear.
2. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.
3. Read the BUSY bit. If it is equal to logic 0, continue to step 4. Otherwise, continue polling the BUSY bit.
4. Read the indirect data registers to find the state of the register bits for the selected channel number.

12.5 Low Power Modes Summary

The device provides the capability of powering off unused blocks. Most of the digital blocks can be powered off independently, or on a face basis. The exceptions to this are the SSWE and the CSUI blocks. The ELVDS blocks can also be placed in a low power mode, either on a per channel basis, or on a face basis. Register bit settings for disabling individual blocks and channels are shown in Table 24.

Table 24 Block Low Power Control

Function	Bit	Low Power Setting	Comments
RSEF Enable/Disable	RSEF Control and Status Register MN00H RSEF_ENB	1	Enables/Disables RSEF on channel MN
PIPM Enable/Disable	PIPM Configuration and Status Register MN40H PIPM_EN	0	Enables/Disables PIPM on channel MN
RTSI Enable/Disable	RTSI Configuration Register MN12H RTSI_ENB	1	Enables/Disables RTSI on channel MN
TTSI Enable/Disable	TTSI Interrupt Enable #1 Register MN23H TTSI_ENB	1	Enables/Disables TTSI on channel MN
TSEC Enable/Disable	TSEC Enable Control Register MN32H TSEC_ENB	1	Enables/Disables TSEC on channel MN
ELVDS Channel Enable/Disable	RSEF Control #2 Register MN03H CH_ENB	1	The RSEF, PIPM and RTSI blocks on the associated channel will be partially disabled in this mode. The TTSI and TSEC on the associated channel blocks will not be affected.

Register bit settings for placing a face into a low power mode are shown in Table 25. Essentially, to power down the face, the CSU is placed into 622 mode, and all blocks on the face are disabled. To minimize power consumption caused by enabling all faces, apply the face low power mode settings in the indicated order, clearing the bits POWERDOWN[4:1]=”0000” and setting the bits ELVDS_PWRDNB=“1” as the last step.

Table 25 Low Power Configuration

Register	Face 1 Register Address	Face 2 Register Address	Face 3 Register Address	Face 4 Register Address	Low Power Settings MSB…………LSB
CSUI #1 - #4 Feedback Divider	0032H	003AH	0042H	004AH	1000 0110 0000 1000
CSUI #1 - #4 AC Coupling Control	0034H	003CH	0044H	004CH	0000 0001 0000 0000
Reserved	0035H	003DH	0045H	004DH	0000 0000 0000 0000
FACE #1 - #4 Configuration	0036H	003EH	0046H	004EH	0000 1000 0000 0000
Port Set #1 - #65 RSEF Control and Status Bit 14 (RSEF_ENB)	MN00H, 1<=MN <=10H	MN00H, 11<=MN <=20H	MN00H, 21<=MN <=30H	MN00H, 31<=MN <=41H	1
Port Set #1 - #65 RSEF Control #2 Bit 1	MN03H, 1<=MN	MN03H, 11<=MN	MN03H, 21<=MN	MN03H, 31<=MN	1

Register	Face 1 Register Address	Face 2 Register Address	Face 3 Register Address	Face 4 Register Address	Low Power Settings MSB…………LSB
(CH_ENB)	<=10H	<=20H	<=30H	<=41H	
Port Set #1 - #65 RTSI Configuration Register Bit 14 (RTSI_ENB)	MN12H, 1<=MN <=10H	MN12H, 11<=MN <=20H	MN12H, 21<=MN <=30H	MN12H, 31<=MN <=41H	1
Port Set #1 - #65 TTSI Interrupt Enable #1 Bit 14 (TTSI_ENB)	MN23H, 1<=MN <=10H	MN23H, 11<=MN <=20H	MN23H, 21<=MN <=30H	MN23H, 31<=MN <=41H	1
Port #1 - #65 TSEC Enable Control Bit 0 (TSEC_ENB)	MN32H, 1<=MN <=10H	MN32H, 11<=MN <=20H	MN32H, 21<=MN <=30H	MN32H, 31<=MN <=41H	1
Port Set #1 - #65 PIPM Configuration and Status Bit 14 PIPM_EN	MN40H, 1<=MN <=10H	MN40H, 11<=MN <=20H	MN40H, 21<=MN <=30H	MN40H, 31<=MN <=41H	0
Master Power Control – Register Bits 3-0 (POWERDOWN[4:1])	0006H	0006H	0006H	0006H	0000
CSUI #1 - #4 Control	0033H	003BH	0043H	004BH	1100 0000 0000 0001

Table 26 presents some applications using the block low power bits.

Table 26 Low Power Applications

Application	Block Low Power Bit Settings
Disable unused channel, both digital and analog blocks.	CH_ENB = 1 RSEF_ENB = 1 RTSI=ENB = 1 PIPM_EN = 0 TSEC_ENB = 1
Disable Face x while keeping power to TTSIs (for Connection ID monitoring on standby links)	CH_ENB = 1, for all channels on Face x. RSEF_ENB = 1, for all channels on Face x. RTSI=ENB = 1, for all channels on Face x. PIPM_EN = 0, for all channels on Face x. TSEC_ENB = 1, for all channels on Face x.

12.6 Using the Performance Monitoring Features

The performance monitor counters within the device include the RSEF line code violation/BIP8 error counters. The counters will saturate and not roll over if they reach their maximum value.

A device update of all the counters can be achieved by writing to the device Master Clock Activity and Accumulation Trigger register (0001H). The TIP bit in the device Master Clock Activity and Accumulation Trigger register can be polled to determine when all the counter values have been transferred and are ready to be read.

The accumulated error counts can then be read from registers MN02H and accumulated in software to obtain a long-term count, generate other statistics or take appropriate actions.

12.7 Synchronized Control Setting Changes

The device supports dual switch control settings. These dual settings permit one switch to be operational while the other is updated as a result of new connection requests. The CMPA and CMPB inputs select the current operational switch control settings. CMPA and CMPB are sampled by the device on the base timing pulse *t*. The internal blocks sample the registered CMPA and CMPB value as they receive the next J0 character, at least a delay of RJ0DLY. The new CMP value is applied on the first A1 character of the second following frame. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted.

12.8 Line/Working/Protect/Auxiliary Interface Mapping to Physical Links

In systems that use the RWSEL pin to switch between working and protect interfaces, the board designer should note the limitations on location of the line side and system side working, protect, and auxiliary interfaces with respect to the physical links. The line side interface will usually be located on faces 1 or 2, since those faces are limited to the lower rates. This limitation also constrains the placement of the system side interfaces, if they are operating at 2.488 Gbit/s. The value of the WPMASK[4:2] bits in the SSWE RWSEL Configuration register 0065H determines the size of the working/protect interfaces, and also constrains the mapping of the logical working, protect, and auxiliary interfaces to the physical links. Table 27 shows the possible interface locations for values of the WPMASK[4:2] bits. For a given WPMASK[4:2] setting and working interface location, it provides the base link ID for the protection interface, and a list of base link IDs for an auxiliary interface for a given value of RWSEL. The auxiliary interface location can be selected from one options in the appropriate list.

Note, there is no formal designation of links as part of the working, protect or auxiliary interfaces. This designation is done indirectly through the connection memory settings on the SSWE ports corresponding to line side interface ports. Additionally, if one is going to use the auxiliary interface, this system assumes that the working and protect interface settings are stored in one connection memory page, with the auxiliary interface settings stored in the other page of connection memory. Switching between the working and protect interfaces uses only the RWSEL pin. Switching to the auxiliary interface requires switching memory pages (CMP pin or SSWE PSEL bit) and forcing RWSEL pin to the appropriate value, depending on whether the auxiliary interface is located based on the lists from the RWSEL=0 column, or the RWSEL=1 column.

Table 27 Working/Protect/Auxiliary Interface Location and WPMASK Correspondence

WPMASK[4:2]	Interface Links Count	Working Interface Base Link ID	Protect Interface Base Link ID	Auxiliary Interface Base Link ID (RWSEL=0)	Auxiliary Interface Base Link ID (RWSEL=1)
001	4	1	5	13, 21, 29, 37, 45, 53, 61	9, 17, 25, 33, 41, 49, 57
		9	13	5, 21, 29, 37, 45, 53, 61	1, 17, 25, 33, 41, 49, 57
		17	21	5, 13, 29, 37, 45, 53, 61	1, 9, 25, 33, 41, 49, 57
		25	29	5, 13, 21, 37, 45, 53, 61	1, 9, 17, 33, 41, 49, 57
		33	37	5, 13, 21, 29, 45, 53, 61	1, 9, 17, 25, 41, 49, 57
		41	45	5, 13, 21, 29, 37, 53, 61	1, 9, 17, 25, 33, 49, 57
		49	53	5, 13, 21, 29, 37, 45, 61	1, 9, 17, 25, 33, 41, 57
		57	61	5, 13, 21, 29, 37, 45, 53	1, 9, 17, 25, 33, 41, 49
010	8	1	9	25, 41, 57	17, 33, 49
		17	25	9, 41, 57	1, 33, 49
		33	41	9, 25, 57	1, 17, 49
		49	57	9, 25, 41	1, 17, 33
100	16	1	17	49	33
		33	49	17	1

For example, in the fifth row of Table 27, (Working Link ID of 33) if the user designates links 33-36 as the working interface, and uses a WPMASK[4:2] setting of "001" then the protect interface should be located at links 37-40. The auxiliary interface can be located at any one of the listed base link ids, from the appropriate list.. If the system accesses the auxiliary interface with RWSEL = 1, then the interface can be located starting at either links 1, 9, 17, 25, 41, 49, or 57. If the interface must be 2.488 Gbit/s links, this further limits the interface location start to either links 41, 49, or 57.

In another example, if the device is being used in Mode 5: 2x(16x777.6) Mbit/s to 2x(3x4x2.488) Gbit/s (W, P, A)., then there are two options.

- Option 1 sets WPMASK to "001"
  - Working interface 1: links 33-36, Working interface 2: links 41-44
  - Protect interface 1: links 37-40, Protect interface 2: links 45-48
  - Auxiliary interface 1: links 49-52, Auxiliary interface 2: links 57-60. (RWSEL = 1 to select)
- Option 2 sets WPMASK to "010"

- Working interface: links 33-40
- Protection interfaces: links 41-48
- Auxiliary Interface: links 49-56 (RWSEL = 1 to select)

Note that interface location is only limited if RWSEL is being used to switch between working and protect interfaces. If switching between interfaces is done without the RWSEL pin (through either the CMP pin or PSEL bits), then location of the interfaces is completely arbitrary.

12.9 Connection ID Monitoring

Per STS-1 connection identification insertion and monitoring are supported in the device. Stream id and user defined bits are carried in the connection identification (CID) structure, mapped onto the CID carrier byte: Z2, across multiple SONET frames. An 18-bit monitored stream id (MCID[17:0]) and 6-bit user defined field (UDCID[5:0]) are supported in the CID. The CID for an STS-1 is inserted in that STS-1's Z2 byte across either four or eight frames, depending on the CID mode of operation selected. The CID mode is selectable per TTSI , not per STS-1. CID structure is defined in sections 12.9.1 and 12.9.2. Finally, a capture operation allows the user to capture a designated CID. Only one CID value for a given STS-1 path can be captured at any one time. Interrupts can be used to signal CID mismatches for all STS-1 paths the device monitors.

Table 28 describes the register bits involved in the CID monitoring/insertion function. Per STS-1 CID configuration is done in the TTSI connection memory through indirect access mechanism. The connection memory has pages 0 and 1, the active page being selected by the CMP_A, or CMP_B pins. Similarly, there are two pages of CID settings, so when a switch occurs on the connection memory, the same switch occurs with the CID setting. Page switching via the CMP_A, CMP_B pins temporarily suspends MCID monitoring. Page switching via other means (via PSEL bits or RWSEL pin) will not suspend MCID monitoring and may result in an MCIDI interrupts. Suspension of monitoring is done because CID insertion is not aligned across the system. TTSIs configured for CID insertion are not synchronized in their insertion of the CID into the frames. One TTSI may be inserting the 4th CID byte while another is inserting the 2nd CID byte..

Table 28 Connection ID Insertion/Monitoring Register Bit Summary

Bits	Description
MN22H MCID[17:9] MN23H: MCID[8:0]	The MCID[17:0] bits contain the connection id that are both inserted and monitored.
MN22H: UDCID[5:0]	The UDCID[5:0] bits contain the user defined connection id bits to be inserted.
MN21H: ITS_SEL[5:0]	Determines the incoming timeslot for that TTSI that is to be monitored for a given setting of MCID[17:0]
MN20H:OTS_SEL[5:0]	Determines the outgoing timeslot for which a given CID will be inserted.
MN20H: PAGE	Determines the page for which CID settings being made
MN22H: CID_GEN	Determines whether the CID bits are inserted into the STS-1 stream identified.

Bits	Description
MN24H: MCIDE[16:1] MN25H: MCIDE[32:17] MN26H: MCIDE[48:33]	Interrupt enable for MCID monitoring
MN28H: MCIDI[16:1] MN29H: MCIDI[32:17] MN2AH: MCIDI[48:33]	Interrupt indication for MCID monitoring. MCIDI[n] signals a single mismatch between the incoming MCID and the MCID in memory for STS-1 #n, or a single mismatch in the expected framing bit.
MN2BH: BUSY_CID	Indication that a CID capture operation complete
MN2BH: CID_SEL[5:0]	Selects the STS-1 for the CID capture operation
MN2CH: CAPCID[15:0] MN2DH: CAPCID[31:16]	Results of CID capture operation
MN23H: CID_MODE	Selects between Four (CID_MODE = 0) and Eight (CID_MODE = 1) Byte CIDs.

Note, since CID monitoring is done in the TTSI block, only STS-1s switched through to the outputs timeslots of the TTSI are being monitored. If the system requires the device to monitor CIDs of multiple STS-1s to make its switching decision, consider the following options. If there are unused transmit ports, the STS-1s to be monitored can be mapped to the spare TTSIs corresponding to those ports, and be monitored there. This requires that the face containing the TTSIs be enabled for operation. If insufficient TTSI outputs are available to monitor STS-1s connection ids, software could cycle through the STS-1s to be monitored on the spare TTSI. adjusting switch settings on the fly.

12.9.1 CID Mode 0: Four Byte CID

The structure of the information contained within a four byte CID is shown in Table 29. The most significant bit of each byte is used to identify the position within the CID. Bit 7 for byte 1 is set to logic 1. Bit 7 for the remaining CID bytes shall be 0. The order of insertion of CID bytes onto the carrier bytes will be bytes 1, 2, 3, 4 as shown in the table. Bit 6 of all CID bytes is always zeroed. Bits 5 to 0 carry the MCID and UDCID bits. The MCID bits are carried in CID bytes 2, 3, and 4. The UDCID bits are carried in CID byte 1.

Table 29 Four Frame CID Structure

CID Byte	Bits [7:6]	Bits[5:0]
1	10	UDCID[5:0]
2	00	MCID[5:0]
3	00	MCID[11:6]
4	00	MCID[17:12]

12.9.2 CID Mode 1: Eight Byte CID

The structure of the information contained within a eight byte CID is shown in Table 30. The most significant bit of each byte is used to identify the position within the CID. Bit 7 for frame 1 is set to logic 1. Bit 7 for the remaining CID bytes shall be 0. The order of insertion of CID bytes onto the carrier bytes will be bytes 1, 2, 3, 4, 5, 6, 7, 8 as shown in the table. Bit 6 of all CID bytes is always zeroed. The MCID bits are carried in CID bytes 2, 3, and 4. The UDCID bits are carried in CID byte 1. CID bytes 5-8 are zeroed out.

Table 30 Eight Frame CID Structure

CID Byte	Bits [7:6]	Bits[5:0]
1	10	UDCID[5:0]
2	00	MCID[5:0]
3	00	MCID[11:6]
4	00	MCID[17:12]
5-8	00	00000

12.10 Input Port Replication and Transmit Channel Multiplexing

The device provides the capability to support input time stage duplication and output time stage selection in order to provide enhanced unicast, multicast and multi-chip fabric support.

Under register control, the output of an RSEF may be duplicated to two adjacent RTSI's. Similarly, under register control, the output of two adjacent TTSI's can be used to feed a single TSEC under mux control to select the desired output. When both input and output modes are enabled, the device has an internal 2x speedup, to provide non-rearranging unicast or enhanced multicast capabilities.

In a 3-stage multi-chip fabric, enhanced switching capabilities are provided by running in asymmetric modes for the first and third stages. In the first stage, input duplication can be provided for a 2x fanout to the second stage of chips. In the third stage, the reduction back to 1x an be performed with output muxing. This provides additional flexibility for space stage scheduling in the first and third stages of the fabric.

See PMC-2010892 TSE 160/TBS9953 System Architectures And Algorithms For Multicast Applications for a discussion of the capabilities provided by these modes.

12.11 Indirect Access Operation Duration

Table 31 shows the duration of the indirect access operations for the blocks that support those operations. Rather than polling the BUSY register bit of a block to determine when an indirect access operation in that block has completed, software can use the delays in this table to determine when that operation has completed. The BUSY Clear time represents the delay from the writing of an indirect access configuration register (0060H SSWE Indirect Access Configuration, MN10H RTSI Indirect Access Configuration, MN20H TTSI Indirect Access Configuration, to when the indirect access has completed, and BUSY bit cleared. Note for the RTSI and SSWE blocks, the operation duration depends on the core timeslot mode, while the operation duration for the TTSI block depends on the line rate.

Table 31 Indirect Access Operation Duration

Operation	Line Rate (Gbit/s)	Core Timeslot Mode	Busy Clear Time (ns)
RTSI Access	X	12	257.2
RTSI Access	X	48	64.3

Operation	Line Rate (Gbit/s)	Core Timeslot Mode	Busy Clear Time (ns)
SSWE Access	X	12	360.1
SSWE Access	X	48	90.0
TTSI Read	.7776 or .622	X	360.1
TTSI Read	2.488	X	205.8
TTSI Write	.7776 or .622	X	128.6
TTSI Write	2.488	X	32.15

Table 32 shows the duration of the other operations supported by BUSY/TIP bits. Rather than polling the BUSY register bit of a block to determine when the operation in that block has completed, software can use the delays in this table to determine when that operation has completed. The clear time represents the delay invoking the operation, to when the operation has completed, and BUSY bit cleared.

Table 32 Other BUSY/TIP Operation Duration

Operation	Bit Clear Time
TTSI BUSY_CID (4 byte CID)	1.0 ms
TTSI BUSY_CID (8 byte CID)	1.5 ms
TIP	100 ns
RSEF_TIP	100 ns
PIPM_TIP	100 ns
TSEC A1ES	250 us
TSEC B1ERR	250 us
TTSI CENTER	250 us

12.12 Device Functional Considerations

This section lists functional considerations for the production release of the TBS-9953 device as of the publication date of this document. For each item, the operating constraints and recommended configurations of the device are described.

12.12.1 Random Line Code Violation Counts on Unprovisioned 777 Mbit/s Timeslots

Description

STS-1 timeslots that are not provisioned (i.e.: an output timeslot not configured to accept data from an input timeslot) will carry random data. It is probable that this random data will eventually produce an invalid 8B/10B character, resulting in a Line Code Violation (LCV) being indicated in downstream devices, such as the PM5317 SPECTRA 9953 and will accumulate for these timeslots. LCVs can cause a downstream receiver to declare OFA and corrupt any valid data on provisioned STS-1 timeslots.

Recommended Configuration

To avoid LCVs reported in downstream devices when using 8B/10B 777Mb/s links, ensure that all STS-1 timeslots are provisioned. Any STS-1 outputs that are not required to carry live traffic should be configured to carry traffic from an enabled receive channel. The enabled receive channel may or may not be connected to a traffic source. Additionally, the RSEF on the selected channel must be configured with J0 masking enabled (J0MASK bit = 1 in MN03H Port Set #1 - #65 RSEF Control #2 register) and LCV propagation disabled (LCVP bit = 0 in MN04H Port #1 - #65 RSEF Control #3 register). This prevents spurious J0s or LCVs present in the data from floating links from disrupting downstream framing.

This is implemented by configuring the RTSI, SSWE, and TTSI connection memory such that any unprovisioned egress timeslots source data from an enabled receive channel. An enabled receive channel is defined as:

a. A receive channel on a face that is powered up and not reset (POWERDOWN[i] = 0 in 0006H Master Power Control register, FACE_RESET[i] = 0, DBLOCK_RESET = 0, DRESET = 0 in 0000H Master Reset register)

b. The analog blocks on that face are powered up and not reset (ARESET = 0 in 0000H Master Reset register , ELVDS_PWRDNB = 1, ELVDS_RSTB = 1 in 0033H, 003BH, 0043H, 004BH CSUI #1 - #4 Control register)

c. The RXLV and DRU analog blocks for that particular channel are enabled (CH_ENB = 0 in MN03H Port Set #1 - #65 RSEF Control #2 register)

d. The RSEF and RTSI digital blocks for that particular channel are powered up (RSEF_ENB = 0 in MN00H Port Set #1 - #65 RSEF Control and Status register, RTSI_ENB = 0 in MN12H Port Set #1 - #65 RTSI Configuration Register)

12.12.2 OFAAIS Data Corruption On STS-12 And STS-48 Scrambled Links

Description

The RSEF block supports the ability to force an all-ones pattern over all bytes of a received data stream when a link goes out of frame alignment (OFAV). A link will go out of frame alignment when a receive link is floating, or the connection experiences excessive bit errors. The feature is enabled via the OFAAIS bit in the MN00H Port Set #1 - #65 RSEF Control and Status register.

When a sufficient number of STS-1 timeslots from links which have triggered the OFAAIS feature are cross connected to a SONET scrambled link, the all-ones pattern in the resultant transmit data stream can cause data recovery errors. As a result, downstream receiver blocks can declare invalid OFAV. Valid STS-1 paths on the STS-48 link can be corrupted.

The problem can arise in the A1, A2, and J0/Z0 byte positions, because in accordance with SONET scrambling, these bytes are not scrambled.

Recommended Configuration

The J0Z0TPINS bit set to 1 in the MN32H Port #1 - #65 TSEC Enable Control register combined with the recommended setting of CCh in the TP[7:0] bit positions in the MN31H Port Set #1 - #65 TSEC Test Pattern register will ensure sufficient transition density in the J0/Z0 positions. Setting the AINS bit to 1 in the MN30H Port Set #1 - #65 TSEC Control and Status register will overwrite the A1 and A2 byte positions with the standard F6H and 28H values respectively, ensuring transition density in those byte positions.

12.12.3 Data Recovery On SONET Scrambled Links

Description

The TBS 9953 can be configured with 4 faces supporting either STS-12 (all faces) or STS-48 (faces 3 and 4) SONET scrambled links. For data received and transmitted on faces of the TBS 9953 configured for SONET scrambled mode, link failure conditions at the TBS 9953 receiver can be improperly propagated to downstream receivers. Such conditions include received SONET scrambled data that has poor DC balance or poor transition density due to a failed transmitter or a floating link. It is expected that such data streams will cause the receiver block (RSEF) to declare out of frame alignment (OFA) after 4 frames and overwrite the receive data with the AIS all-ones pattern. AIS insertion is controlled via the OFAAIS bit in the MN00H Port Set #1 - #65 RSEF Control and Status register and should be set. Until OFA is declared, the data stream can be duplicated on a transmit serial interface of the TBS 9953 provided the STS-1 timeslot mapping is preserved from the receive side to the transmit side. The degree of duplication depends on the degree that STS-1 timeslot positions are preserved. The result is that a downstream RSEF may declare OFA even though the transmit link inserts valid A1/A2 framing bytes. STS-1s from valid TBS 9953 receive links cross-connected in with a majority of STS-1s from a failing TBS 9953 receive link may be affected.

The re-transmission of poor DC balanced or poor transition density serial data occurs when the STS-1 sequence presented to the de-scrambler on the receive side is maintained and sent to the scrambler on a transmit link. Due to the SONET scrambling algorithm, the XOR of the scrambling sequence with the data stream applied twice (once by the de-scrambler, once by the scrambler) at the exact same bit positions will re-create the initial serial data stream.

Recommended Configuration

If the STS-1 sequence is sufficiently altered between the de-scrambler and scrambler , the bit sequence generated at the TBS 9953 transmitter will have acceptable transition density and DC balance. This can be accomplished by re-ordering the STS-1 timeslots of the receive data using the RTSI or TTSI blocks of the TBS 9953. The following rule will prevent the propagation of problem data streams downstream:

1) For every STS-1 path received at the TBS 9953, ensure that the transmit time-slot for a given STS-1 path is not the same as the receive time-slot for the same STS-1 path.

In applications where the TBS 9953 is entirely using 8B/10B encoded links or when 8B/10B receive links are internally cross-connected to SONET scrambled transmit links (or vice versa), this issue is not applicable due to 8B/10B encoding that ensures transition density and DC balance.

12.12.4 Floating 8B/10B Link Frame Alignment Status

Description

The RSEF block can go in and out of frame alignment (OFAI toggling) on floating receive links configured for STS-12 8B/10B encoded data streams. As a result of OFAI toggling, the OFAAIS feature used to insert an all-ones pattern over all bytes of a link will toggle between enabling and disabling the all-ones pattern insertion. When all-ones is not inserted on the data stream, the data transmitted from a floating RSEF block will be random.

When 8B/10B receive links are unused, they should be disabled via the CH_ENB bit in the MN03H Port Set #1 - #65 RSEF Control #2 register. For hot-swap applications where 8B/10B encoded links can transition from connected to floating state, the system must take into account the possible transitioning between all-ones and random data content in the STS-1 paths transmitted from the floating link.

Recommended Configuration

For applications where floating receive 8B/10B encoded links are connected to transmit 8B/10B encoded links, the J0MASK bit in register MN03H Port Set #1 - #65 RSEF Control #2 and J0INS bit in register MN30H Port Set #1 - #65 TSEC Control and Status must be set to 1. This will prevent the propagation of invalid 8B/10B K28.5 J0 characters to downstream RSEF/8B/10B framer blocks. Downstream pointer interpreter blocks will be expected to toggle declaration of PAIS and LOP for STS-1 paths sourced from floating RSEF blocks.

12.12.5 Constant OFAV Status At 8B/10B Receiver

Description

The STS-12 8B/10B configured links can falsely character align (i.e. establish 10 bit word boundaries) to the receive DataStream when the far end transmitter is disabled or the receive link is floating. When the transmitter turns on or is connected, the receiver begins to receive valid data from a transmitter. The transmit stream may not contain sufficient LCVs based on the current character alignment to cause an out of character alignment (OCA) alarm. As a result, the RSEF block will not be able to correctly frame align to the receive data stream and data corruption will occur.

Recommended Configuration

This behavior is present when the following conditions at the RSEF block persist for more than two receptions of the K28.5 J0 control character from an STS-12 8B/10B configured transmitter.

Register MN00H Port Set #1 - #65 RSEF Control and Status

OFAV = 1

OCAV = 0

Register MN01H Port Set #1 - #65 RSEF Interrupt Status and Clock Monitor (Status after second read after reception of two J0 characters)

OFAI = 0

OCAI = 0

If one K28.5 J0 control character is sent per frame, the minimum wait period is 250 µs. For example, the J0INS bit in register MN30H Port Set #1 - #65 TSEC Control and Status will ensure that one J0 character is transmitted per frame.

If the above conditions are detected, the FOCA bit in the MN00H Port Set #1 - #65 RSEF Control and Status register should be set and cleared to force the RSEF block to re-character align to the receive DataStream.

12.12.6 Removal From Power-Down Mode on Device Power-Up

Description

An updated face low power mode must be used for the device. On reset or power-up of the device, the default state of the four faces of the device are in power-down mode and most of the digital and analog circuitry is disabled. This default state must be avoided for proper operation of the device by setting the device (described below) into normal operating mode and using the updated low power mode as appropriate.

Recommended Configuration

Remove the device from the default power-down mode immediately following power-up and immediately following device reset. To do this, the POWERDOWN[4:1] bits in the Master Power Control Register 0006H should be set to zero (POWERDOWN[4:1]=”0000”) and the ELVDS_PWRDNB bit in the CSUI #1 - #4 Control Registers 0033H, 003BH, 0043H, 004BH should each be set to one (ELVDS_PWRDNB=“1”).

The user can use the updated register settings to reduce power on unused faces after device power up. Register settings to enable this mode are found in Table 35. The table indicates the register addresses appropriate for powering down each face.

12.12.7 Performance Meter Register TIP Bits Default Unknown Reset

Description

The TIP, PIPM_TIP and RSEF_TIP bits default following either a software or hardware reset is unknown as opposed to logic 0. Given that when these TIP bits are high they should indicate that a performance meter register transfer is in progress, the user may mistakenly infer that a transfer is occurring following the reset., when this is not the case. This is only an issue following reset. If the user refers to the TIP bits to determine when performance meter register transfers are complete, they should use the recommended configuration.

Recommended Configuration

To ensure that the TIP bits are restored to the standby value before normal operation starts, the user should initiate a normal performance meter register transfer, by writing to Register 0001H Master Clock Activity and Accumulation Trigger, which will result in the bit being cleared.

The bits can also be individually cleared by writing the specific register for enabled blocks. For the RSEF_TIP bit in enabled RSEF blocks, initiating a normal LCVBIP8 error counter transfer, by writing to Register MN02H Port Set #1 - #65 RSEF LCV and BIP8 Error Count will result in the bit being cleared. Only poll the RSEF_TIP bit if the corresponding RSEF is enabled.

For the PIPM_TIP bit in enabled PIPM blocks, initiating a normal PRBS error counter transfer, by writing to Register MN42H Port Set #1 - #65 PIPM Error Count will result in the bit being cleared. Only poll the PIPM_TIP bit if the corresponding PIPM is enabled.

12.12.8 RSTI BUSY Bit Default Unknown Following ResetDescription

The RSTI BUSY bits default following either a software or hardware reset is unknown as opposed to logic 0. Given that when these BUSY bits are high they should indicate that a indirect access is in progress, the user may mistakenly infer that a indirect access is occurring following the reset., when this is not the case. This is only an issue following reset. If the user refers to the BUSY bits to determine when performance meter register transfers are complete, they should use the recommended configuration.

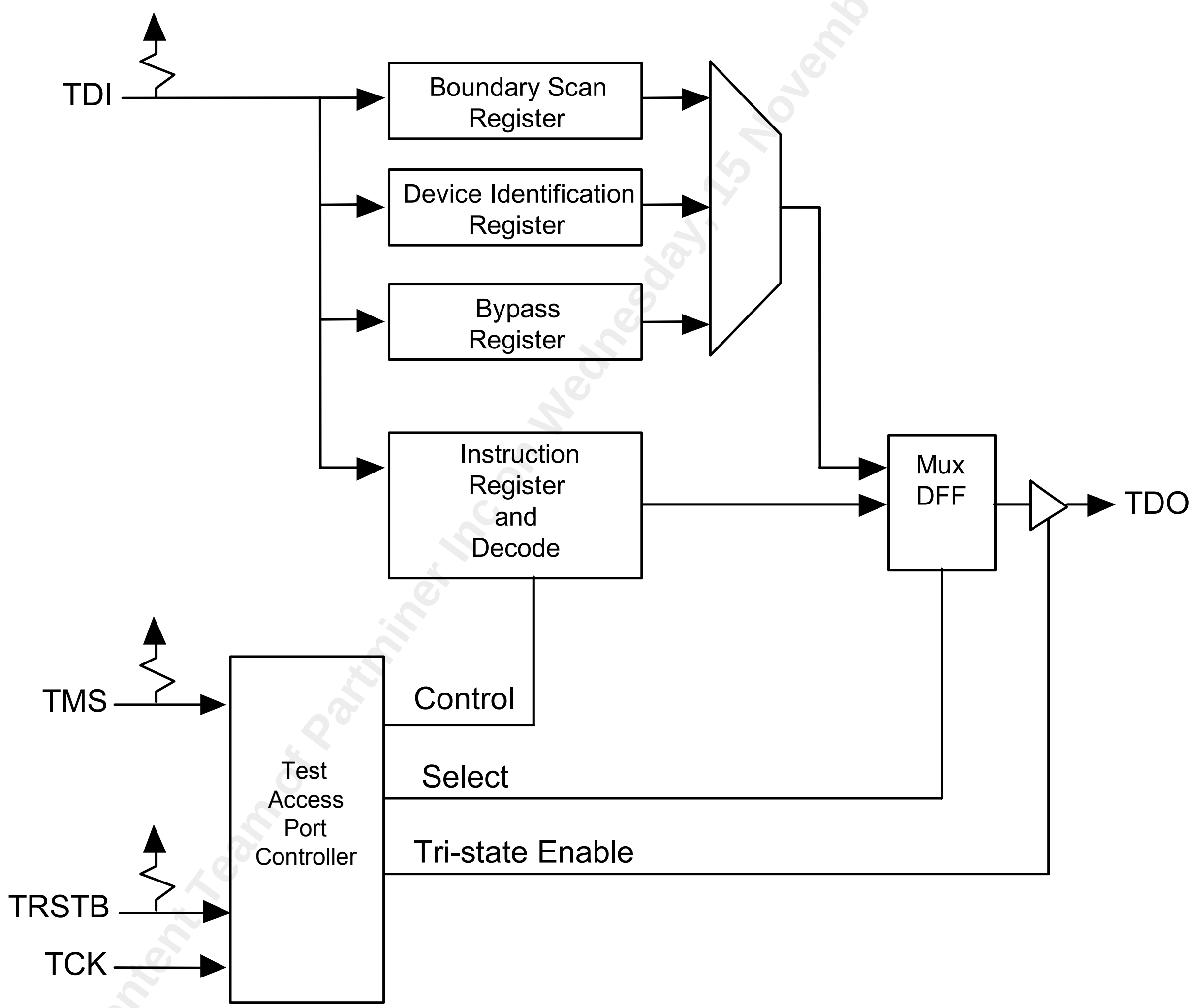
Recommended Configuration

To ensure that the BUSY bits are restored to the standby value before normal operation starts, the user should initiate a normal indirect access in all enabled RTSI blocks, by writing to the RTSI Indirect Access Configuration Registers. This will result in the bit being cleared according to the normal indirect access duration.

12.13 JTAG Support

The device supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO, used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI, and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is in Figure 11.

Figure 11 Boundary Scan Architecture



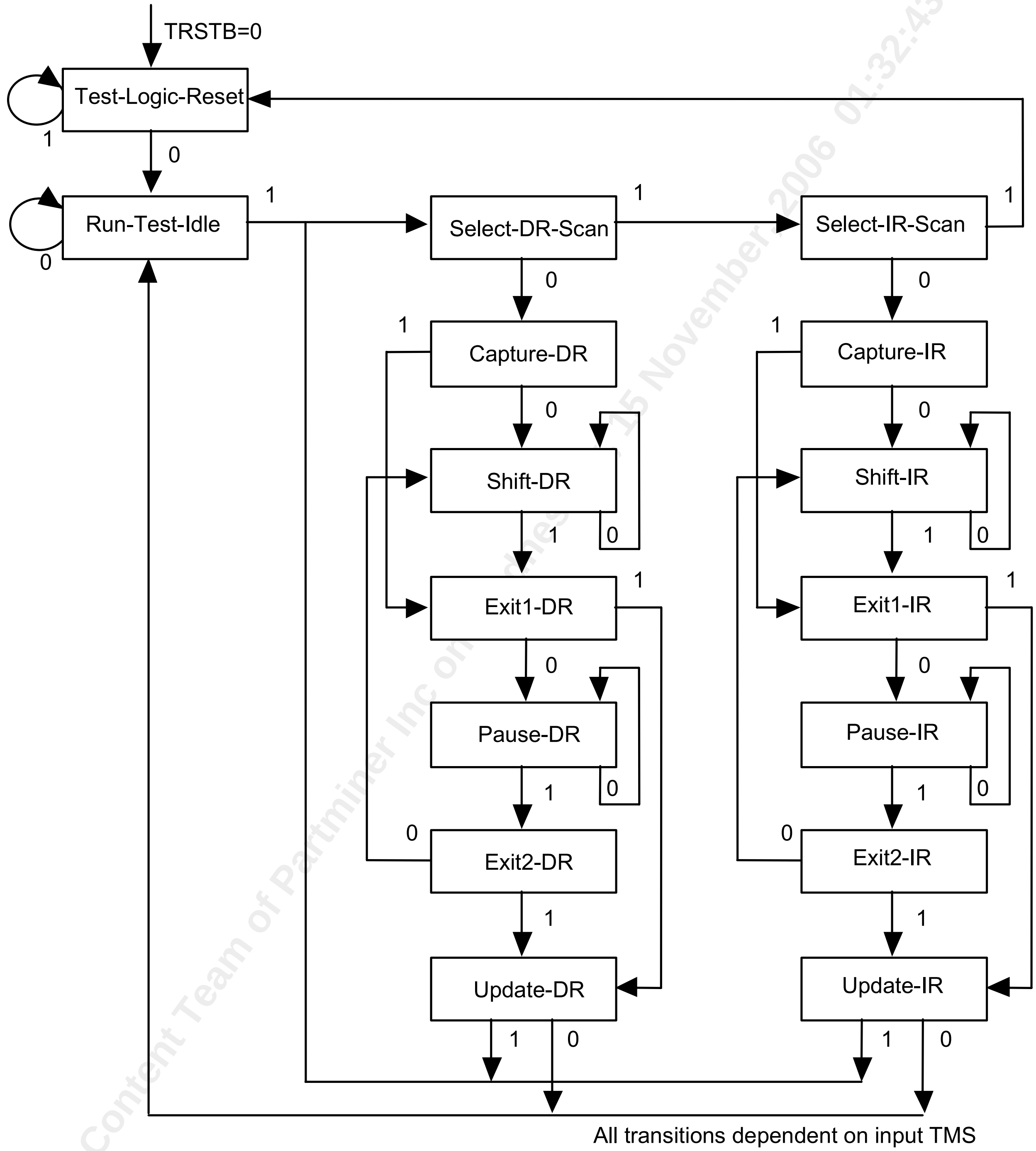
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI, to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

12.13.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is illustrated in Figure 12.

Figure 12 TAP Controller Finite State Machine



12.13.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads, or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

Section 12.13.3 describes the standard instructions. Each instruction selects a serial test data register path between input, TDI, and output, TDO.

12.13.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI, to output, TDO, with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI, and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns, shifted in through input TDI, into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register connects TDI and TDO. During the Capture-DR state, the device identification code is loaded into the Boundary Scan Register. The code can then be shifted out to output, TDO, using the Shift-DR state

13 Functional Timing

13.1 Receive Interface Timing

The Receive Interface timing describes the appropriate setting of the RJ0FP delay registers: RJ0DLY_A and RJ0DLY_B. Receive links configured to timing plane A, as per the RGRPASEL register bits, will use the RJ0DLY_A setting. Receive links configured to timing plane B will use the RJ0DLY_B setting. The RJ0DLY registers control how long data will remain in the receive FIFO. The value of the RJ0DLY register represents approximately the count in core clock cycles from the frame pulse to the reading of the J0 byte from the receive FIFO. The receive FIFO is used to synchronize frames from the receive links within a specific timing plane. The receive FIFO is also used to buffer data for timeslot interchange. Given that timeslot interchange consumes a fixed amount of time, varying RJ0DLY varies only the depth of the receive FIFO. Without loss of generality, this discussion will focus on links configured for timing plane A.

RJ0DLY_A settings are affected by the receive link rate, the core timeslot mode and the RTSI pass through (R_PASSTHRU) configuration. Valid RJ0DLY_A settings for the case when the J0 character is received at a given RP/N input coincident with the external frame pulse arrival are provided in Table 33. The last column shows the maximum FIFO depth in bytes. The maximum FIFO depth is twice or half the difference between the programmed RJ0DLY and the minimum RJ0DLY, because the line rate which the data is written into the Rx FIFO is either twice or half the core clock rate which the data is read out of the Rx FIFO.

Ignoring skew and transmit uncertainty, this gives an approximate guide to the maximum range for J0 arrivals on links designated to a common timing plane. To determine an appropriate RJ0DLY_A for the application one must factor in the delay between the frame pulse and nominal J0 arrival and possible skew from nominal delays on links. In computing the appropriate RJ0DLY, the arithmetic is modulus the RJ0DLY limit shown in Table 34.

Table 33 Valid RJ0DLY Settings

RX Link Rate (Mbit/s)	Core Timeslot Mode	RTSI Pass Through Enabled?	RJ0DLY Min	RJ0DLY Max	FIFO Depth Formula n= Actual RJ0DLY m= MIN RJ0DLY	Max FIFO Depth (in RX bytes)
622 or 777	12	No	16	32	(n-m+1)*2	34
622 or 777	12	Yes	10	38	(n-m+1)*2	58
622 or 777	48	No	57	144	(n-m+2)/2	44
622 or 777	48	Yes	33	167	(n-m+2)/2	68
2488	48	No	29	118	(n-m+1)*2	180
2488	48	Yes	5	142	(n-m+1)*2	276

To produce an RJ0DLY_A range suited for a specific system, the delay between the frame pulse and the nominal J0 arrival is converted to core clock periods and added to the RJ0DLY_A minimum and maximum values in table 33. Then a nominal value between the *system* minimum and maximum values across *all* receive links should be programmed as the RJ0DLY_A value

Table 34   Core Clock Period

Core Timeslot Mode	Clock Period (ns)	Valid RJ0DLY Settings
12	25.72016	1 to 4860
48	6.43004	1 to 19440

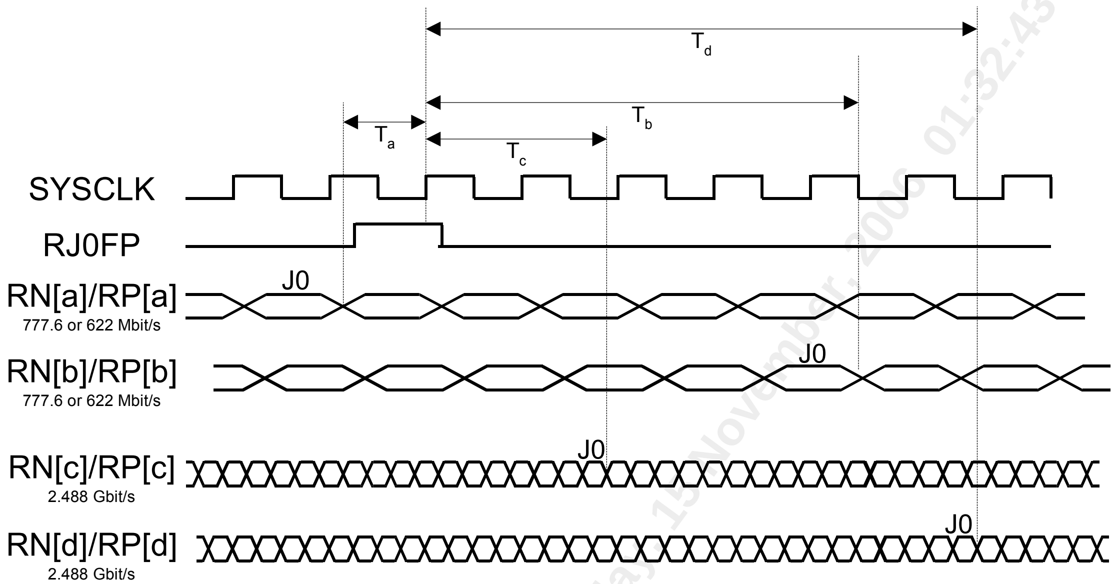
Skew from the nominal delay on links can be due to factors such as system frame pulse distribution skew, and transmit FIFO uncertainty. This dynamic skew should result in an increase in the minimum RJ0DLY_A and a decrease in the maximum RJ0DLY_A. Convert the skew into core clock periods, and add this number to the minimum RJ0DLY_A, and subtract this number from the maximum RJ0DLY_A. Again, after computing the RJ0DLY_A range, if the minimum RJ0DLY_A exceeds the maximum RJ0DLY_A, then the system as defined is unfeasible. Measures should be taken either to reduce frame pulse distribution skew or shrink the window of J0 arrivals.

Provided after these computations are done a RJ0DLY_A range results, one can validly choose any RJ0DLY_A within the range. Note that a higher RJ0DLY_A value will result in increased device latency, Device latency is discussed in the following Transmit Interface Timing section

Figure 13 illustrates an example of J0 arrivals on links relative to the system frame pulse (in 77MHz frame pulse mode). The time deltas in the figure represent the difference from the frame pulse to the J0 arrival on the respective link in core clock periods. As shown, the J0 arrival differs on links. One can calculate the valid RJ0DLY_A range for each link, and then select an RJ0DLY_A from the intersection of the calculated ranges. The minimum RJ0DLY_A value from the intersection would provide the minimum FIFO depth that can handle the J0 arrival spread on the receive links.

For example, valid RJ0DLY_A will be calculated for the example below, ignoring links c and d. Assume that the core timeslot mode is 48 and RTSI pass through is disabled. The RJ0DLY_A range for link RN[a]/RP[a] would be from T_a+57 to T_a+144, based on RJ0DLY boundaries from Table 33. The RJ0DLY_A range for link RN[b]/RP[b] would be from T_b+57 to T_b+144. Assume that all links on the timing plane are 777.6 MHz have a delay T_x relative to the frame pulse such that $T_a <= T_x <= T_b$ Given that $T_a < T_b$ then the valid RJ0DLY_A for the timing plane would be T_b+57 to T_a+144. If the frame pulse distribution skew is +/-20ns, and transmit uncertainty is 12.86 ns, then the RJ0DLY_A range should be reduced by (2x20+12.86)/6.43 < 9 at either end of the RJ0FP range resulting in a RJ0DLY_A range of T_b+66 to T_a+135. In this example the window for J0 arrivals, or the maximum difference between T_b and $T_{a,}$ is 69 core clock periods, or 443 ns.

Figure 13 Receive Interface Timing



The RJ0DLY_A for 2.488 Gbit/s links is calculated using the same methodology for 777.6 Mbit/s links, ignoring links a and b. Note the core timeslot mode must be 48. The RJ0DLY_A range for link RN[c]/RP[c] would be from T_c+29 to T_c+118. The RJ0DLY_A range for link RN[d]/RP[d] would T_d+29 to T_d+118. Assume that all links on the timing plane are 2.488 Gbit/s have a delay T_x relative to the frame pulse such that $T_c <= T_x <= T_d$ Given that $T_c < T_d$ then the valid RJ0DLY_A for the timing plane would be T_d+29 to T_c+118. As in the previous example, if the frame pulse distribution skew is +/-20ns, and transmit uncertainty is 3.215 ns, then the RJ0DLY range should be reduced by (2x20+3.215)/6.43 < 7 at either end of the RJ0FP range, resulting in a RJ0DLY_A range of T_d+36 to T_c+111. In this example the window for J0 arrivals, or the maximum difference between T_d and T_c is 75 core clock periods, or 482 ns.

Note that a timing plane could handle all three rates of traffic simultaneously, as indicated in the diagram. The same procedure should be used, computing valid RJ0DLY_As for the earliest and latest J0 arrivals for each link rate.

13.2 Transmit Interface Timing

The transmit interface timing describes the device delay. Measured delay on data through the device is captured in Table 35. Delay through the device depends on receive link rate, transmit link rate, core timeslot mode, TTSI pass through (TPASSTHRU_A) configuration, and the RJ0DLY_A setting. Each row in the table provides a frame pulse to J0 latency formula in terms of RJ0DLY for the delay from the frame pulse time until J0 emission for a device with the given configuration. The delay on the data imposed by the device is the sum of the frame pulse to J0 latency and the difference between the frame pulse arrival and the frame arrival (specifically J0 character arrival) at receive serial interface.

Table 35 Data Transmit Delay

TX Link Rate (Mbit/s)	Core Timeslot Mode	TTSI Pass Through	FP to J0 Latency Formula (ns) where n is RJ0DLY used	Expected Variation from Typical Delay
622 or 777	12	No	668+n*25.72	±1 *12.86ns
		Yes	540+n*25.72	±1 *12.86ns
622 or 777	48	No	515+n*6.43	±1 *12.86ns
		Yes	386+n*6.43	±1 *12.86ns
2488	48	No	340+n*6.43	±1 *3.125ns
		Yes	192+n*6.43	±1 *3.125ns

These represent the typical delays through the device, with CORE_FP_CENTER toggled and the TTSI FIFO CENTER bit being set following successful locking of the CSU to the reference clock. Failure to do these will increase the uncertainty in device delay requiring deeper receive FIFOs. The expected variation increases to ±4 byte clocks from ±1 byte clocks shown in the table.

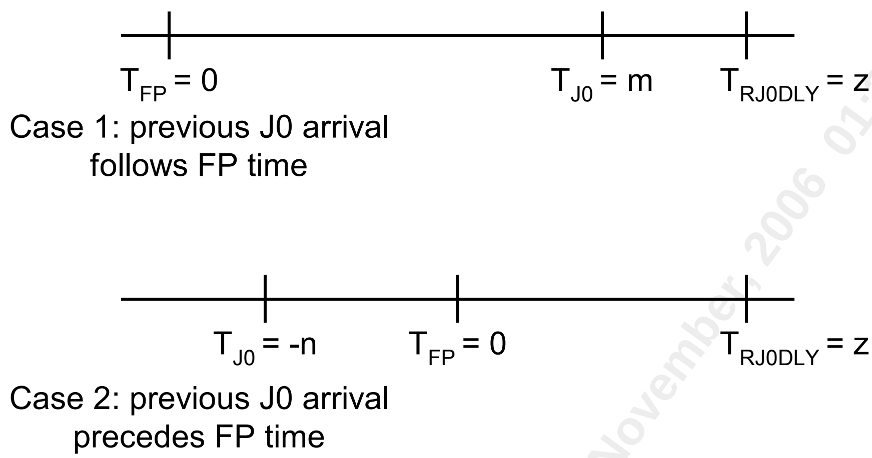
As indicated before, the delay on the data imposed by the device is the sum of the total latency and the difference between the frame pulse arrival and the frame arrival (specifically J0 character arrival) at receive serial interface. This is shown in Equation 1

Equation 1 Data Delay

$$DATA\_DELAY = LATENCYfp\_to\_j0 + (Tfp - Tj0)$$

To be clear which frame we are referencing against a frame pulse, it is not necessarily the frame containing the first J0 following the frame pulse. It is the frame containing the J0 arriving previous to the time of the frame pulse + RJ0DLY* core clock period. Refer to Figure 14 for an illustration of the possible positions of the J0 arrival relative to the frame pulse and RJ0 delay.

Figure 14 Frame Pulse and J0 Arrival Relative Positions



In the figure T_{FP} represents the frame pulse time, T_{RJ0DLY} represents the time T_{FP} +RJ0DLY*core_clock_period, and T_{J0} represents the time of the J0 arrival on the link of interest, immediately preceding $T_{RJ0DLY.}$ In case #1, we see the TJ0 following the frame pulse. In this case, the data latency will be the FP to J0 latency less m. In case #2, we see the preceding J0, in advance of the frame pulse. In this case the data latency will be the FP to J0 latency + n. Table 36 provides examples of each case with actual numbers. All cases assume 2.488 Gbit/s rate on both receive and transmit links, receive and transmit TSI.

Table 36 Data Delay Examples

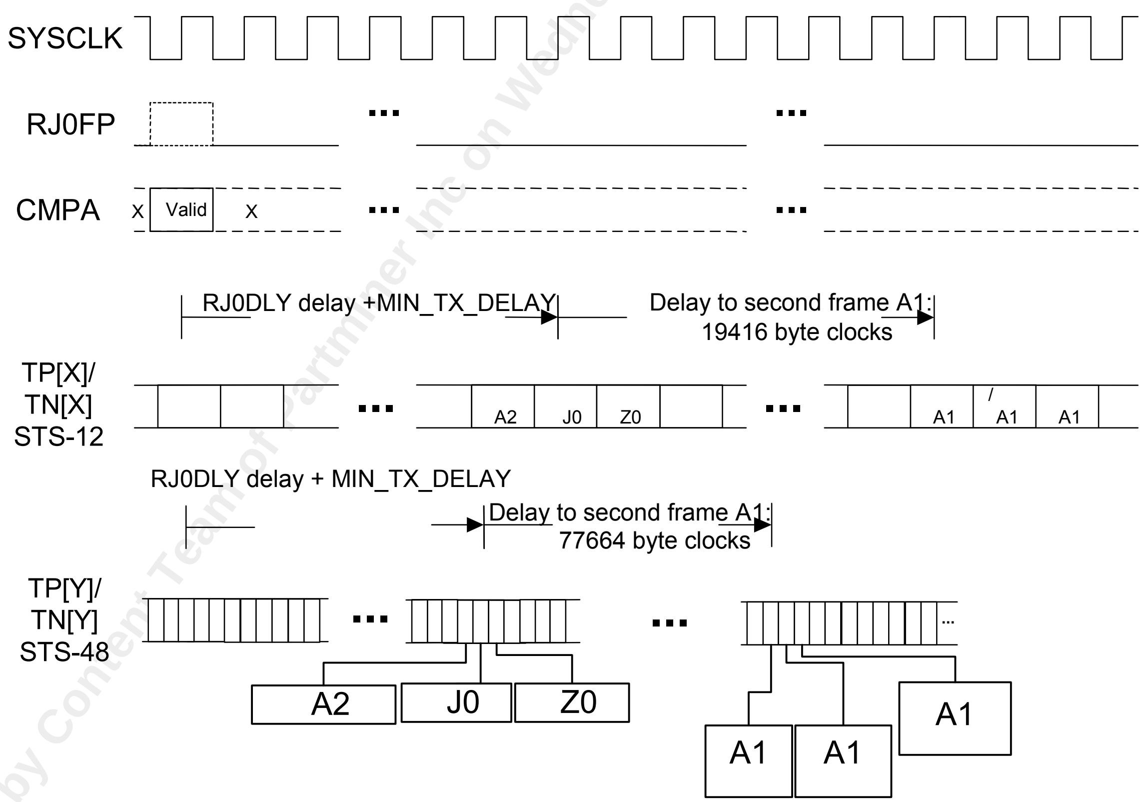
Case	T_{J0} (ns) (assume T_{FP} = 0)	Min RJ0DLY	RJ0DLY	FIFO depth	FP to J0 Latency (ns)	Data Latency (ns)
1 (J0 follows frame pulse)	124300	19361	19440	160	125327	1027
2 (J0 precedes frame pulse)	-700	19361	1	162	333	1033
2 (J0 precedes frame pulse)	-200	19438	10	26	391	591

13.3 RWSEL_A, RWSEL_B, CMP_A, and CMP_B Timing

Figure 15 shows the relationship of delay from CMP_A to its effect on data on the transmit serial data links, given that receive 8 kHz mode is off (R8KCLK register bit is logic 0). The behavior of RWSEL_A, RWSELB, and CMP_B is identical except RWSEL_B and CMP_B are sensitive to RJ0DLY_B. When the R8KCLK register bit is low, RWSEL_A, RWSEL_B, CMP_A and CMP_B are sampled on the RJ0FP pulse (whether it is pulsed or not) and are held for approximately 2 frames before the changes are applied to the data. The values of RWSEL_A, RWSEL_B, CMP_A and CMP_B are ignored at other locations of the transport frame. When the R8KCLK register bit is high, RWSEL_A, RWSEL_B, CMP_A and CMP_B are sampled on the rising edge of SYSCLK, and held for approximately 2 frame times before being applied to the data.

A change in value to the connection memory page signal (CMP_A) results in changes to the active switch settings. Given that CMP_A is sampled on the RJ0FP pulse time 0, the first data that is switched according to the newly selected connection memory page are the A1 bytes of the second frame following the J0 transmitted after time RJ0DLY_A delay + minimum transmit delay detailed in Section 13.2.

Figure 15 CMP_A Timing



13.4 TJ0FPA, TJ0FPB Timing

The transmit frame pulse signal for timing plane A (TJ0FPA) provides system timing for timing plane A configured transmit links. The transmit frame pulse signal for timing plane B (TJ0FPB) provides system timing for timing plane B configured transmit links. The timing of these signals is identical with the exception that TJ0FPA timing is sensitive to the RJ0DLY_A value and TJ0FPB timing is sensitive to the RJ0DLY_B value. The remainder of the section will therefore discuss only TJ0FPA timing.

TJ0FPA pulses high to indicate that all J0 signals of a frame should have been transmitted from the timing plane A configured TN/TP signals at the time the pulse occurs. TJ0FPA is a pessimistic signal. It assumes that some transmit link in the timing plane is configured for the slowest operation: STS-12 link rate with transmit time switching enabled. Therefore its delay is relatively fixed once the delay from RJ0FP (RJ0DLY_A) is taken into account . The formula for the delay (in ns) is given in Equation 2. The initial delay is 0 ns if in 8 kHz frame pulse mode. Otherwise the delay is two SYSCLK cycles.

Equation 2   TJ0FP Delay Calculation

$$TJ0FPA\_DELAY = initial\_delay + (RJ0DLY\_A + 124) * core\_clock\_period$$
$$TJ0FPB\_DELAY = initial\_delay + (RJ0DLY\_B + 124) * core\_clock\_period$$

Given the variation between the RJ0FP and the internal frame counter, the time when the pulse initially appears can be +/- 57 ns.

14 Absolute Maximum Ratings

Absolute maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 37 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (VDDI)	-0.3V to +2.5V
3.3V Supply Voltage (VDDO)	-0.3V to +4.6V
Input pad tolerance	-2V < VDDO < +2V for 10ns, 100mA max
Output pad overshoot limits	-2V < VDDO < +2V for 10ns, 20mA max
Voltage on Any Digital Pin	-0.3V to V_{VDD}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Reflow Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 Power Information

15.1 Power Requirements

Table 38 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
Mode 1: 16x777.6 Mbit/s to 48x777.6 Mbit/s (W, P, A).	IDDI (1.8V)	4.965	—	6.28	A
	IDDA (1.8V)	519.5	—	990.46	mA
	IDDO (3.3 V)	6.447	—	17.01	mA
	Total Power	9.96	12.01	—	W
Mode 3: 32x777.6 Mbit/s to 8xx2.488 Gbit/s (W, P) - Dual TBS.	IDDI (1.8V)	6.08			A
	IDDA (1.8V)	520.41	—		mA
	IDDO (3.3 V)	6.96	—		mA
	Total Power	11.90	12.71	—	W

Notes

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system
4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=95° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics
5. For more information on the power dissipation of a particular configuration, please refer to document PMC-2011553 “Power Consumption for the PM5307 TBS-9953 and PM5374 TSE-160”.

15.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. VDDO power must be supplied either before VDDI or simultaneously with VDDI.

2. VDDA must be applied after VDDO, and either before or after VDDI. Or, VDDA can be applied simultaneously with VDDO and VDDI.

3. I/Os get driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

4. Power down the device in the reverse sequence.

15.3 Power Supply Filtering

The device uses three separate power sources: VDDO, VDDI, and VDDA. The device has one set of analog and digital ground pins: VSS. The ground pins can be connected to a common uninterrupted physical ground plane. All analog and digital power pins are to be decoupled to the VSS ground.

Power supply filter recommendations are found in Application Note PMC-2011065 and are required for proper operation of the device.

16 D.C. Characteristics

T_a = -40°C to T_j =95°C, $V_{VDDI} = V_{VDDItypical}$ ± 5%, $V_{VDDO} = V_{VDDOtypical}$ ± 5%
(Typical Conditions: T_J = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{VDDA} = 1.8V)

Table 39 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDA}	Analog Power Supply	1.71	1.8	1.89	Volts	—
V_{VDDI}	Power Supply at 1.8V	1.71	1.8	1.89	Volts	—
V_{VDDO}	Power Supply at 3.3V	3.135	3.3	3.465	Volts	—
V_{IL}	Input Low Voltage	0	—	0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0	—	—	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage	—	0.1	0.4	Volts	Guaranteed output Low voltage at VDD=3.13V and IOL=maximum rated for pad
V_{OH}	Output or Bi-directional High Voltage	2.4	2.7	—	Volts	Guaranteed output High voltage at VDD=3.13V and IOH=maximum rated current for pad.
VT+	Reset Input High Voltage	2.2	—	—	Volts	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage	—	—	0.8	Volts	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage	—	0.5	—	Volts	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	-100	-50	-4	µA	VIL = GND Notes 1 and 3.
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD Notes 1 and 3.
IIL	Input Low Current	-10	0	+10	µA	VIL = GND Notes 2 and 3.
IIH	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 2 and 3.
CIN	Input Capacitance	—	5	—	PF	TA=25°C, f = 1 MHz
COUT	Output Capacitance	—	5	—	PF	TA=25°C, f = 1 MHz
CIO	Bi-directional Capacitance	—	5	—	PF	TA=25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IRM}	REFCLK Differential Input Pulse Amplitude	1200		2000	mV	Differential pk-pk

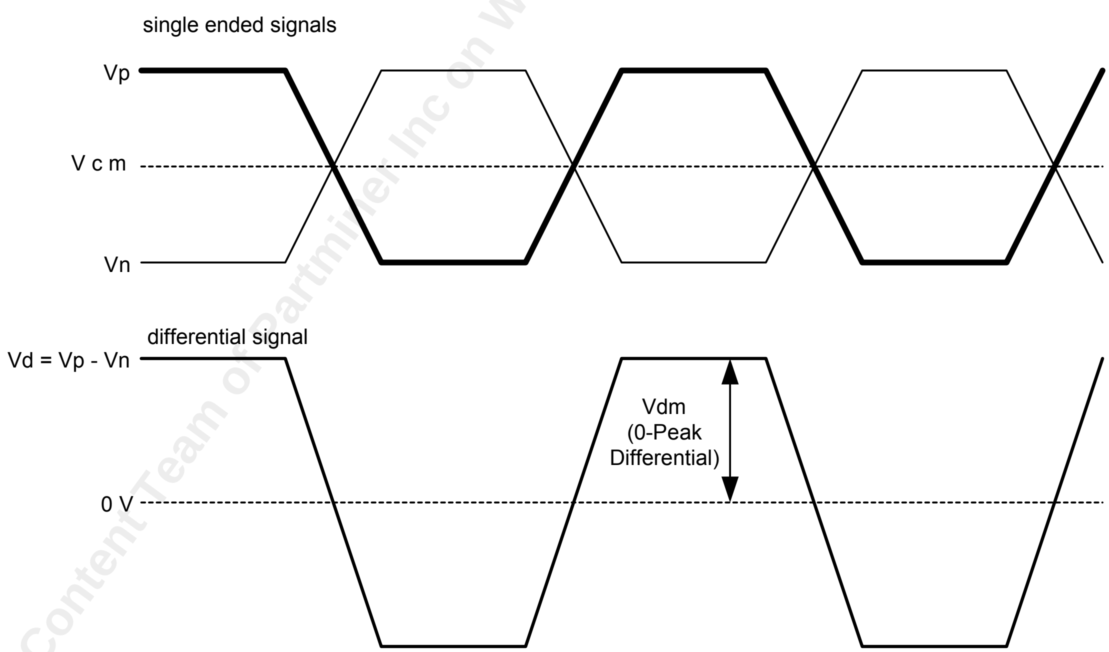
Notes on D.C. Characteristics

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

16.1 D.C. Specifications of High-Speed Links

This section describes DC operation of the high-speed serial ELVDS links. The ELVDS operation of the links is described in Table 40, Table 42, and Table 43. The ELVDS links of the device also support D.C. coupled operation that is described in Table 41 and Table 44. Figure 16 defines the differential and common mode level terminology used in the DC specification tables. The V_{CM} and V_{DM} parameters apply to both the receiver (V_{ICM}/V_{IDM}) and the transmitter (V_{OCM}/V_{ODM}). Refer to PMC-2021638, Jitter Budget and Pre-Emphasis Settings for the TSE 160 and TBS 9953, for a description of pre-emphasis, including transfer functions and recommendations on when to enable pre-emphasis.

Figure 16 D.C. Specification Parameter Definition



16.1.1 Transmitter

The DC characteristics of the transmitter depend on the configuration of the transmit links for high current mode and pre-emphasis. The high current mode is set via the HICUR bit in the Register: 0036H, 003E, 0046H, 004EH FACE #1 - #4 Configuration. The pre-emphasis mode is set via the PREEMPH_EN bit in the Register: MN32H Port #1 - #65 TSEC Enable Control.

Table 40 Transmitter Common Mode/Differential Swing Range for 100 ohm Termination

Spec.	Description	Min	Max	Units	Comment
V_{ODM}	Output Differential Voltage HICUR = 1 PREEMPH_EN = 0	0.651	0.960	V	0-Peak Differential R_{LOAD}=100Ω ±1%differential (Floating, no external DC bias). Transmitter is interfaced to AC coupled receiver. Pre-emphasis not supported when HICUR=0.
	Output Differential Voltage HICUR = 0 PREEMPH_EN = 0	0.344	0.518		
	Output Differential Voltage - Peak HICUR = 1 PREEMPH_EN = 1	0.609	0.860		
	Output Differential Voltage - Steady State HICUR = 1 PREEMPH_EN = 1	0.354	0.548		
V_{OCM}	Output Common Mode HICUR = 1 PREEMPH_EN = 0	0.768	0.944	V	R_{LOAD}=100Ω ±1% differential (Floating, no external DC bias).
	Output Common Mode HICUR = 1 PREEMPH_EN = 1	0.768	0.940		
	Output Common Mode HICUR = 0 PREEMPH_EN = 0	0.756	0.936		
R_O	Output Resistance Differential	80	120	Ω	
I_{SP},I_{SN}	Short-Circuit Output Current		15	mA	Drivers shorted to ground
I_{SPN}	Short-Circuit Output Current		15	mA	Drivers shorted together

Table 41 Transmitter Common Mode/Differential Swing Range for 50 ohm Termination to 0.5VDDI to 0.7 VDDI

Spec.	Description	Min	Max	Units	Comment
V_{ODM}	Output Differential Voltage HICUR = 1 PREEMPH_EN = 0	0.600	1. 050	V	0-Peak Differential R_{LOAD}=50Ω ±1% single ended to $V_{common\ mode}$. $V_{common\ mode}$=0.5*VDDI (min.) to 0.7*VDDI (max). Transmitter is interfaced to DC coupled receiver. Actual amplitude will depend on the amplitude of the common mode voltage termination of the load.
	Output Differential Voltage HICUR = 0 PREEMPH_EN = 0	0.300	0.620		
	Output Differential Voltage - Peak HICUR = 1 PREEMPH_EN = 1	0.550	1.050		
	Output Differential Voltage - Steady State HICUR = 1 PREEMPH_EN = 1	0.300	0.680		
V_{OCM}	Output Common Mode HICUR = 1 PREEMPH_EN = 0	0.700	1.100	V	R_{LOAD}=50Ω ±1% single ended to $V_{common\ mode}$. $V_{common\ mode}$=0.5*VDDI (min.) to 0.7*VDDI (max). Actual amplitude will depend on the amplitude of the common mode termination voltage of the load.
	Output Common Mode HICUR = 1 PREEMPH_EN = 1	0.700	1.100		
	Output Common Mode HICUR = 0 PREEMPH_EN = 0	0.700	1.100		
R_O	Output Resistance Differential	80	120	Ω	
I_{SP},I_{SN}	Short-Circuit Output Current		18	mA	Drivers shorted to ground
I_{SPN}	Short-Circuit Output Current		18	mA	Drivers shorted together

16.1.2 Receiver

The DC characteristics of the receiver depend on the configuration of the receive links for internal vs. external AC coupling or DC coupling. The coupling mode is set via the ACCOUPLE bits in the Register: 0034H, 003CH, 0044H, 004CH CSUI #1 - #4 AC Coupling Control. ACCOUPLE = 0 enables the internal AC coupling capacitor. ACCOUPLE = 1 disables the internal AC coupling capacitor.

Table 42 Receiver Common Mode/Differential Swing Range for Internally AC Coupled Receiver

Spec.	Description	Min	Max	Units	Comment
V_{ICM}	Input Common-Mode Range	0.250	1.565	V	ACCOUPLE = 0 No External AC capacitor
V_{IDM}	Input Differential Swing	0.0875	1.100	V	0-Peak Differential Input signal must meet the following conditions: $V_{ICM} + V_{IDM}/2 < (VDDI + 0.4V)$ and $V_{ICM} – V_{IDM}/2 > - 0.4 V$
R_{IN}	Differential Input Resistance	80	120	Ω	

Table 43 Receiver Common Mode/Differential Swing Range for Externally AC Coupled Receiver

Spec.	Description	Min	Max	Units	Comment
V_{ICM}	Input Self Bias Common-Mode Range	VDDI/2 – 0.2	VDDI/2 + 0.2	V	ACCOUPLE = 1 External AC capacitor
V_{IDM}	Input Differential Swing	0.0875	1.100	V	0-Peak Differential
R_{IN}	Differential Input Resistance	80	120	Ω	

Table 44 Receiver Common Mode/Differential Swing Range for Externally DC Coupled Receiver

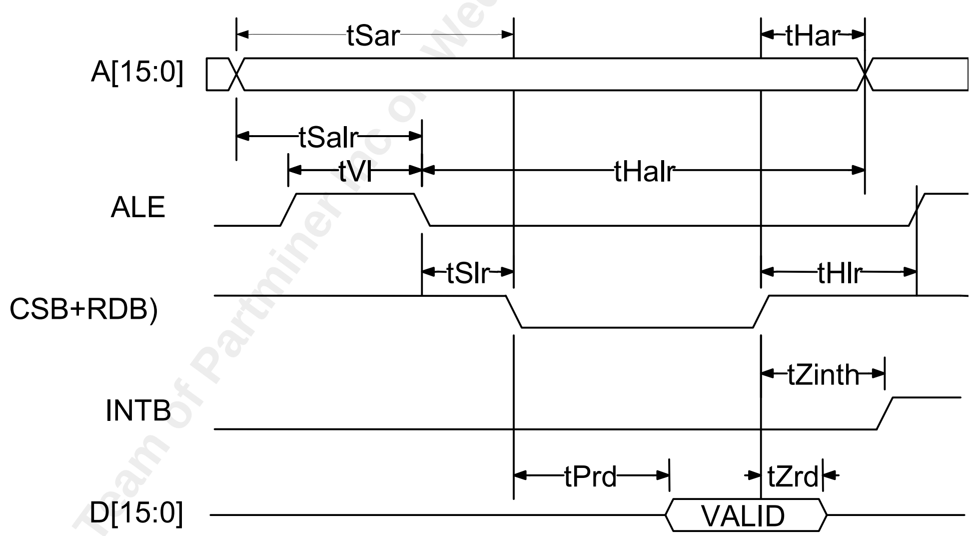
Spec.	Description	Min	Max	Units	Comment
V_{ICM}	Input Common-Mode Range	VDDI/2	VDDI	V	ACCOUPLE = 1 No external AC capacitor
V_{IDM}	Input Differential Swing	0.0875	1.100	V	0-Peak Differential Input signal must meet the following condition: $V_{ICM} + V_{IDM}/2 < (VDDI + 0.4V)$
R_{IN}	Differential Input Resistance	80	120	Ω	

17 Microprocessor Interface Timing Characteristics

Table 45 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	10	—	ns
tH_{AR}	Address to Valid Read Hold Time	5	—	ns
tS_{ALR}	Address to Latch Set-up Time	10	—	ns
tH_{ALR}	Address to Latch Hold Time	10	—	ns
tV_{L}	Valid Latch Pulse Width	5	—	ns
tS_{LR}	Latch to Read Set-up	0	—	ns
tH_{LR}	Latch to Read Hold	5	—	ns
tP_{RD}	Valid Read to Valid Data Propagation Delay	—	70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state	—	20	ns
tZ_{INTH}	Valid Read Negated to INTB High	—	50	ns

Figure 17 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing

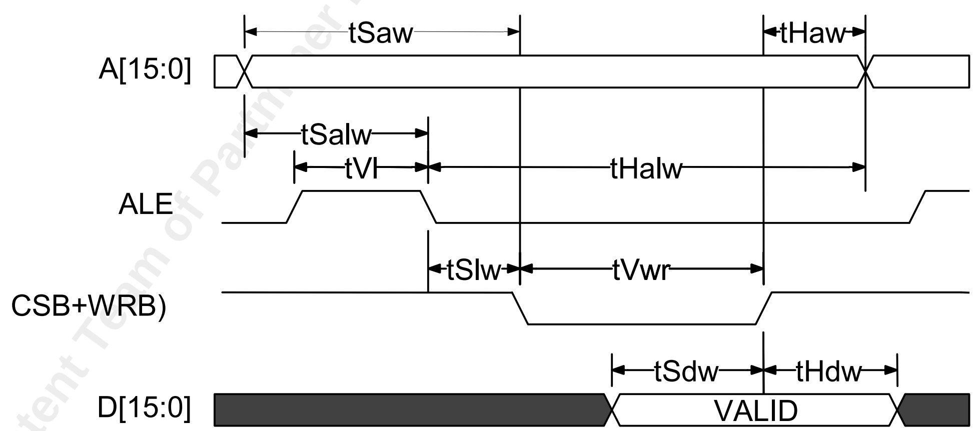
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical NOR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock

Table 46 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10	—	ns
tS_{DW}	Data to Valid Write Set-up Time	20	—	ns
tS_{ALW}	Address to Latch Set-up Time	10	—	ns
tH_{ALW}	Address to Latch Hold Time	10	—	ns
tV_L	Valid Latch Pulse Width	5	—	ns
tS_{LW}	Latch to Write Set-up	0	—	ns
tH_{LW}	Latch to Write Hold	5	—	ns
tH_{DW}	Data to Valid Write Hold Time	5	—	ns
tH_{AW}	Address to Valid Write Hold Time	5	—	ns
tV_{WR}	Valid Write Pulse Width	40	—	ns

Figure 18 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing

1. A valid write cycle is defined as a logical NOR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

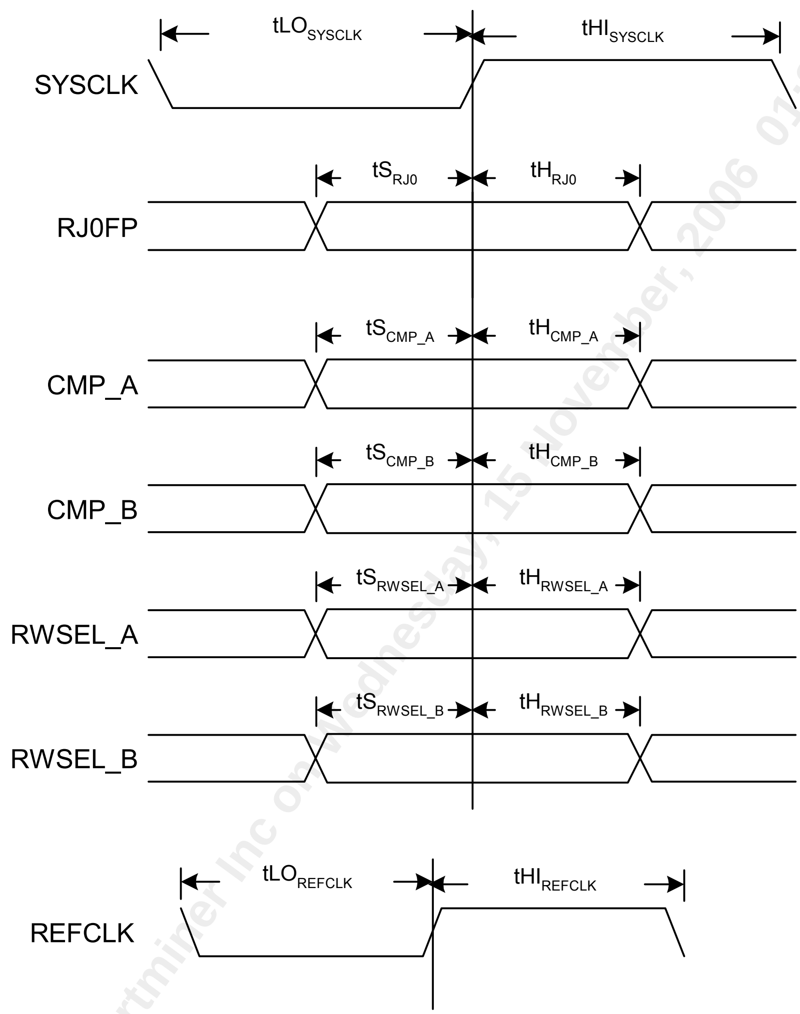
18 A.C. Timing Characteristics

18.1 Input Timing

Table 47 Input Timing

Symbol	Description	Min	Max	Units
FSYSCLK	SYSCLK Frequency (77.76 MHz mode)	77.76	77.76	MHz
FSYSCLK	SYSCLK Frequency (8 kHz mode)	8	8	kHz
tHISYSCLK	SYSCLK Minimum High Pulse Width	40	—	%
tLOSYSCLK	SYSCLK Minimum Low Pulse Width	40	—	%
tSRWSEL_A	RWSEL_A Set-Up Time	3	—	ns
tHRWSEL_A	RWSEL_A Hold Time	1.1	—	ns
tSRWSEL_B	RWSEL_B Set-Up Time	3	—	ns
tHRWSEL_B	RWSEL_B Hold Time	1.1	—	ns
tSCMP_A	CMP_A Set-Up Time	3	—	ns
tHCMP_A	CMP_A Hold Time	1.1	—	ns
tSCMP_B	CMP_B Set-Up Time	3	—	ns
tHCMP_B	CMP_B Hold Time	1.1	—	ns
tSRJ0	RJ0FP Set-Up Time	3	—	ns
tHRJ0	RJ0FP Hold Time	1.1	—	ns

Figure 19 TBS 9953 Input Timing



Notes on Input Timing

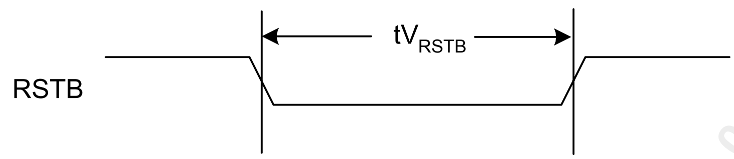
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18.2 Reset Timing

Table 48 RSTB Timing (Figure 20)

Symbol	Parameter	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100	—	ns

Figure 20 RSTB Timing



18.3 Reference Clock Interface

Table 49 provides the reference clock specification.

Table 49 Reference Clock Specifications

Symbol	Parameter	Min	Nominal	Max	Units
Dcref	Reference Clock Duty Cycle	40	—	60	%
Tjref	Reference Clock Total Jitter (12k-20M RMS)	—	—	4.0	pS RMS
FREFCLK	REFCLK Frequency	—	155.52	—	MHz
tRFref	Reference Clock Rise / Fall Times	—	—	1.0	ns

Notes on Reference Clock Timing

1. Total jitter includes both deterministic jitter and random jitter but it is assumed the majority of the jitter is random
2. Rise time is measured from the 10% threshold of the reference signal to the 90% threshold of the reference signal.
3. Fall time is measured from the 90% threshold of the reference signal to the 10% threshold of the reference signal.
4. Note that Tjref is at the chip pin, so the jitter contribution of clock buffers needs to be accounted for in addition to the crystal reference. This spec should allow 4-level of buffering assuming a 3.5ps reference (SaRonix SEL24xx/SEL25xx series references) and a 1ps RMS contributed by each buffering stage

18.4 ELVDS Data Interface

Table 50 and Table 51 give specifications for the ELVDS data interfaces. Refer to PMC-2021638, Jitter Budget and Pre-Emphasis Settings for the TSE 160 and TBS 9953, for an explanation of how to derive a jitter budget for the TBS 9953.

Table 50 Output Data Timing (TxData)

Symbol	Parameter	Min	Typ	Max	Units	Comments
Djod	Output Data Deterministic Jitter (pk-pk between dataRate/1667 to dataRate/2)	—	0.15	—	UI	—
Tjod	Output Data Total Jitter (pk-pk between dataRate/1667 to dataRate/2)	—	0.45	—	UI	Assumes no REFCLK jitter
Dttod	Differential transition time for TX[n]_P/N 20% to 80%.	60	—	130	ps	Based on design specification. Not a tested parameter

Notes on Output Timing

1. The Unit Interval (UI) is the reciprocal of the symbol rate.
2. The above values do not include the reference clock jitter
3. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
4. Values are measured with each LVDS output AC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
5. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 51 Input Data Timing (RxData)

Symbol	Parameter	Min	Typical	Max	Units
DJid	Input Data Deterministic Jitter Tolerance	—	0.57	—	UI
TJid	Input Data Total Jitter Tolerance (pk-pk between dataRate/1667 to dataRate/2)	—	0.87	—	UI
tDSin	Input Differential Skew	—	—	±60	ps

Notes on Input Timing

1. The Unit Interval (UI) is the reciprocal of the symbol rate.
2. The above values do not include the reference clock jitter
3. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
4. Values are measured with each LVDS input AC coupled into a 50 Ohm impedance.
5. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

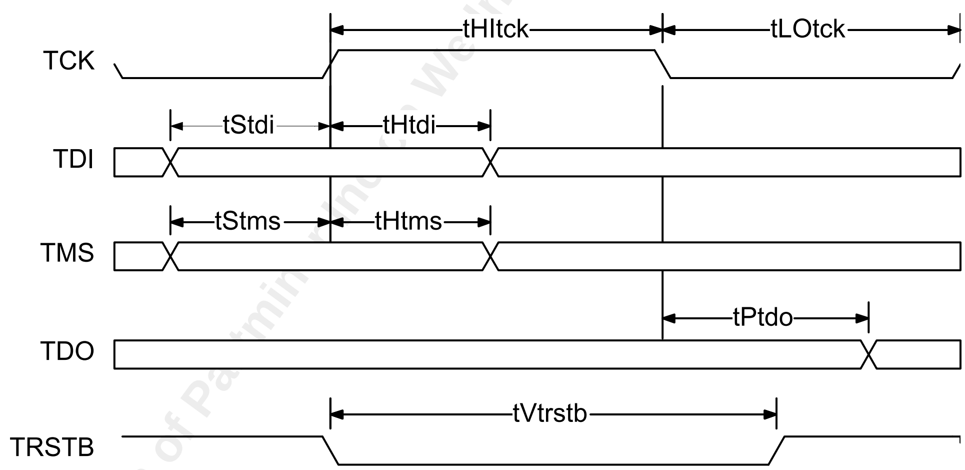
6. It is expected that no more than 0.1UI of Input Data Deterministic Jitter be applied as Sinusoidal Jitter (SJ).

18.5 JTAG Port Interface

Table 52 JTAG Port Interface

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency	—	4	MHz
THITCK	TCK HI Pulse Width	100	—	ns
THITCK	TCK LO Pulse Width	100	—	ns
TSTMS	TMS Set-up time to TCK	25	—	ns
tHTMS	TMS Hold time to TCK	25	—	ns
tSTDI	TDI Set-up time to TCK	25	—	ns
tHTDI	TDI Hold time to TCK	25	—	ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100	—	ns

Figure 21 JTAG Port Interface Timing



19 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1]. The maximum long-term operating junction temperature is 95°C.

Table 53 Outside Plant Thermal Information

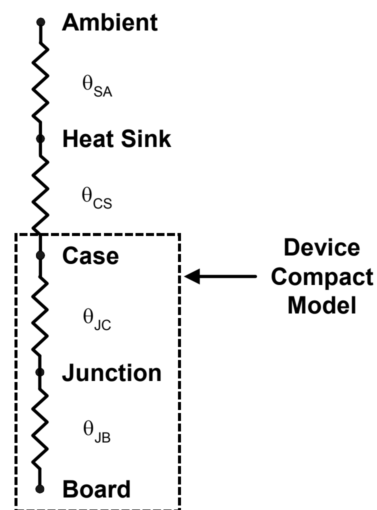
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	95 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 54 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.10 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	2.8 °C/W

Table 55 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(95 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation

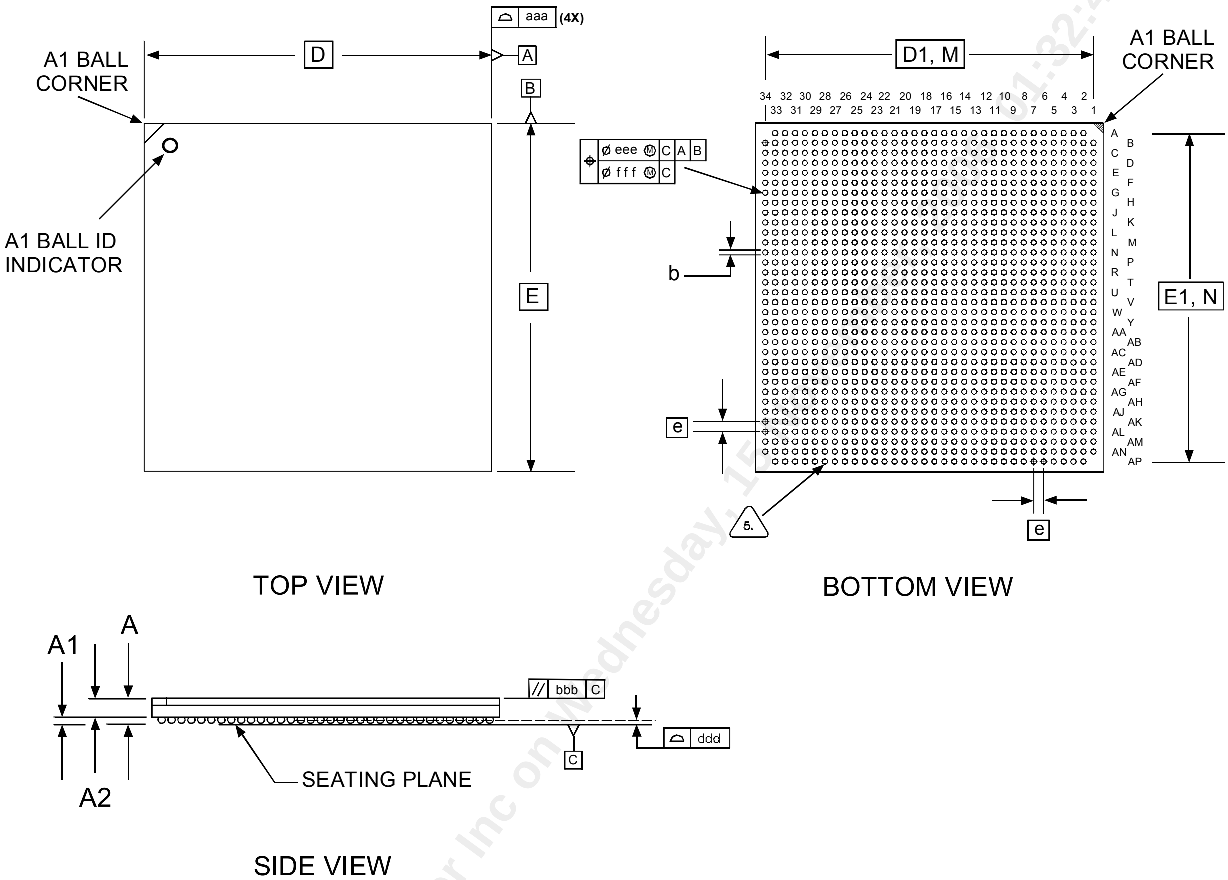


Power depends upon the operating mode. To obtain power information, refer to 'High' power values in Section 15.1 Power Requirements.

Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about this standard, see [13]
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see [11]
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

20 Mechanical Information



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.530 MM (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MS-034, VARIATION AAR-1.

PACKAGE TYPE : 1152 FLIP CHIP BALL GRID ARRAY - FCBGA															
BODY SIZE : 35 x 35 x 2.39 MM (7 LAYERS)															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f
Min.	2.11	0.40	1.71	-	-	-	-	-	0.50	-	-	-	-	-	-
Nom.	2.39	0.50	1.89	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.64	1.00 BSC	-	-	-	-	-
Max.	2.67	0.60	2.07	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10

Notes