POWER MOSFET TRANSISTORS

2N6791
2N6792

400 Volt, 1.8 Ohm
N-Channel

T-39-09

FEATURES
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

DESCRIPTION

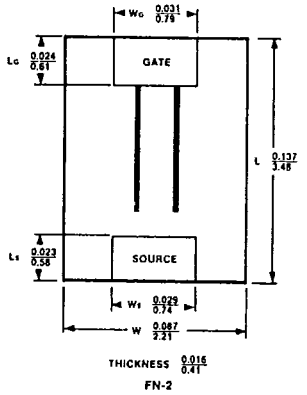
The Unitrode power MOSFET design utilizes the most advanced technology available. This efficient design achieves a very low $R_{DS(on)}$ and a high transconductance.

The Unitrode power MOSFET features all of the advantages of MOS technology such as voltage control, freedom from second breakdown, very fast switching speeds, and thermal stability.

These power MOSFETS are ideally suited for many high-speed, high-power switching applications such as switching power supplies, motor controls, and wide-band and audio amplifiers.

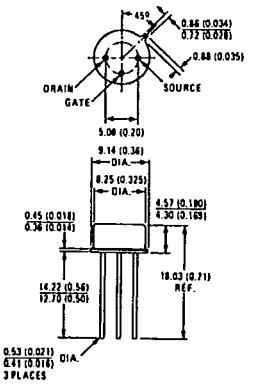
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6791	350V	1.8Ω	2.0A
2N6792	400V	1.8Ω	2.0A



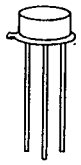
MECHANICAL SPECIFICATIONS

2N6791, 2N6792



All Dimensions in Millimeters and (Inches)

TO-205 AF (TO-39)



UNITRODE

2N6791 2N6792

T-39-09

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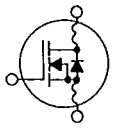
ABSOLUTE MAXIMUM RATINGS

Parameter		2N6791	2N6792			Units
V_{DS}	Drain - Source Voltage ①	350*	400*			V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1MΩ) ①	350*	400*			V
I_D @ T_C = 25°C	Continuous Drain Current	2.0*	2.0*			A
I_{DM}	Pulsed Drain Current ③	10	10			A
V_{GS}	Gate - Source Voltage	±20*				V
P_D @ T_C = 25°C	Max. Power Dissipation	20* (See Fig. 14)				W
	Linear Derating Factor	0.16* (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	10	(See Fig. 15 and 16) L = 100μH 10			A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300(0.063 in. (1.6mm) from case for 10s)				°C

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless otherwise specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	2N6791	350*	—	—	V	V_{GS} = 0V
		2N6792	400*	—	—	V	I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100*	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	ALL	2.0	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	ALL	—	—	1.8*	Ω	V_{GS} = 10V, I_D = 1.25A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	ALL	—	—	4.0*	Ω	V_{GS} = 10V, I_D = 1.25A, T_C = 125°C
$V_{DS(on)}$	On-State Drain-Source Voltage ②	ALL	—	—	3.6*	V	V_{GS} = 10V, I_D = 2.0A
g_{fs}	Forward Transconductance ②	ALL	1.0*		3.0*	S(℧)	V_{DS} = 15V, I_D = 1.25A
C_{iss}	Input Capacitance	ALL	200*	—	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	40*	—	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	5*	—	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	40*	ns	V_{DD} = 35V, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
T_r	Rise Time	ALL	—	—	35*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	60*	ns	
t_f	Fall Time	ALL	—	—	35*	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V_{GS} = 10V, I_D = 5.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead. 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	—	—	6.25*	K/W	
R_{thJA}	Junction-to Ambient	ALL	—	—	175	K/W	Free Air Operation

*Indicates JEDEC registered values.

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	ALL	—	—	20*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ③	ALL	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	ALL	0.6*	—	1.4*	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{rr}	Reverse Recovered Charge	ALL	—	3.1	—	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25° to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*Indicates JEDEC registered values.

Fig. 1 – Typical Output Characteristics

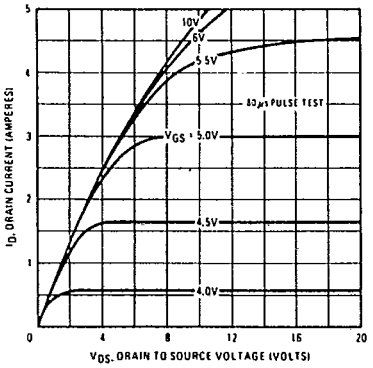

Fig. 2 – Typical Transfer Characteristics

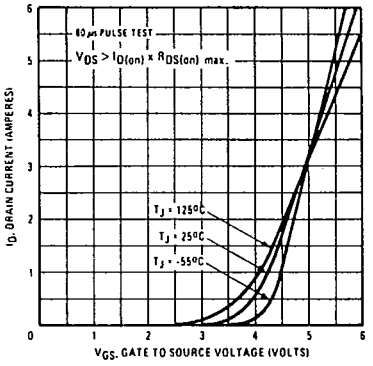

Fig. 3 – Typical Saturation Characteristics

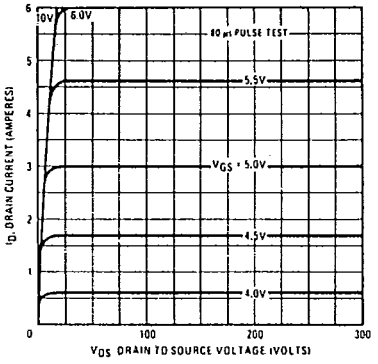

Fig. 4 — Forward Bias Safe Operating Area

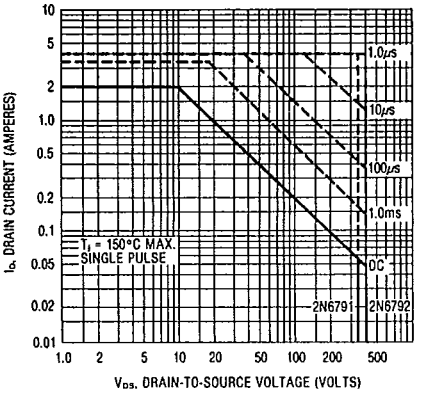

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Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

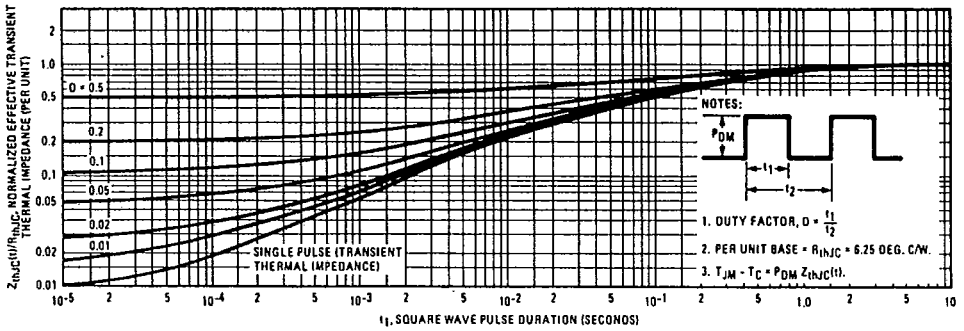

Fig. 6 – Typical Transconductance Vs. Drain Current

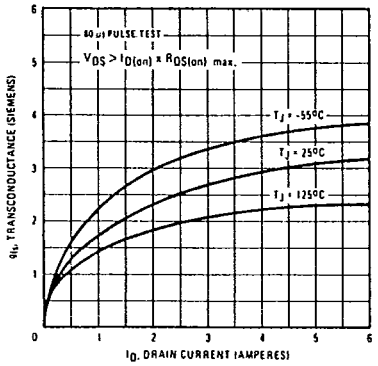

Fig. 7 – Typical Source-Drain Diode Forward Voltage

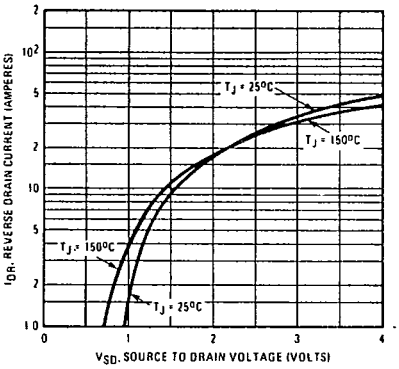

Fig. 8 – Breakdown Voltage Vs. Temperature

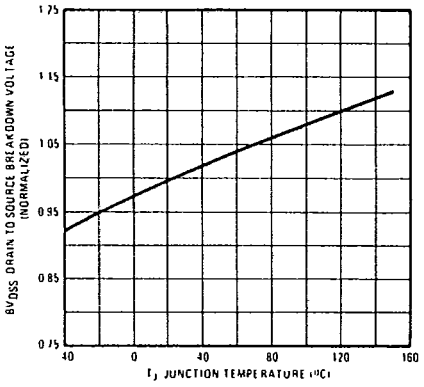

Fig. 9 – Normalized On-Resistance Vs. Temperature

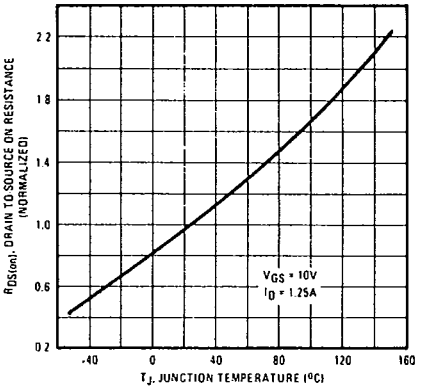

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Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

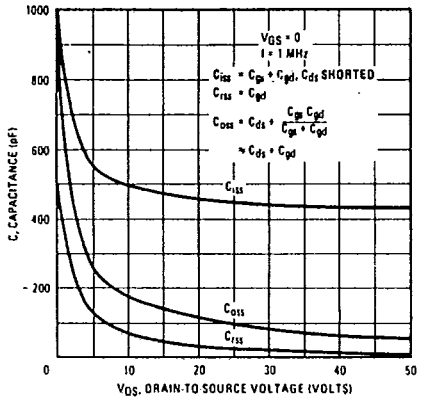

Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

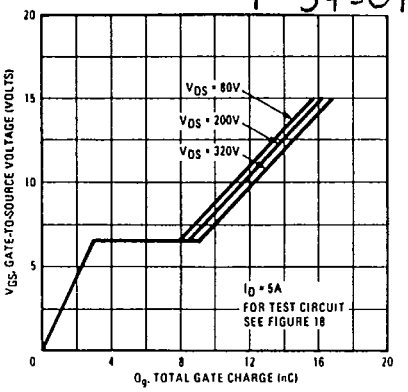

Fig. 12 – Typical On-Resistance Vs. Drain Current

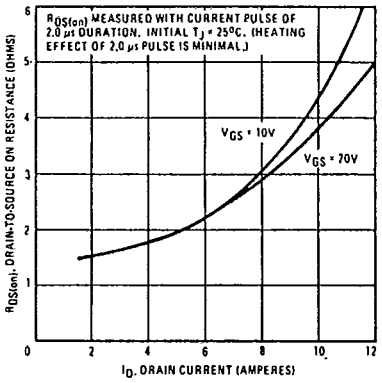

Fig. 13 – Maximum Drain Current Vs. Case Temperature

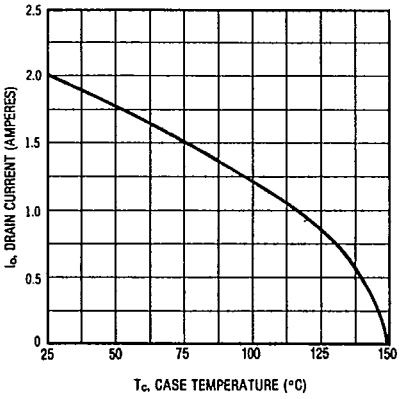

Fig. 14 – Power Vs. Temperature Derating Curve

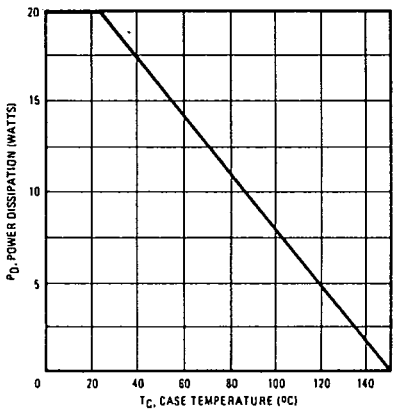

Fig. 15 – Clamped Inductive Test Circuit

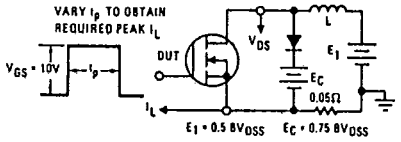

Fig. 16 – Clamped Inductive Waveforms

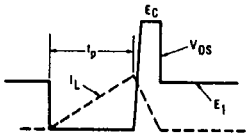

Fig. 17 – Switching Time Test Circuit

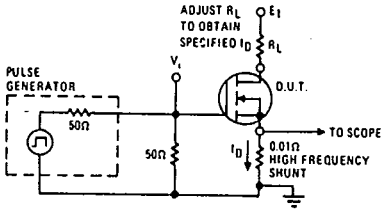

Fig. 18 – Gate Charge Test Circuit