

8M-WORD BY 64-BIT

VIRTUAL CHANNEL SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-45V8AD64S is a 8,388,608 words by 64 bits virtual channel synchronous dynamic RAM module (small outline DIMM) on which 8 pieces of 64M virtual channel SDRAM : μ PD4565161 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 64 bits organization
- Clock frequency and clock access time

Family	Read latency	Clock frequency (MAX.)	Clock access time (MAX.)	Maximum supply current				
				Operating			Refresh	
				Prefetch	Restore	Channel read / write (Burst)	Auto	Self
MC-45V8AD64S-A70	2	143 MHz	5.4 ns	460 mA		500 mA	680 mA	8 mA
★ MC-45V8AD64S-A75		133 MHz	5.4 ns	440 mA		480 mA	640 mA	
MC-45V8AD64S-A10		100 MHz	6 ns	420 mA		400 mA	560 mA	
★ MC-45V8AD64S-A15	1	66 MHz	12 ns	380 mA		340 mA	540 mA	
★ MC-45V8AD64S-A70L	2	143 MHz	5.4 ns	460 mA		500 mA	680 mA	3.2 mA
★ MC-45V8AD64S-A75L		133 MHz	5.4 ns	440 mA		480 mA	640 mA	
★ MC-45V8AD64S-A10L		100 MHz	6 ns	420 mA		400 mA	560 mA	
★ MC-45V8AD64S-A15L	1	66 MHz	12 ns	380 mA		340 mA	540 mA	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Programmable burst-length : 1, 2, 4, 8 or 16
- Programmable wrap sequence : Sequential or Interleave
- Prefetch read latency : 4
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V \pm 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles / 64 ms
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

The information in this document is subject to change without notice.

Ordering Information

Part number	Clock frequency (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
★ MC-45V8AD64S-A70	143 MHz	2	4	144-pin Small Outline DIMM (Socket type) Edge connector : Gold plated 26.67 mm (1.05 inch) height	8 pieces of μ PD4565161G5 (400 mil TSOP (II))
★ MC-45V8AD64S-A75	133 MHz				
★ MC-45V8AD64S-A10	100 MHz				
★ MC-45V8AD64S-A15	66 MHz	1			

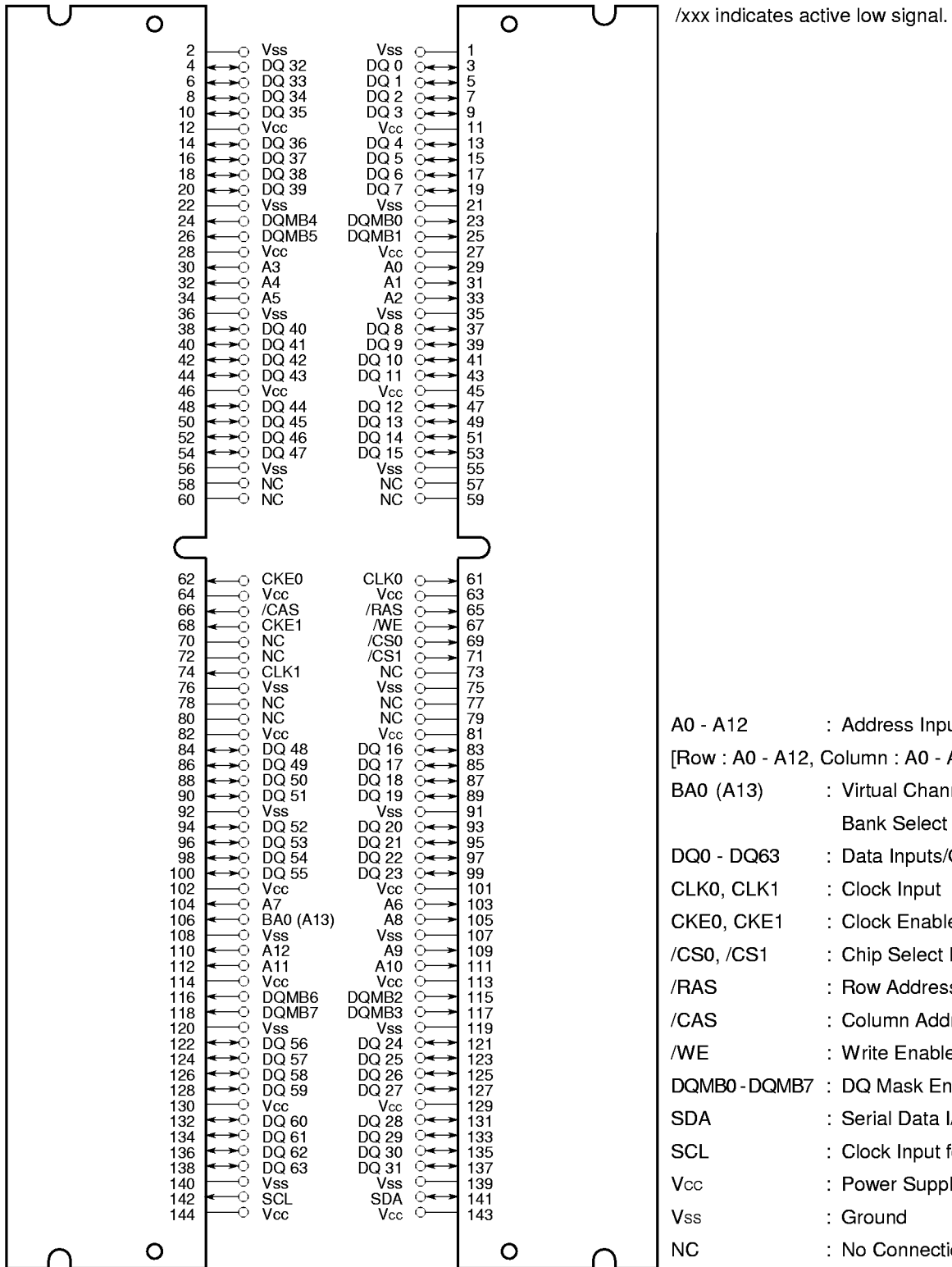
[Low Power Operation]

Part number	Clock frequency (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
★ MC-45V8AD64S-A70L	143 MHz	2	4	144-pin Small Outline DIMM (Socket type) Edge connector : Gold plated 26.67 mm (1.05 inch) height	8 pieces of μ PD4565161G5 (400 mil TSOP (II))
★ MC-45V8AD64S-A75L	133 MHz				
★ MC-45V8AD64S-A10L	100 MHz				
★ MC-45V8AD64S-A15L	66 MHz	1			

Pin Configuration

144-pin Small Outline Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

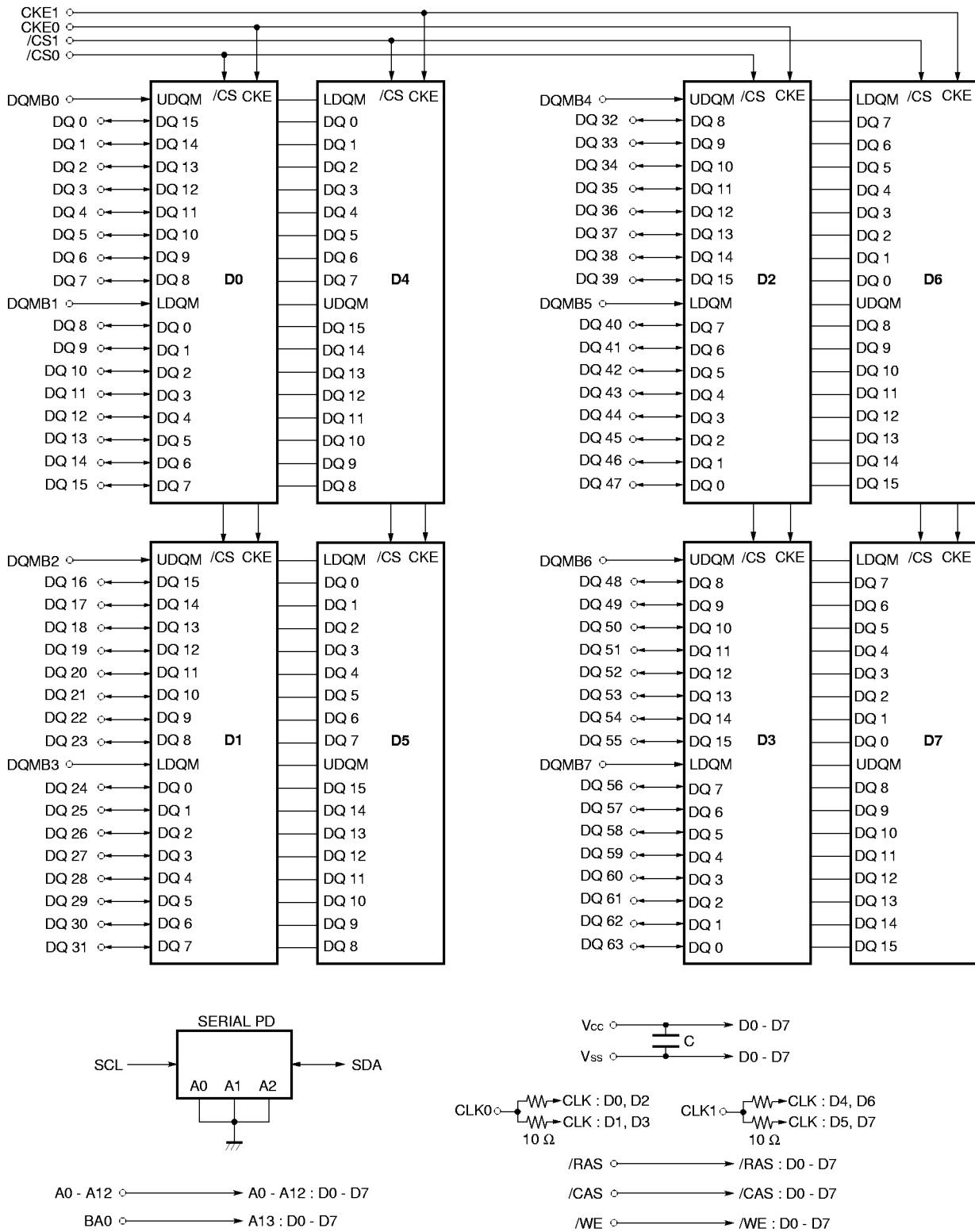
[MC-45V8AD64S]



/xxx indicates active low signal.

- A0 - A12 : Address Inputs
- [Row : A0 - A12, Column : A0 - A5]
- BA0 (A13) : Virtual Channel SDRAM Bank Select
- DQ0 - DQ63 : Data Inputs/Outputs
- CLK0, CLK1 : Clock Input
- CKE0, CKE1 : Clock Enable Input
- /CS0, /CS1 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- NC : No Connection

Block Diagram



Remark D0 - D7 : μ PD4565161 (2M words \times 16 bits \times 2 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μ s and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _T		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		8	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _I	A0 - A12, BA0 (A13), /RAS, /CAS, /WE, CLK0, CLK1, CKE0, CKE1, /CS0, /CS1, DQMB0 - DQMB7	TBD	TBD	TBD	pF
Data input/output capacitance	C _{I/O}	DQ0 - DQ63	TBD	TBD	TBD	pF

★ DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

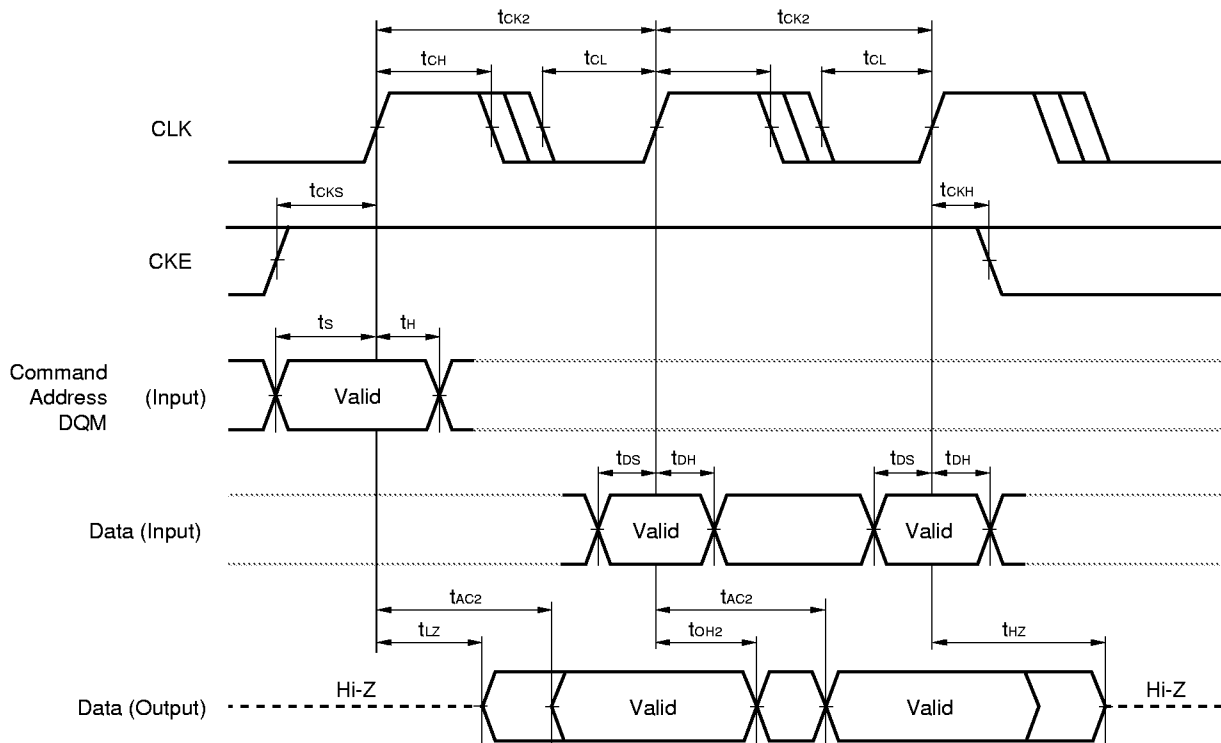
Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	I _{CC1P}	t _{RC} ≥ t _{RC(MIN.)} Prefetch is executed one time during t _{RC} .	-A70		460	mA	1
			-A75		440		
			-A10		420		
			-A15		380		
Operating current (Restore mode at one bank active)	I _{CC1R}	t _{RC} ≥ t _{RC(MIN.)}	-A70		460	mA	1
			-A75		440		
			-A10		420		
			-A15		380		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			8	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			4		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			200	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞ Input signals are stable.			64		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			40	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			32		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			200	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞ Input signals are stable.			80		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA Background : precharge standby	-A70		500	mA	2
			-A75		480		
			-A10		400		
			-A15		340		
Auto refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	-A70		680	mA	3
			-A75		640		
			-A10		560		
			-A15		540		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V	-A70		8	mA	
			-A75		8		
			-A10		8		
			-A15		8		
			-AxxL		3.2		
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-8	+8	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

- Notes 1.** I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
- 2.** I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
- 3.** I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

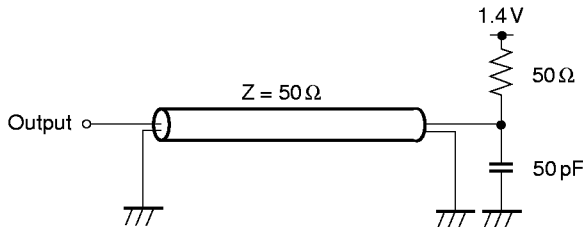
- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



★ AC characteristics

Parameter	Symbol	-A70		-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	t _{CK}	7	–	7.5	–	10	–	15	–	ns	
Access time from CLK	t _{AC}	–	5.4	–	5.4	–	6	–	12	ns	1
CLK high level width	t _{CH}	2.5	–	2.5	–	3	–	3	–	ns	
CLK low level width	t _{CL}	2.5	–	2.5	–	3	–	3	–	ns	
Data-out hold time	t _{OH}	2.7	–	2.7	–	3	–	3	–	ns	1
Data-out low-impedance time	t _{LZ}	0	–	0	–	0	–	0	–	ns	
Data-out high-impedance time	t _{HZ}	2.5	5.5	2.5	5.5	3	6	3	6	ns	
Data-in setup time	t _{DS}	2	–	2	–	2	–	2	–	ns	
Data-in hold time	t _{DH}	1	–	1	–	1	–	1	–	ns	
Address, Command, DQM setup time	t _S	2	–	2	–	2	–	2	–	ns	
Address, Command, DQM hold time	t _H	1	–	1	–	1	–	1	–	ns	
CKE setup time	t _{CKS}	2	–	2	–	2	–	2	–	ns	
CKE hold time	t _{CKH}	1	–	1	–	1	–	1	–	ns	
CKE setup time (Power down exit)	t _{CKSP}	2	–	2	–	2	–	2	–	ns	
Transition time	t _T	1	30	1	30	1	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}	–	64	–	64	–	64	–	64	ms	
Mode register set cycle time	t _{RSC}	2	–	2	–	2	–	2	–	CLK	

Note 1. Output load.



★ AC characteristics (Background to Background operation)

Parameter	Symbol	-A70		-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Same Bank Operation											
ACT to ACT / REF Command period	t _{RC}	70	–	75	–	80	–	90	–	ns	
REF to REF / ACT Command period	t _{RCF}	70	–	75	–	90	–	90	–	ns	
ACT to ACT / REF Command period (Prefetch to dummy channel and write to dummy channel with auto restore)	t _{RCPD}	119	–	120	–	160	–	165	–	ns	
ACT to PRE Command period	t _{RAS}	49	120,000	52	120,000	60	120,000	60	120,000	ns	
PRE to ACT / REF Command period	t _{RP}	20	–	20	–	20	–	30	–	ns	
ACT to PFC / PFCA / PFD / PPF / PPFA Command delay time	t _{APD}	15	–	15	–	20	–	30	–	ns	
ACT to PFR Command delay time (Prefetch read operation)	t _{APRD}	20	–	20	–	20	–	30	–	ns	
PFC to PRE Command delay time	t _{PPL}	21	–	22.5	–	30	–	30	–	ns	
PFCA / PFR to ACT / REF Command delay time	t _{PAL}	42	–	45	–	50	–	60	–	ns	
PPF to PRE Command delay time	t _{PPP}	42	–	45	–	60	–	75	–	ns	
PPFA to ACT / REF Command delay time	t _{PPA}	63	–	67.5	–	80	–	90	–	ns	
RST / RSTA to ACT (R) ^{Note1} Command delay time	t _{RAD}	7	28	7.5	30	10	40	10	60	ns	2
Data in to ACT / REF Command period (Write to dummy channel with auto restore)	t _{DAL}	77	–	82.5	–	110	–	120	–	ns	
Same, Other Bank Operation											
ACT (R) ^{Note1} to PFC / PFCA / PFR / PFD / PPF / PPFA Command delay time	t _{RPD}	35	–	37.5	–	40	–	45	–	ns	
PFC to PFC / PFCA Command delay time	t _{PPD}	21	–	22.5	–	30	–	30	–	ns	
PPF to PPF / PPFA Command delay time	t _{PPPD}	42	–	45	–	60	–	75	–	ns	
Other Bank Operation											
ACT to ACT / ACT (R) or ACT (R) to ACT Command delay time	t _{RRD}	14	–	15	–	20	–	30	–	ns	
ACT (R) to ACT (R) Command delay time	t _{RRDR}	28	–	30	–	40	–	45	–	ns	
PFC / PFCA to RST / RSTA Command delay time	t _{PRD}	21	–	22.5	–	30	–	30	–	ns	
PPF / PPFA to RST / RSTA Command delay time	t _{PPRD}	42	–	45	–	60	–	75	–	ns	

Notes 1. ACT (R) command is ACT command after RST command.

2. The another background operation and same channel foreground operation are illegal while t_{RAD} period.

★ AC characteristics (Foreground to Foreground operation)

Parameter	Symbol	-A70		-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
READ / WRITE to READ / WRITE Command delay time	t _{ccd}	7	–	7.5	–	10	–	15	–	ns	

★ AC characteristics (Background to Foreground operation)
(after same channel Prefetch / Restore)

Parameter	Symbol	-A70		-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
PFC / PFCA / PPF / PPFA to READ / WRITE and PFD to WRD / WRDA Command delay time	t _{pCD}	14	–	15	–	20	–	30	–	ns	
PPF / PPFA to READ / WRITE Command delay time (2nd prefetch channel read write)	t _{ppCD}	35	–	37.5	–	50	–	75	–	ns	
ACT (R) to READ / WRITE Command delay time	t _{rCD}	28	–	30	–	40	–	45	–	ns	1

Note 1. ACT (R) command is ACT command after RST command.

★ Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	08H	0	0	0	0	1	0	0	0	VC SDRAM	
3	Number of row addresses	0DH	0	0	0	0	1	1	0	1	13 rows	
4	Number of column addresses	06H	0	0	0	0	0	1	1	0	6 columns	
5	Number of banks	02H	0	0	0	0	0	0	1	0	2 banks	
6	Data width	40H	0	1	0	0	0	0	0	0	64 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface standard	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	Read latency (/CAS latency) = 2 cycle time	-A70	70H	0	1	1	1	0	0	0	0	7 ns
		-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
10	Read latency (/CAS latency) = 2 access time	-A70	55H	0	1	0	1	0	1	0	1	5.5 ns
		-A75	55H	0	1	0	1	0	1	0	1	5.5 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
11	DIMM configuration type	00H	0	0	0	0	0	0	0	0	None	
12	Refresh rate / type	80H	1	0	0	0	0	0	0	0	Normal	
13	VC SDRAM width	10H	0	0	0	1	0	0	0	0	×16	
14	Error checking SDRAM width	00H	0	0	0	0	0	0	0	0	None	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	1FH	0	0	0	1	1	1	1	1	1, 2, 4, 8, 16	
17	Number of banks on each VC SDRAM	02H	0	0	0	0	0	0	1	0	2 banks	
18	Read latency (/CAS latency) supported	03H	0	0	0	0	0	0	1	1	1, 2	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	VC SDRAM module attributes	00H	0	0	0	0	0	0	0	0		
22	VC SDRAM device attributes : general	0EH	0	0	0	0	1	1	1	0		
23	Read latency (/CAS latency) = 1 cycle time	-A70	00H	0	0	0	0	0	0	0	0	Not supported
		-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
24	Read latency (/CAS latency) = 1 access time	-A70	00H	0	0	0	0	0	0	0	0	Not supported
		-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
25-26		00H	0	0	0	0	0	0	0	0		
27	t _{RP} (MIN.)	-A70	14H	0	0	0	1	0	1	0	0	20 ns
		-A75	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns

(2/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
28	t _{RRD} (MIN.)	-A70	0EH	0	0	0	0	1	1	1	0	14 ns
		-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
29	t _{APD} (MIN.)	-A70	0FH	0	0	0	0	1	1	1	1	15 ns
		-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
30	t _{RAS} (MIN.)	-A70	31H	0	0	1	1	0	0	0	1	49 ns
		-A75	34H	0	0	1	1	0	1	0	0	52 ns
		-A10	3CH	0	0	1	1	1	1	0	0	60 ns
		-A15	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density	08H	0	0	0	0	1	0	0	0	32M bytes	
32	Address and command signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
33	Address and command signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal hold setup time	10H	0	0	0	1	0	0	0	0	1 ns	
36	Prefetch read latency	-A70	04H	0	0	0	0	0	1	0	0	4 clocks
		-A75	04H	0	0	0	0	0	1	0	0	4 clocks
		-A10	04H	0	0	0	0	0	1	0	0	4 clocks
		-A15	00H	0	0	0	0	0	0	0	0	Not supported
37	t _{PCD} (MIN.)	-A70	0EH	0	0	0	0	1	1	1	0	14 ns
		-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
38	Number of segment addresses	02H	0	0	0	0	0	0	1	0	2 bits	
39	Number of channels	04H	0	0	0	0	0	1	0	0	16	
40	Depth of channels	06H	0	0	0	0	0	1	1	0	64 bits	
41-61												
62	SPD revision	02H	0	0	0	0	0	0	1	0	2.0	
63	Checksum for bytes 0 - 62	-A70	DAH	1	1	0	1	1	0	1	0	
		-A75	E4H	1	1	1	0	0	1	0	0	
		-A10	31H	0	0	1	1	0	0	0	1	
		-A15	B5H	1	0	1	1	0	1	0	1	
64-71	Manufacturer's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacturer's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

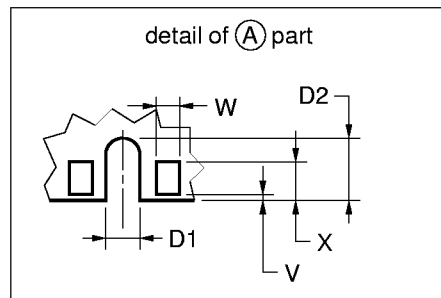
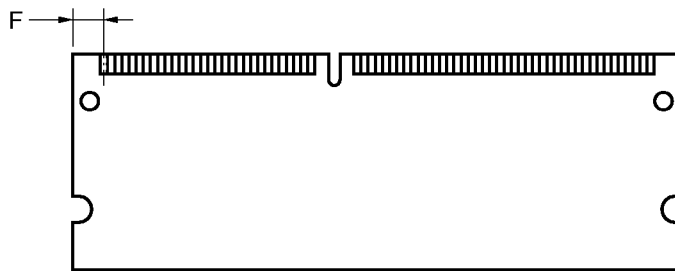
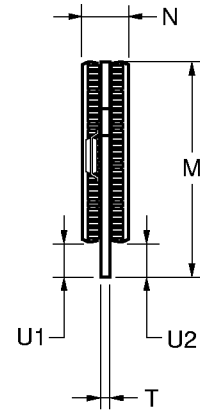
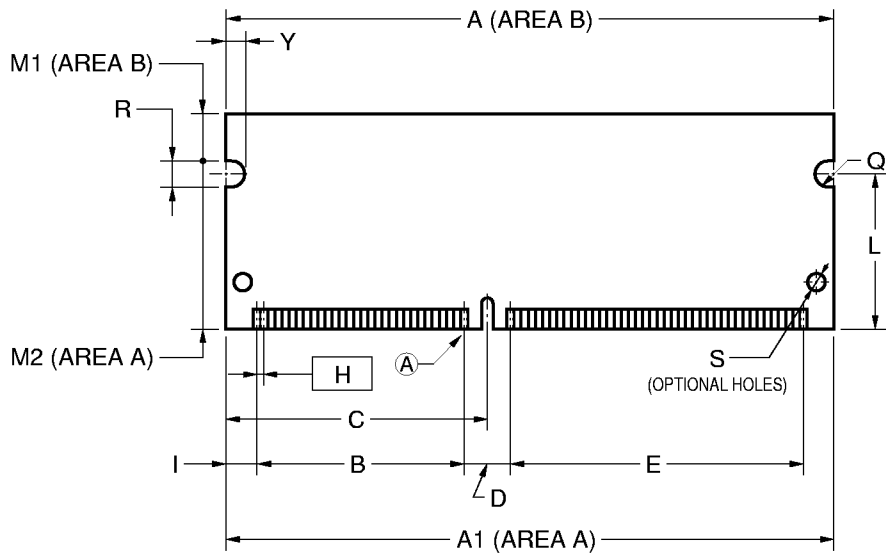
Timing Charts

Please refer to **NEC 64M-BIT VIRTUAL CHANNEL SDRAM SINGLE DATA RATE Data sheet.**

Package Drawing

[MC-45V8AD64S]

144 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	67.6
A1	67.6±0.15
B	23.2
C	29.0
D	4.6
D1	1.5±0.10
D2	4.0
E	32.8
F	3.7
H	0.8(T.P)
I	3.3
L	20.0
M	26.67±0.15
M1	4.67
M2	22.0
N	3.8 MAX.
Q	R2.0
R	4.0±0.10
S	φ1.8
T	1.0±0.1
U1	3.2 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	0.6±0.05
X	2.55 MIN.
Y	2.0 MIN.