

8-BIT 8-CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS

GENERAL DESCRIPTION

The UTC M62364 is a CMOS 8-bit, 8-ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI,CLK,LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0mA or more and can operate in a whole supply range from V_{DD} to GND.

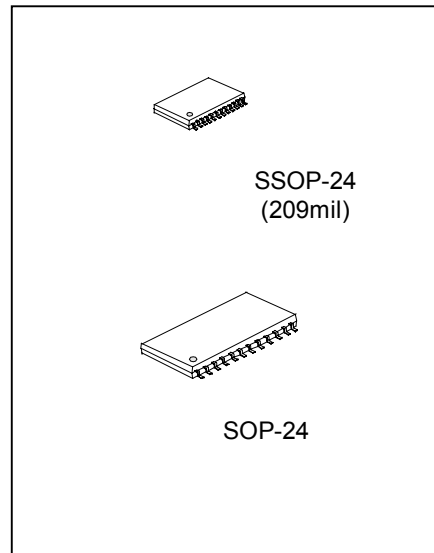
The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal Do for a cascading connection.

FEATURES

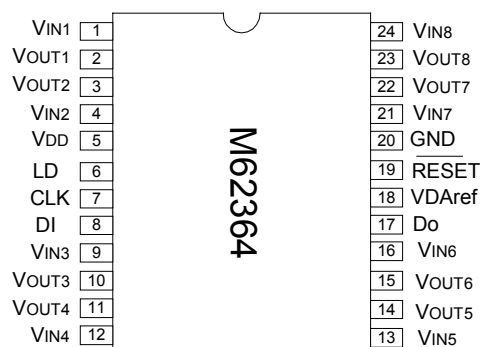
- *Three-wiring serial data transmission
- *Doubled precision 8-ch D/A converter employing an R-2R with higher-order segment method
- *8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- *4-quadrant multiplication

APPLICATION

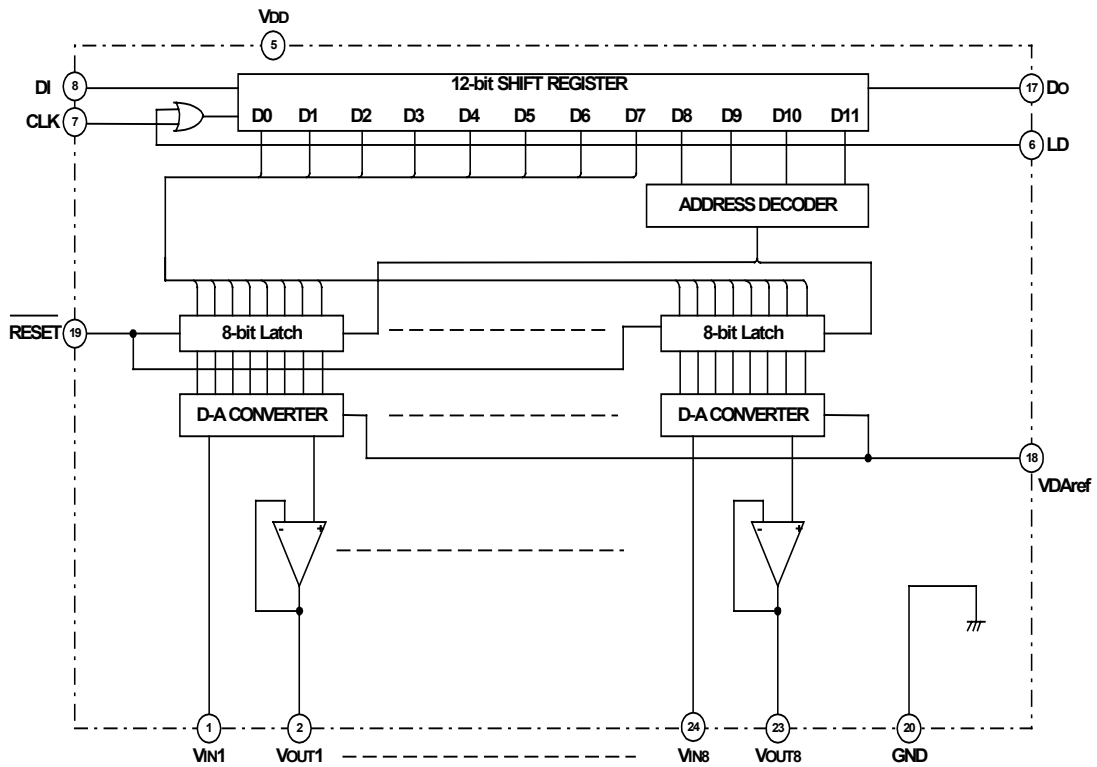
Digital to analog conversion for consumer and industrial equipment. Gain setting and automatic adjustment of display-monitor and CTV.



PIN CONFIGURATION (TOP VIEW)



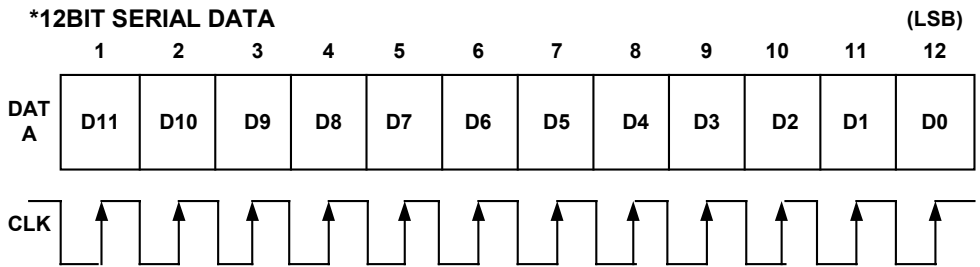
BLOCK DIAGRAM



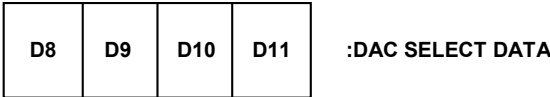
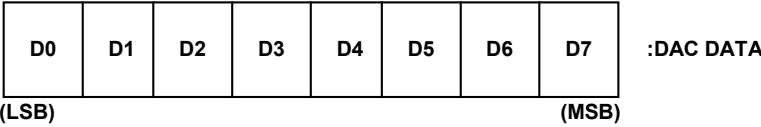
EXPLANATION OF TERMINALS

PIN No.	Symbol	Function
8	DI	Serial data input
17	DO	Serial data output
7	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock
6	LD	A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register
19	RESET	Reset 8-bit latches
2	VOUT1	D/A Converter Output with 8-bit resolution
3	VOUT2	
10	VOUT3	
11	VOUT4	
14	VOUT5	
15	VOUT6	
22	VOUT7	
23	VOUT8	
5	VDD	Power Supply
20	GND	Ground
1	VIN1	D/A Converter Input
4	VIN2	
9	VIN3	
12	VIN4	
13	VIN5	
16	VIN6	
21	VIN7	
24	VIN8	
18	VDAREF	D/A Converter Reference Voltage Input

DIGITAL FORMAT



*DATA ASSIGNMENT



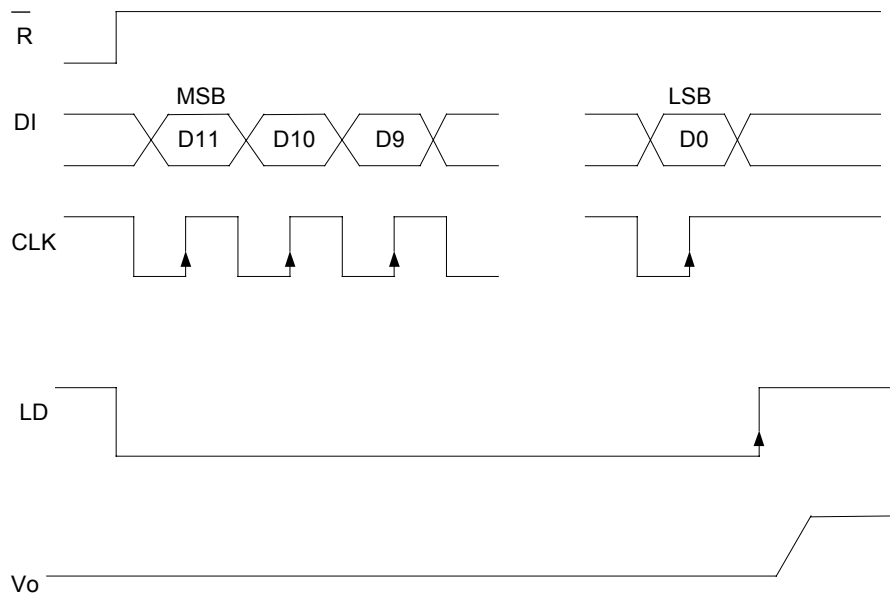
Dac Select Data

D8	D9	D10	D11	Dac Selection
0	0	0	0	Don't Care
0	0	0	1	VOUT1 Selection
0	0	1	0	VOUT2 Selection
0	0	1	1	VOUT3 Selection
0	1	0	0	VOUT4 Selection
0	1	0	1	VOUT5 Selection
0	1	1	0	VOUT6 Selection
0	1	1	1	VOUT7 Selection
1	0	0	0	VOUT8 Selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

*Digital Data Format

D0	D1	D2	D3	D4	D5	D6	D7	DAC OUTPUT
0	0	0	0	0	0	0	0	V_{DAref}
1	0	0	0	0	0	0	0	$(V_{IN}-V_{DAref})/256 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	$(V_{IN}-V_{DAref})/256 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	$(V_{IN}-V_{DAref})/256 \times 3 + V_{DAref}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	1	1	$(V_{IN}-V_{DAref})/256 \times 255 + V_{DAref}$

TIMING CHART



*Input data carried out LD signal Low besides CLK signal positive edge.
CLK, LD is keep generally HIGH level.

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	MEASUREMENT CONDITION	VALUE	UNIT
Supply Voltage	VDD		-0.3 ~ +7.0	V
Digital Input Voltage	VIND		-0.3 ~ +7.0	V
Analog Input Voltage	VIN		-0.3 ~ VDD+0.3	V
Analog Output Voltage	VOU		-0.3 ~ VDD+0.3	V
D-A Reference Voltage	VDAREF		-0.3 ~ VDD+0.3	V
Operating Temperature	Topr		-20 ~ +75	°C
Storage Temperature	Tstg		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

< Ana/Dig Common Part > (VDD=5V±10% , VDD≥ VIN,GND,VDAREF=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	MEASUREMENT CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Supply Voltage	VDD		2.7	3.0	3.6	V
Supply Current	IDD	CLK=1MHz,Vcc=3V,IAO=0μ A			3.5	mA

< Digital Part > (VDD=5V±10% , VDD≥ VIN,GND,VDAREF=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Input Leak Current	IILK	VIN=0 ~VDD	-10		10	μ A
Digital Input "Low" Voltage	IIL				0.2 VDD	V
Digital Input "High" Voltage	IiH		0.8VDD			V
Do Terminal Output "Low" Voltage	VOL	IOL=2.5mA			0.4	V
Do Terminal Output "High" Voltage	VOH	IOH=-400μ A	VDD-0.4			V

< Analog Part > (VDD=5V±10% , VDD≥ VIN,GND,VDAREF=0V,Ta=-20~85°C unless otherwise noted)

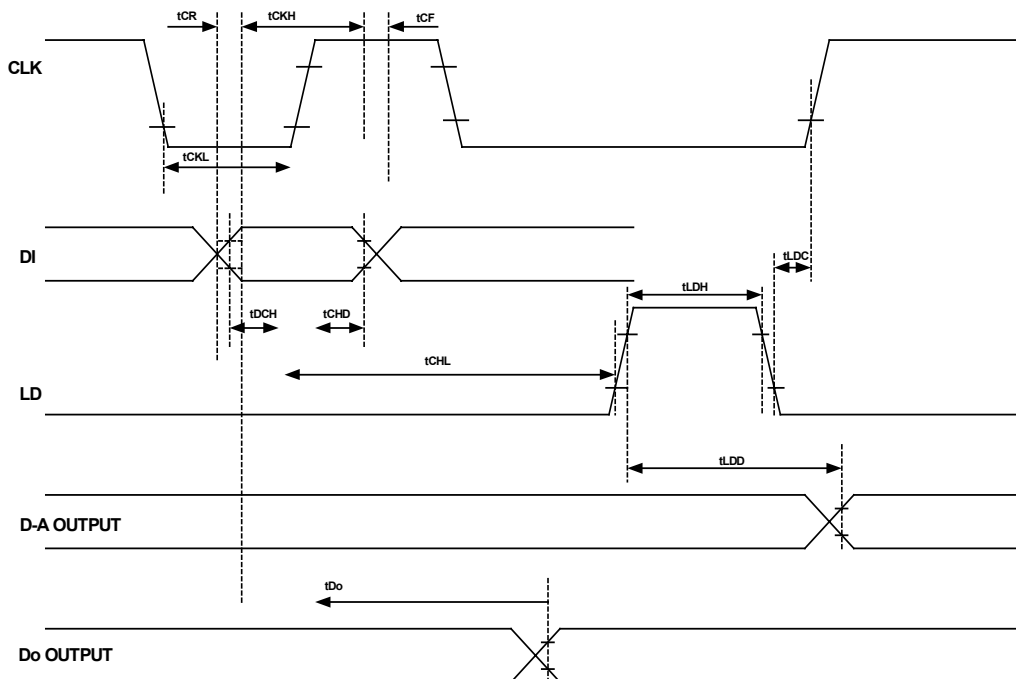
PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Input Current	IIN	VIN=3V,VDAREF=0V, *Proportional to max. input current condition(VIN-VDAREF) and digital data of each channels.			0.18	mA
D-A Reference Input Current	IDAREF	VIN=3V,VDAREF=0V, *Proportional to max. input current condition(VIN-VDAREF) and digital data of each channels	-1.44			mA
Resolution	RES	VDD=2.61V,VDAREF=0.050V (10mV/1LSB)		8		bit
Differential Nonlinearity	DNL	Without Load(IAO=±0)	-1		1	LSB
Nonlinearity	NL		-1.5		1.5	LSB
Buffer Amplifier Output Voltage Range	VAO	IAO=±100μ A	0.1		Vcc-0.1	V
		IAO=±500μ A	0.2		Vcc-0.2	
Buffer Amplifier Output Current Range	IAO	Upper Saturation Voltage=0.4V Lower Saturation Voltage=0.4V	-1		1	mA

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Output Capacitive Load	Co				0.1	μ F
Buffer Amplifier Output Impedance	Ro			5		Ω

< AC Characteristics > ($V_{DD}=5V\pm 10\%$, $V_{DD}\geq V_{IN,GND}, V_{Dref}=0V, T_a=-20\sim 85^{\circ}C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Clock "L" Pulse Width	tCKL		200			ns
Clock "H" Pulse Width	tCKH		200			ns
Clock Rise Time	tCR				200	ns
Clock Fall Time	tCF					
Data Set Up Time	tDCH		60			ns
Data Hold Time	tCHD		100			ns
LD Set Up Time	tCHL		200			ns
LD Hold Time	tLDC		100			ns
LD "H" Pulse Duration Time	tLDH		100			ns
Data Output Delay Time	tDo	CL=100pF	70		350	ns
D-A Output Setting Time	tLDD	CL $\leq$ 100pF, VAO:0.1 <=> 2.6V This Time Until The Output Becomes The final Value Of 1/2 LSB			300	μ s

TIMING CHART



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