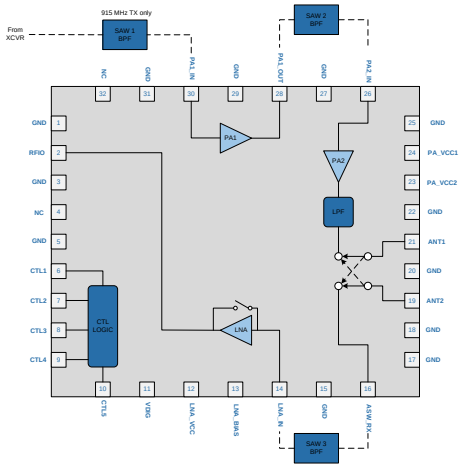
RFMD + TriQuint = Qorvo

RFFM6901

2.8V to 4.2V, 915MHz ISM Band Transmit/Receive Module with Diversity Switch

The RFFM6901 is a single-chip front end module (FEM) for application in the 868MHz and 915MHz ISM Bands. The RFFM6901 addresses the need for aggressive size reduction for typical portable equipment RF front end designs and greatly reduces the number of components outside of the core chipset thus minimizing the footprint and assembly cost of the overall solution. The RFFM6901 contains an integrated 1W PA, dual port diversity antenna switch, LNA with bypass mode, and matching components. The RFFM6901 is packaged in a 32-pin, 6.0mm x 6.0mm x 1.2mm over-molded laminate package.



Functional Block Diagram

Package: LGA, 32-pin, 6.0mm x 6.0mm

Features

- Tx Output Power: 30dBm
- Separate Rx/Tx 50Ω Transceiver Interface
- Antenna Diversity Switch
- LNA with Bypass Mode

Applications

- Wireless Automated Metering
- Wireless Alarm Systems
- Portable Battery Powered Equipment
- Smart Energy
- 868MHz/915MHz ISM Band Application
- Single Chip RF Front End Module

Ordering Information

RFFM6901SB	Standard 5-piece bag
RFFM6901SQ	Standard 25-piece bag
RFFM6901SR	Standard 100-piece reel
RFFM6901TR13	Standard 2500-piece reel
RFFM6901PCK-410	Fully assembled evaluation board w/ 5-piece bag

Absolute Maximum Ratings

Parameter	Rating	Unit
Voltage	5.25	VDC
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range	-40 to +85	°C
Maximum Input Power to PA, pin 30, 2 (no damage)	+5	dBm
Maximum Input Power to PA, pin 26(no damage)	+23	dBm
Maximum Input Power to LNA, pin 19, 21 (no damage)	+10	dBm
Moisture Sensitivity Level	MSL3	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Overall					
Active Frequency	868	902 to 928		MHz	PA and LNA
RF Port Impedance		50		Ω	
ESD, Human Body Model	500			V	RF Pins
	500			V	All Other Pins
ESD, Charge Device Model	500			V	RF Pins
	500			V	All Other Pins
PA Section					
Transmit Mode 4V (High Bias)					PA V_{CC} = V_{DIG} = 4.0V, LNAV_{CC} = 0V, CTL1 = CTL4 = CTL5 = 3.8V, CTL2 = CTL3 = 0V.
Power Supply Operation Voltage-High	3.8	4	4.2	V	PA V_{CC}
Input Power		0	5	dBm	Pin 30
CW Output Power-near saturation (ANT1/2) at 4.0V	31	31.5		dBm	
Output Power (ANT1/2) at 4.0V	30	30.5		dBm	
Thermal Resistance	39.83			C°/W	V_{CC} = V_{DIG} = 4.0V, LNAV_{CC} = 0V, CTL1 = CTL4 = CTL5 = 3.8V, CTL2 = CTL3 = 0V, P_{OUT} = 30.1dBm, Modulation = CW, Freq = 902MHz, DC = 100%, T = 85°C
1W Current (ANT1/2) at 4.0V at P_{OUT} = 30dBm		600	700	mA	
1/2W Current (ANT1/2) at 4.0V at P_{OUT} = 27dBm	415	450	490	mA	
1/4W Current (ANT1/2) at 4.0V at P_{OUT} = 24dBm	310	340	370	mA	
Large Signal Gain Overall High Bias (ANT1/2) at 4.0V	27	30	33	dB	
Large Signal Gain Overall Low Bias (ANT1/2) at 4.0V	22	25	28	dB	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Large Signal Gain PA2 High Bias (ANT1/ANT2) at 4.0V	12	14		dB	
PA PAE		64		%	PA V_{CC} = V_{DIG} = 3.6V, P_{OUT} = 30.1dBm
Transmit Mode 3V (Low Bias)					PA V_{CC} = V_{DIG} = 3.0V, $LNAV_{CC}$ = 0V, CTL1 = CTL4 = 2.8V, CTL2 = CTL3 = CTL5 = 0V.
Power Supply Operation Voltage-Low	2.8	3.0	3.2	V	PA V_{CC}
Input Power			5	dBm	
CW Output Power-near saturation (ANT1/2) at 3.0V	27.5	28		dBm	
Output Power (ANT1/2) at 3.0V	26.5	27		dBm	V_{CC} = 3.0V, P_{OUT} at ANT1 and ANT2
1/2W Current (ANT1/2) at 3.0V at P_{OUT} = 27dBm	400	450	500	mA	
1/4W Current (ANT1/2) at 3.0V at P_{OUT} = 24dBm	300	340	375	mA	
Quiescent current		12		mA	PA V_{CC} = V_{DIG} = 3.0V
		25		mA	PA V_{CC} = V_{DIG} = 3.6V
2nd Harmonic (ANT1/2) High Voltage (4.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT1/2) High Voltage (4.0V) 30dBm P_{OUT}			-71	dBc	
2nd Harmonic (ANT1/2) Low Voltage (3.0V) 30dBm P_{OUT}			-32	dBc	
3rd to 10th Harmonic (ANT1/2) Low Voltage (3.0V) 30dBm P_{OUT}			-71	dBc	
Input Return Loss (PA1-ANT1/2)High Voltage (4.0V)		-10		dB	Measured at PA-IN Port at Pin 30
Input Return Loss (PA1-ANT1/2)Low Voltage (3.0V)		-10		dB	
PA Leakage Current		0.5	5	µA	PA V_{CC} = 4.2V, PD SEL Logic = 0.0V
Noise Power at ANT ½ -Electric only at -8MHz Offset from carrier		-132		dBm/Hz	PA_V_{CC} voltage of 4.2V and P_{OUT} = +28dBm, PA2 only zero noise contribution from PA1
RX Section					
LNA Mode (High Bias)					$LNAV_{CC}$ = V_{DIG} = 4.0V, PA V_{CC} = 0V, CTL1 = CTL2 = CTL3 = CTL4 = 3.8V, CTL5 = 0V. Pin 13 floating
Operating Voltage	2.7	4.0	4.2	V	
Gain at High Bias	15	17		dB	LNA_V_{CC} = 3.3 to 4.2V; LNA Bias = High Bias, PI = -40 to -10 dBm
	13	15		dB	LNA_V_{CC} = 2.7V; LNA Bias = High Bias, PI = -40 to -10 dBm
Noise Figure at High Bias		1.5	2	dB	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = High Bias
		1.5	2	dB	LNA_V_{CC} = 2.7V LNA Bias = High Bias
Input IP3 at High Bias	3	5		dBm	LNA_V_{CC} = 4.2V; LNA Bias = High Bias
	2	5		dBm	LNA_V_{CC} = 2.7V LNA Bias = High Bias
Input P1dB		-5		dBm	LNA_V_{CC} = 3.3 to 4.2V; LNA Bias = High Bias
Input Return Loss	10			dB	Measured at LNA-IN Port at Pin 14
Output Return Loss	10			dB	Measured at RFIO 900 Pin 2
Power Supply Current	6	8	10	mA	LNA_V_{CC}
LNA Mode (Low Bias)					$LNAV_{CC}$ = V_{DIG} = 4.0V, PA V_{CC} = 0V, CTL1 = CTL2 = CTL3 = CTL4 = 3.8V, CTL5 = 0V. 51KΩ pull-down resistor from pin 13 to ground
Gain at Low Bias	13	15		dB	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias

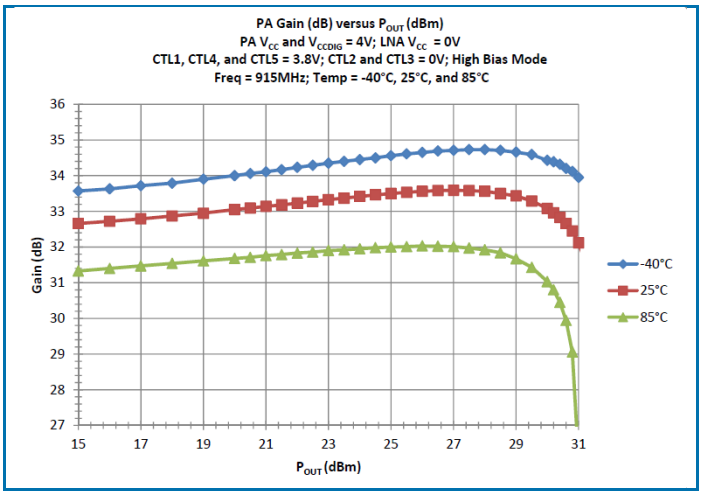
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
	9	12		dB	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias
Noise Figure at Low Bias		2.5	3.5	dB	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias
		3	4	dB	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias
Input IP3 at LB	-1	1		dBm	LNA_V_{CC} = 3.3V to 4.2V; LNA Bias = Low Bias
Rx LNA Bypass Mode		-5		dBm	LNA_V_{CC} = 2.7V; LNA Bias = Low Bias
Power Supply Current	3	3	4	mA	LNA_V_{CC} = 3.6V
Rx LNA Bypass Mode					LNAV_{CC} = V_{DIG} = 4.0V, PA V_{CC} = 0V, CTL1 = CTL2 = CTL4 = 3.8V, CTL3 = CTL5 = 0V.
Operating Voltage	2.7	4.0	4.2	V	LNA_V_{CC}
Gain	-3.0	-2.5	-2.0	dB	
Input Ip3	12	18		dBm	
Input Return Loss	10			dB	
Output Return Loss	10			dB	
Power Supply Current		1	2	mA	
LNA Leakage Current		0.5	5.0	µA	LNA_V_{CC} = 4.2, PD_SEL = LOW
Antenna Switch Section					
Insertion Loss TX-ANT1/2		0.8	1.0	dB	
Insertion Loss ANT1/2- ASWRX		1.0	1.25	dB	
Isolation	20			dB	
Tx Return Loss	10	15		dB	
Logic					
Control Logic HIGH	2.5		4.0	V	Max Control Logic HIGH = Vcc +/- 0.2VDC
Control Logic LOW	0.0	0.2	0.3	V	

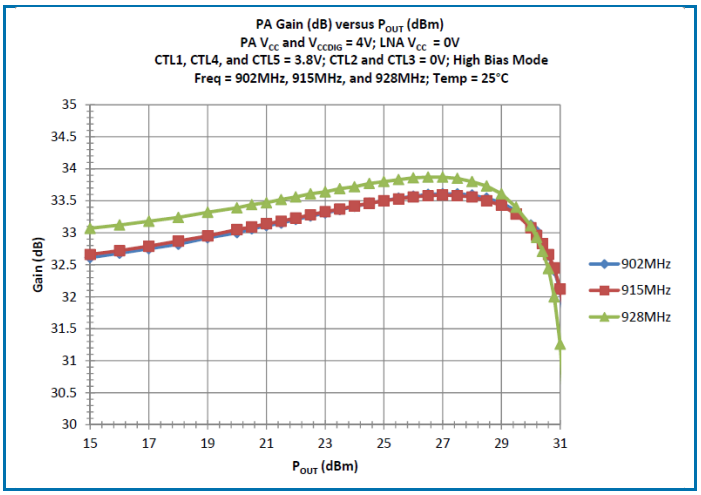
Switch Control Table

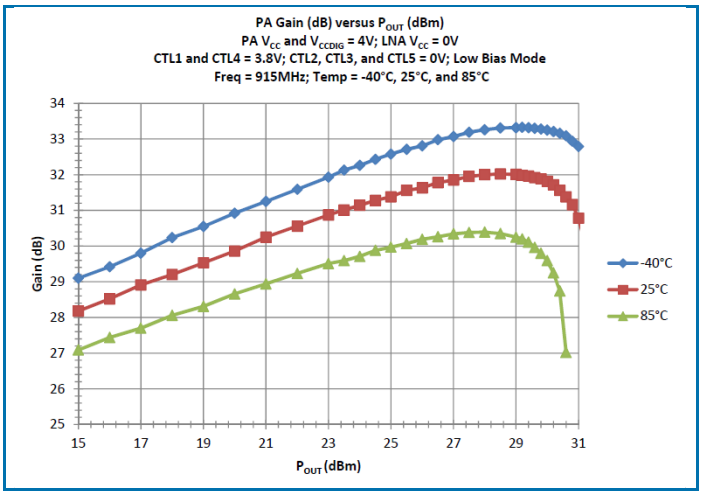
Operating Mode	CTL1(ANT Select)	CTL2(TxRx Select)	CTL3(LNA Select)	CTL4(PD Select)	CTL5(PA_High Bias)
Tx to ANT1 LOW BIAS	1	0	0	1	0
Tx to ANT2 LOW BIAS	0	0	0	1	0
Rx from ANT1 HIGH/LOW BIAS*	1	1	1	1	0
Rx from ANT2 HIGH/LOW BIAS*	0	1	1	1	0
Rx from ANT1 LNA Bypass	1	1	0	1	0
Rx from ANT2 LNA Bypass	0	1	0	1	0
Tx ANT1 HIGH BIAS	1	0	0	1	1
Tx ANT2 HIGH BIAS	0	0	0	1	1

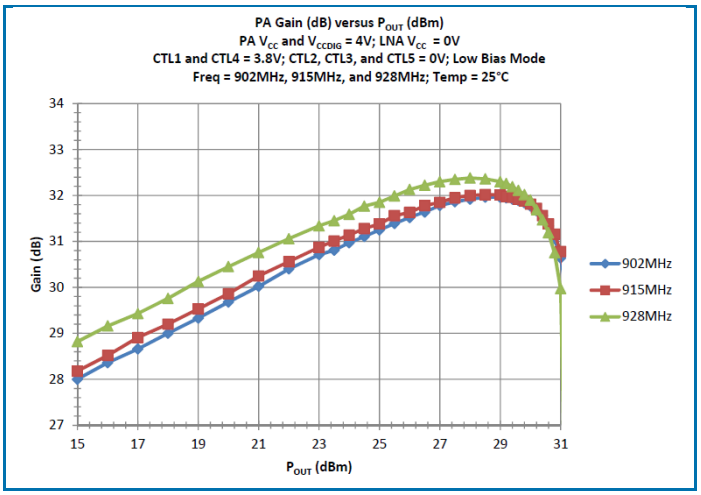
* The difference between Rx Mode High Bias and Rx Mode Low Bias is with Low Bias there is a 51KΩ pull-down resistor from pin 13 to ground while High Bias leaves pin 13 floating.

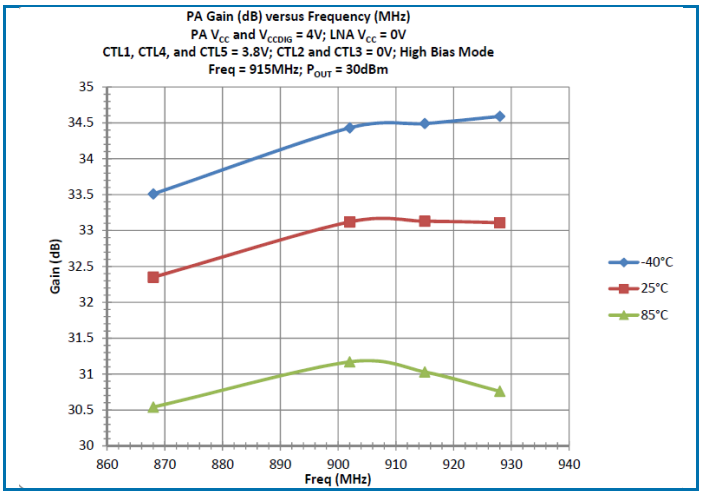
Performance Plots

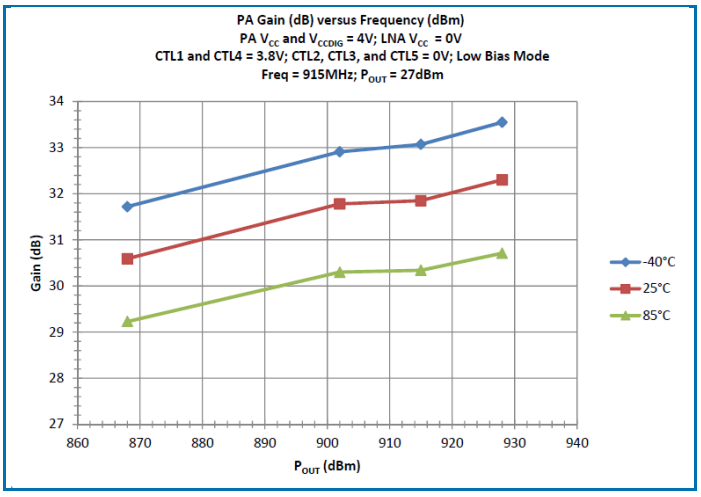


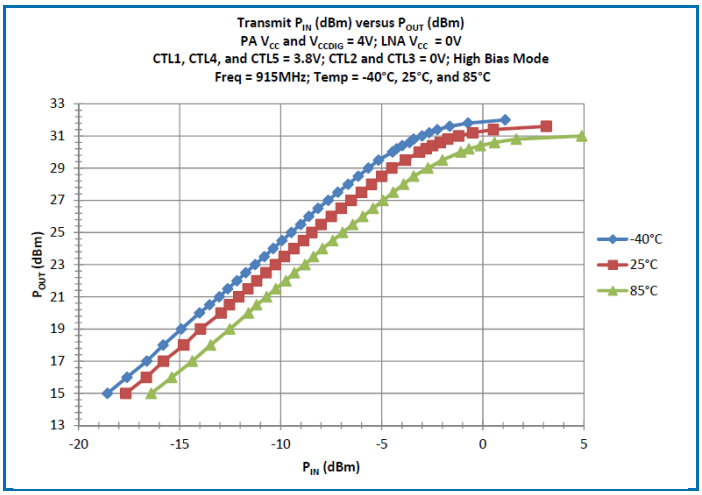


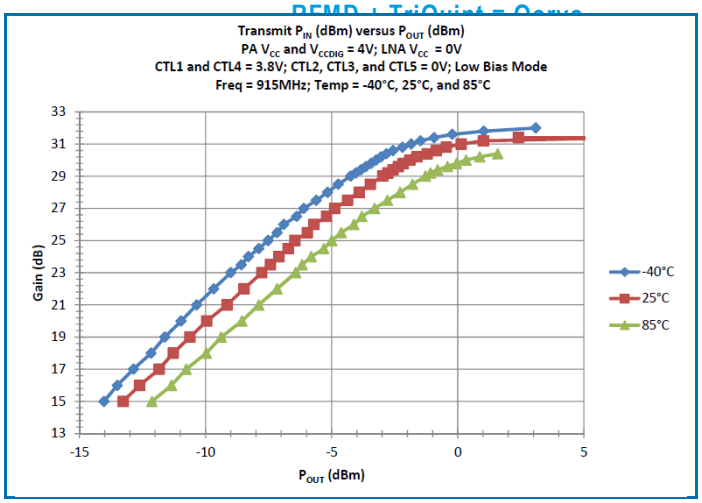


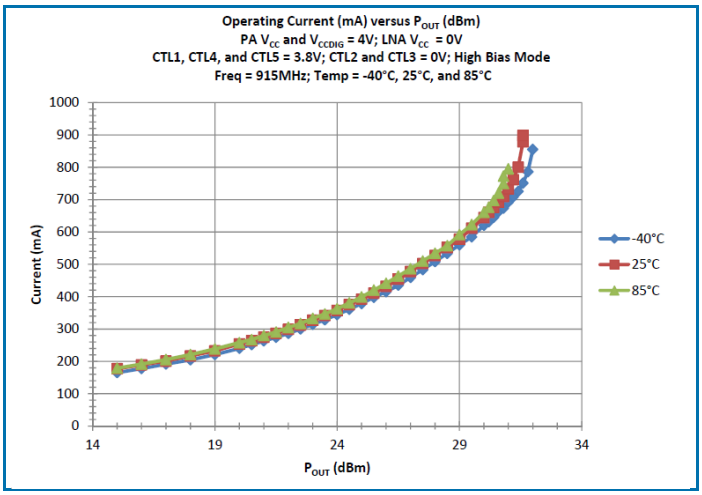


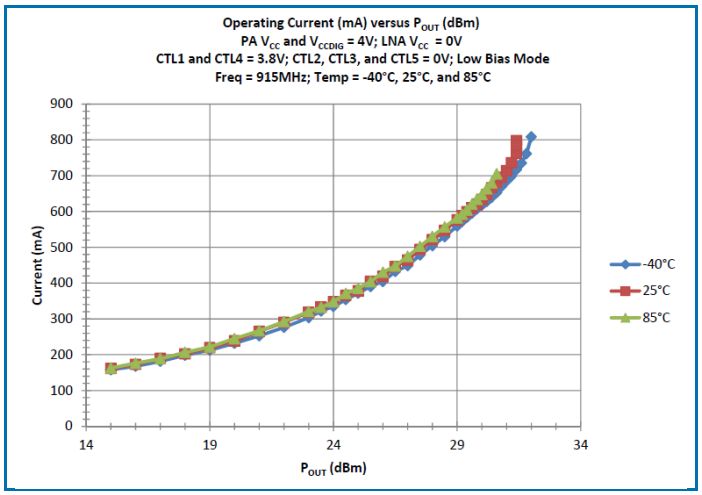


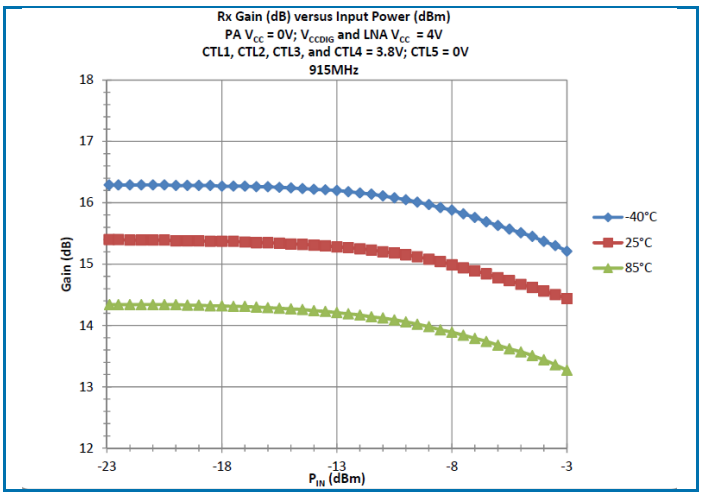


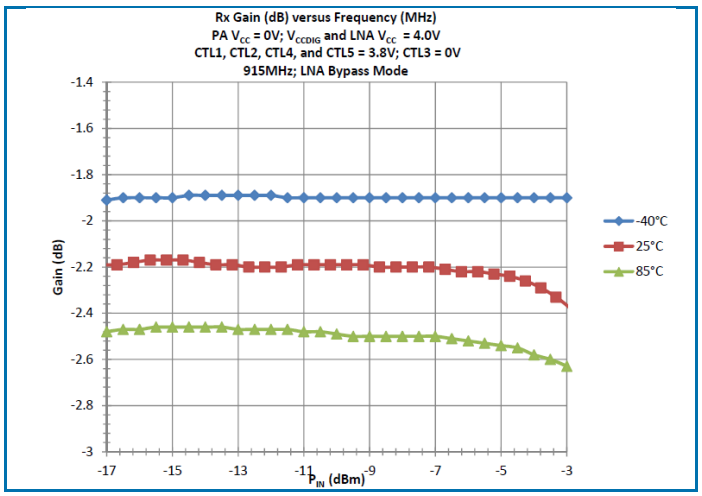


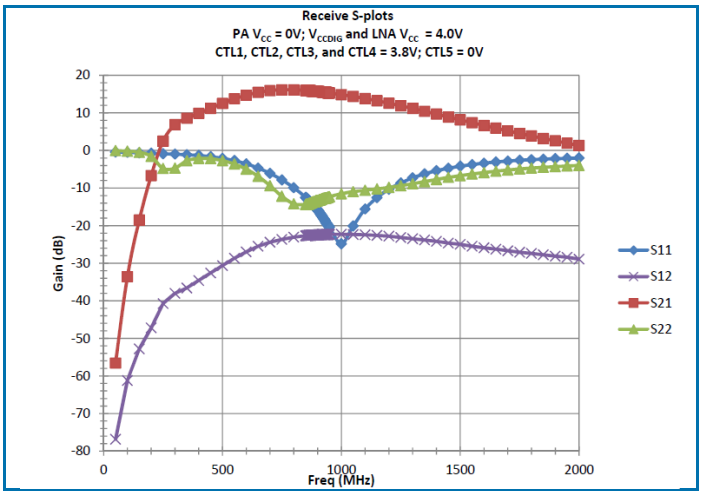


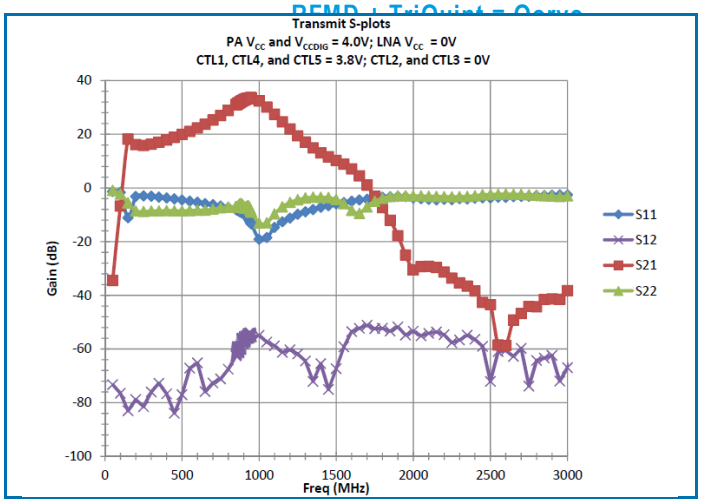




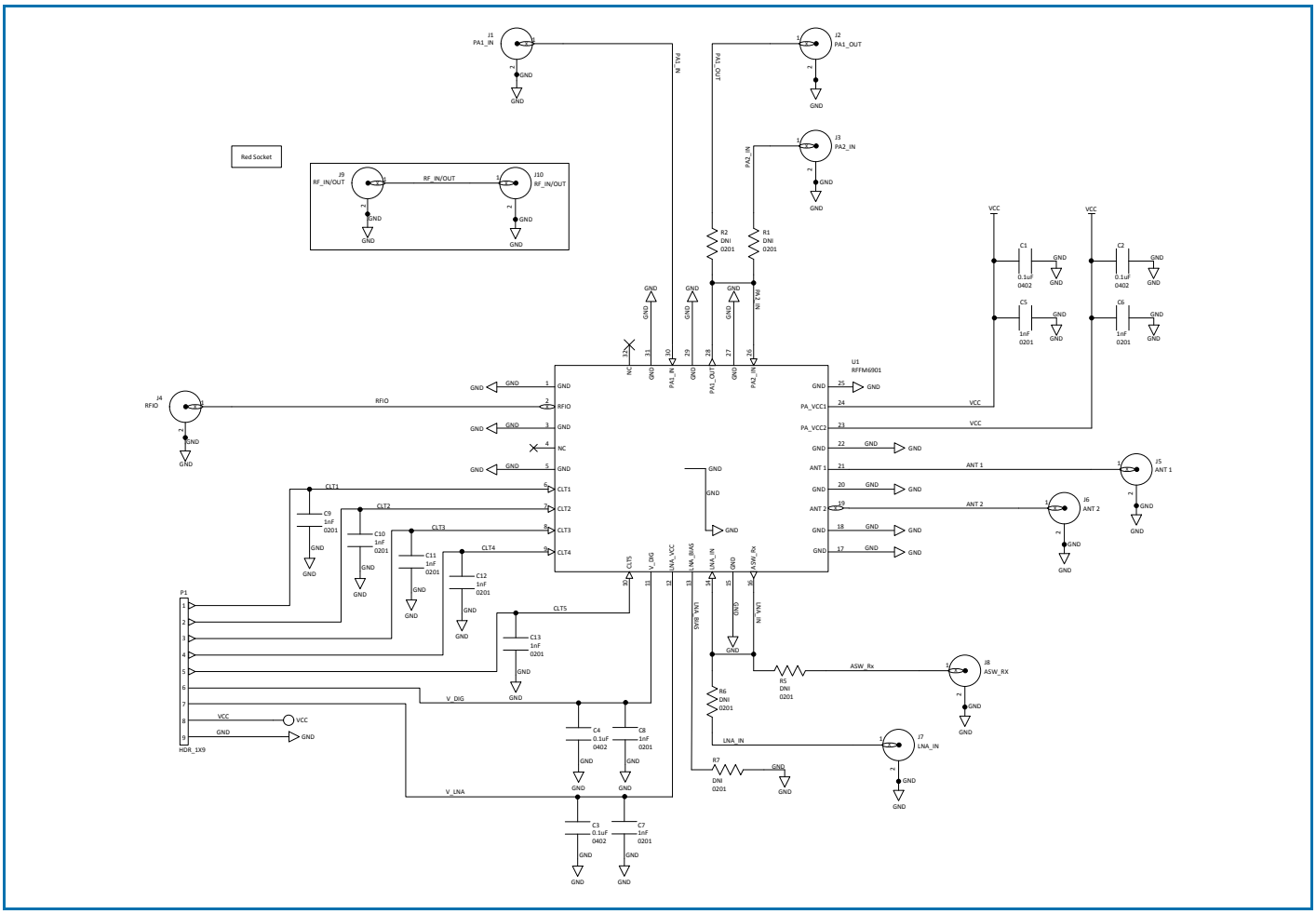






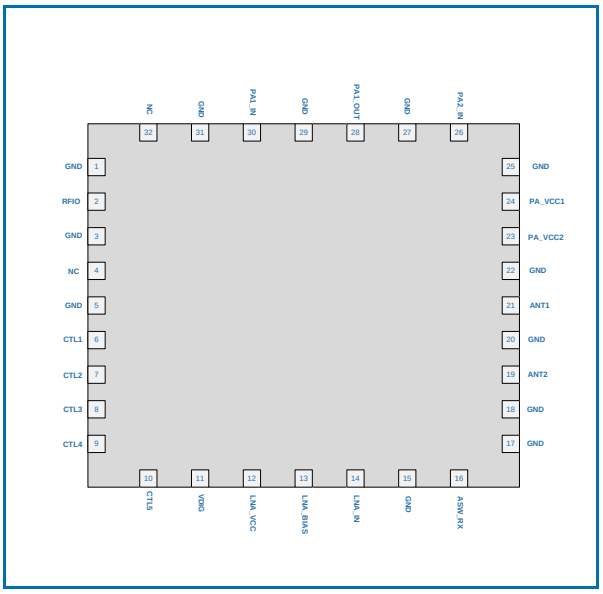


Evaluation Board Schematic

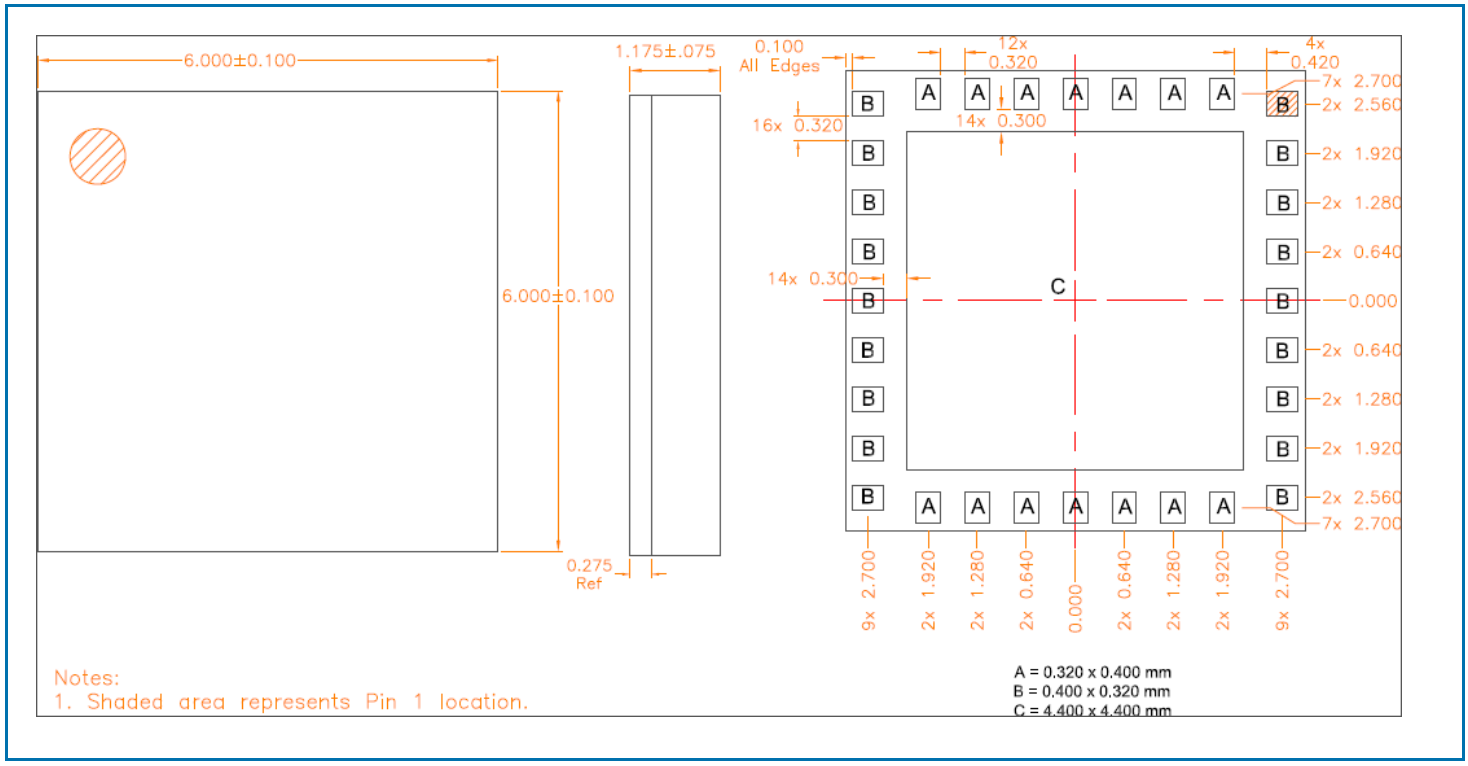


RFMD + TriQuint = Qorvo

Pin Out

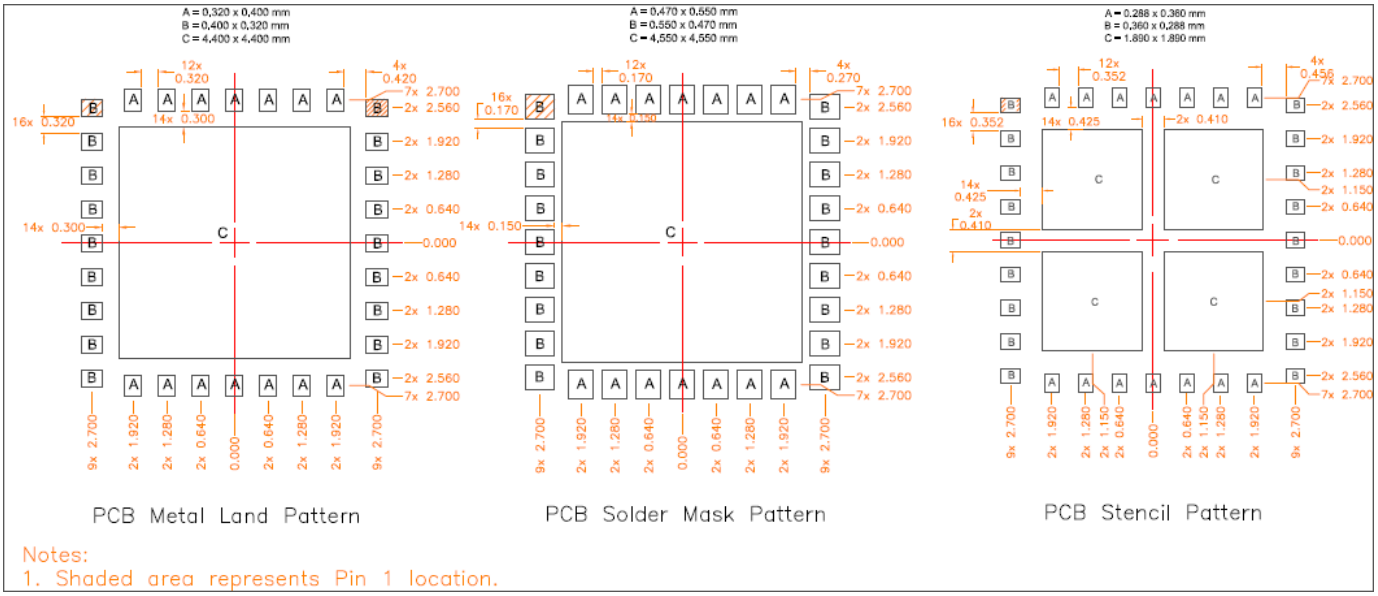


Package Drawing



PCB Patterns

RFMD + TriQuint = Qorvo



Pin Names and Descriptions

Pin	Name	Description
1	GND	Ground.
2	RX	868MHz/900MHz Receive, Internally DC Blocked.
3	GND	Ground.
4	NC	Not Connected in FEM.
5	GND	Ground.
6	CTL1	ANT Select.
7	CTL2	TxRx Select.
8	CTL3	LNA Select.
9	CTL4	PD Select.
10	CTL5	PA_High Bias.
11	VDIG	Digital V_{CC}.
12	LNA_VCC	LNA V_{CC}.
13	LNA_BIAS	LNA linearity bias (Place SMD Resistor to GND to Lower LNA I_{DD}).
14	LNA_IN	LNA Signal Input, Internally DC Blocked.
15	GND	Ground.
16	ASW_RX	Antenna Switch Receive Output, Internally DC Blocked.
17	GND	Ground.
18	GND	Ground.
19	ANT2	Antenna 2 Output/Input, Internally DC Blocked.
20	GND	Ground.
21	ANT1	Antenna 1 Output/Input, Internally DC Blocked.
22	GND	Ground.
23	PA VCC2	PA Battery Bias for Second Stage.
24	PA VCC1	PA Battery Bias for First Stage.
25	GND	Ground.
26	PA2_IN	Power Amplifier 2nd Stage Signal Input Port.
27	GND	Ground.
28	PA1_OUT	Power Amplifier 1st Stage Signal Output Port, Internally DC Blocked.
29	GND	Ground.
30	PA1_IN	Power Amplifier 1st Stage Signal Input Port, Internally DC Blocked.
31	GND	Ground.
32	NC	Not connected in FEM.