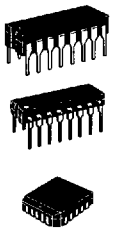
PECL* to TTL Translator
(+5 Vdc Power Supply Only)

MC10H350

The MC10H350 is a member of Motorola's 10H family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3–state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the H350 to be used as an inverting or noninverting translator, or a differential line receiver. The H350 can also drive CMOS with the addition of a pullup resistor.

- Propagation Delay, 3.5 ns Typical
- MECL 10K–Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

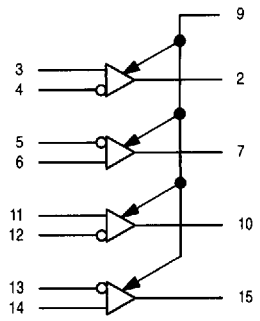
P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (VEE = Gnd)	V_{CC}	7.0	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C °C

LOGIC DIAGRAM



V_{CC} (+5.0 VDC) = PINS 1 AND 16
GND = PIN 8

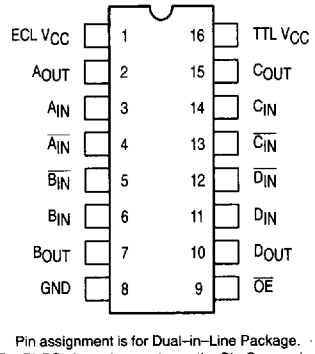
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Note 1)

Characteristic		Symbol	T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
Power Supply Current	TTL ECL	I_{CC}	— —	20 12	mA
Input Current High	Pin 9 Others	I_{IH} I_{INH}	— —	20 50	µA
Input Current Low	Pin 9 Others	I_{IL} I_{INL}	— —	–0.6 50	mA µA
Input Voltage High	Pin 9	V_{IH}	2.0	—	Vdc
Input Voltage Low	Pin 9	V_{IL}	—	0.8	Vdc
Differential Input Voltage (1) Pins 3–6, 11–14 (1)		V_{DIFF}	350	—	mV
Voltage Common Mode Pins 3–6, 11–14		V_{CM}	2.8	V_{CC}	Vdc
Output Voltage High I_{OH} = 3.0 mA		V_{OH}	2.7	—	Vdc
Output Voltage Low I_{OL} = 20 mA		V_{OL}	—	0.5	Vdc
Short Circuit Current V_{OUT} = 0 V		I_{OS}	–60	–150	mA
Output Disable Current High V_{OUT} = 2.7 V		I_{OZH}	—	50	µA
Output Disable Current Low V_{OUT} = 0.5 V		I_{OZL}	—	–50	µA

(1) Common mode input voltage to pins 3–4, 5–6, 11–12, 13–14 must be between the values of 2.8 V and 5.0 V. This common mode input voltage range includes the differential input swing.
(2) For single ended use, apply 3.75 V (V_{BB}) to either input depending on output polarity required. Signal level range to other input is 3.3 V to 4.2 V.
(3) Any unused gates should have the inverting inputs tied to V_{CC} and the non–inverting inputs tied to ground to prevent output glitching.
(4) 1.0 V to 2.0 V w/50 pF into 500 ohms.

*Positive Emitter Coupled Logic

DIP PIN ASSIGNMENT



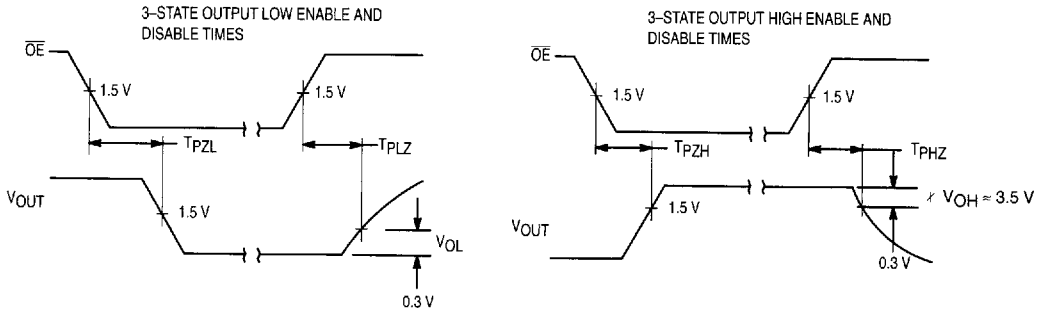
Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

MOTOROLA

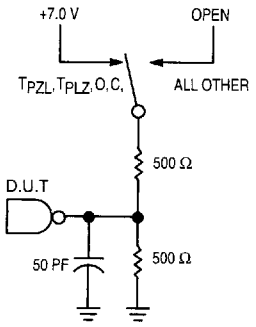
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (See Notes 1 & 4)

Characteristic	Symbol	T_A = 0°C to 75°C Min	Max	Unit
AC PARAMETERS (C_L = 50 pF) (V_{CC} = 5.0 ± 5%) (T_A = 0°C to 75°C)				
Propagation Delay Data	t_{pd}	1.5	5.0	ns
Rise Time	t_r	0.3	1.6	ns
Fall Time	t_f	0.3	1.6	ns
Output Disable Time	t_{pdLZ} t_{pdHZ}	2.0 2.0	6.0 6.0	ns
Output Enable Time	t_{pdZL} t_{pdZH}	2.0 2.0	8.0 8.0	ns

3–STATE SWITCHING WAVEFORMS



TEST LOAD



*INCLUDES JIG AND PROBE CAPACITANCE

Application Note: Pin 9 is an $\overline{OE}$ and the 10H350 is disabled when $\overline{OE}$ is at V_{IH} or higher.