TMC2330
CMOS Coordinate Transformer
16 x 16 Bit, 25 MOPS

Description

The TMC2330 VLSI circuit converts bidirectionally between Cartesian (real and imaginary) and Polar (magnitude and phase) coordinates at up to 25 MOPS (Million Operations Per Second).

In its Rectangular-to-Polar mode, the TMC2330 can extract phase and magnitude information or backward "map" from a rectangular raster display to a radial (e.g., range-and-azimuth) data set.

The Polar-to-Rectangular mode executes direct digital waveform synthesis and modulation. With its 32-bit phase accumulator, the chip can generate and frequency or phase-modulate quadrature sinusoidal waveforms with a frequency resolution of 0.006 Hz at a 25 MHz clock rate. The TMC2330 greatly simplifies real-time image-space conversion between the radially-generated image scan data found in radar, sonar, and medical imaging systems, and raster-oriented display formats.

All input and output data ports are registered, and a new transformed data word pair is available at the output every 40 ns. The user-configurable phase accumulator structure, input clock enables, and asynchronous three-state output bus enables simplify interfacing. All signals are TTL compatible.

Fabricated in Raytheon Semiconductor's OMICRON-C™ one-micron CMOS process, the TMC2330 operates at up to the 25 MHz maximum clock rate over the full commercial (0 to 70°C) temperature and supply voltage ranges, and is available in a low-cost 120-pin plastic pin grid array package. The MIL-STD-883C version, the TMC2330L5V, is housed in a ceramic chip carrier and is specified over the full extended (-55 to 125°C) case temperature range.

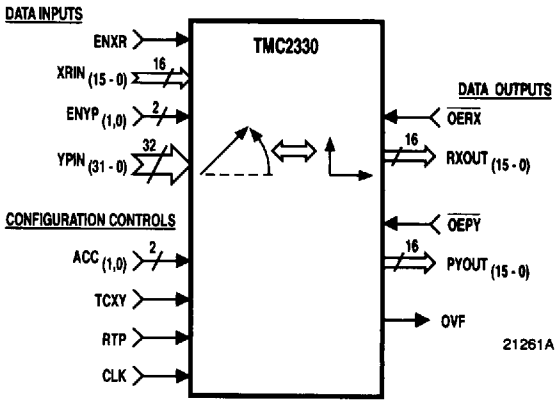
Features

- Rectangular-to-Polar or Polar-to-Rectangular conversion at guaranteed 25 MOPS pipelined throughput rate
- Polar data: 16-bit magnitude, 32-bit input/16-bit output phase
- 16-bit user-selectable two's complement or sign-and-magnitude rectangular data formats
- Input register clock enables and asynchronous output enables simplify interfacing
- User-configurable phase accumulator for waveform synthesis and amplitude, frequency, or phase modulation
- Magnitude output data overflow flag (in Polar-to-Rectangular mode)
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package
- Available in a 132-leaded CERQUAD

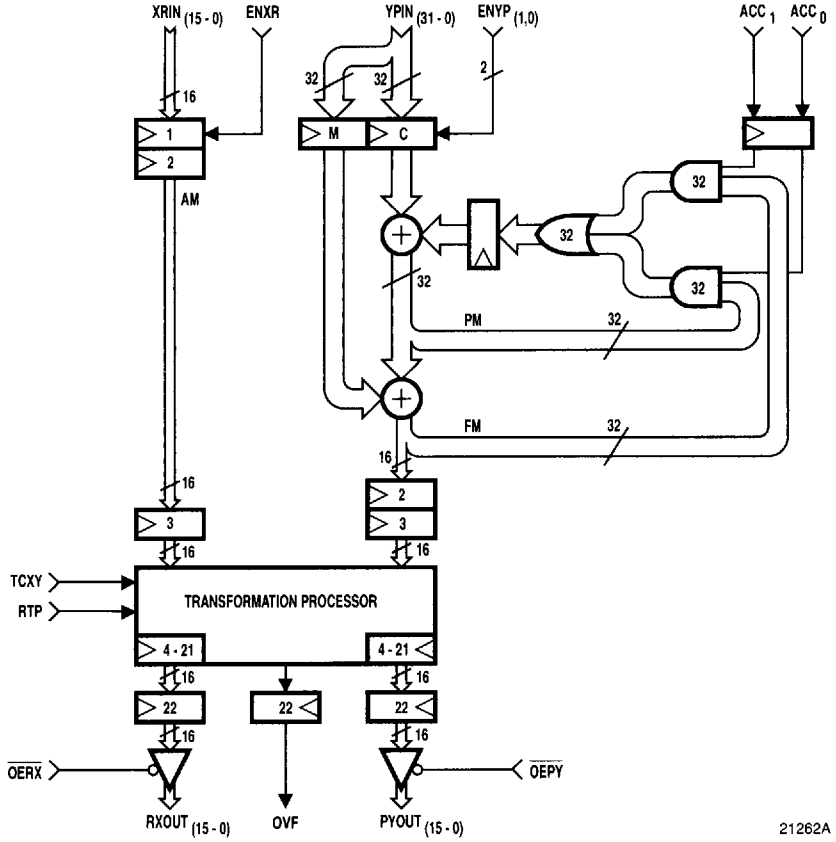
Applications

- Scan conversion (phased array to raster)
- Vector magnitude estimation
- Range and bearing derivation
- Spectral analysis
- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

TMC2330 Logic Symbol



Functional Block Diagram



Functional Description

General Information

The TMC2330 converts between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinate data word pairs. The user selects the numeric format and transformation to be performed (Rectangular-To-Polar or Polar-To-Rectangular), and the operation is performed on the data presented to the inputs on the next clock. The transformed result is then available at the outputs 22 clock cycles later, with new output data available every 40ns. All input and output data ports are registered, with input clock enables and asynchronous high-impedance output enables to simplify connections to system buses.

When executing a Rectangular-To-Polar conversion, the input ports accept 16-bit Rectangular coordinate words, and the output ports generate 16-bit magnitude and 16-bit phase data. The user selects either two's complement or sign-and-magnitude Cartesian data format. Polar magnitude data are always in magnitude format only. Since the phase angle word is modulo 2π, it may be regarded as either unsigned or two's complement format (*Tables 1 and 2*).

In Polar-To-Rectangular mode, the input ports accept 16-bit Polar magnitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words. Again, the user selects between two's complement or sign-and-magnitude Cartesian data format. The dual 32-bit phase accumulator input registers are useful in signal synthesis applications, storing high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. This allows the TMC2330 to generate precision quadrature waveforms unattended, once the accumulator has been enabled. The flexible input phase accumulator structure supports

General Information (cont.)

frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator control word $ACC_{1,0}$. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2330 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2330 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

$XRIN_{15\text{-}0}$ — $XRIN_{15\text{-}0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15}$ is the MSB.

$YPIN_{31\text{-}0}$ — $YPIN_{31\text{-}0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENYP_{1,0}$. When RTP is HIGH (Rectangular-To-Polar), the input accumulators are normally not used. The 16 MSBs of YPIN are the input port, and the lower 16 bits become "don't cares" if ACC=00. $YPIN_{31}$ is the MSB.

$RXOUT_{15\text{-}0}$ — $RXOUT_{15\text{-}0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OERX}$=HIGH. $RXOUT_{15}$ is the MSB.

$PYOUT_{15\text{-}0}$ — $PYOUT_{15\text{-}0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEPY}$=HIGH. $PYOUT_{15}$ is the MSB.

Controls

ENXR — The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.

$ENYP_{1,0}$ — The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$, as shown below:

$ENYP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

RTP — This registered input selects the current transformation mode of the device. When RTP is HIGH, the TMC2330 executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input. See the *Timing Diagram*.

$ACC_{1,0}$ — In applications utilizing the TMC2330 to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below:

$ACC_{1,0}$	Configuration
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

Controls (cont.)

$ACC_{1,0}$ (cont.) Note that the accumulators will also function when RTP = HIGH (Rectangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates. However, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.

TCXY The format select control sets the numeric format of the Rectangular data, whether input (RTP = HIGH) or output (RTP = LOW). This control indicates two's complement format when TCXY = HIGH, and sign-and-magnitude when LOW. This is a static input. See the *Timing Diagram*.

OVF When RTP = LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put value(s) return to full-scale or less. See the *Applications Discussion* section. Overflow is not possible in Rectangular-To-Polar mode (RTP = HIGH).

$\overline{OERX}$, $\overline{OEPY}$ Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OERX}$ or $\overline{OEPY}$ is HIGH, the respective output port(s) is in the high-impedance state.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, F2, G3, K3, L3, L7, K11, J11, G11, E12, D11, C10, C9, C7, C5, C4	5, 11, 14, 17, 29, 33, 49, 75, 83, 89, 95, 104, 108, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	$XRIN_{15-0}$	X or Radius Data	F12, F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	86, 85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	$YPIN_{31-0}$	Y or Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	$RXOUT_{15-0}$	Radius or X Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	$PYOUT_{15-0}$	Phase or Y Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENXR	X or Radius In Enable	M11	63
	$ENYP_{1,0}$	Y or Phase In Enable	G1, G2	18, 16
	RTP	Conversion Select	E1	12
	$ACC_{1,0}$	Accumulate Control	H2, H1	20, 19
	TCXY	Cartesian Data Format	F1	15
	$\overline{OERX}$	Radius or X Out Enable	E13	88
	$\overline{OEPY}$	Phase or Y Out Enable	D1	10
Flags	OVF	Overflow Flag	B7	115
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Inputs

The controls RTP and TCXY determine the transformation mode and the assumed numeric format of the Rectangular data. The user must exercise caution when changing either of these controls, as the new transformed results will not be seen the at the outputs until the entire internal pipe (22 clocks) has been flushed. Thus, these controls are considered static.

Table 1. Data Input/Output Formats – Integer Format

Port	RTP	TCXY	31	30	29	. . .	16	Bit # 15	14	. . .	0	Format	
XRIN	0	X						2^{15}	2^{14}	. . .	2^{0}.		U
XRIN	1	0						NS	2^{14}	. . .	2^{0}.		S
XRIN	1	1						-2^{15}	2^{14}	. . .	2^{0}.		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	(xπ)T/U	
YPIN	1	0	NS	2^{14}	2^{13}	. . .	2^{0}.						S
YPIN	1	1	-2^{15}	2^{14}	2^{13}	. . .	2^{0}.						T
RXOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
RXOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
RXOUT	1	X						2^{15}	2^{14}	. . .	2^{0}.		U
PYOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
PYOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	(xπ)T/U	

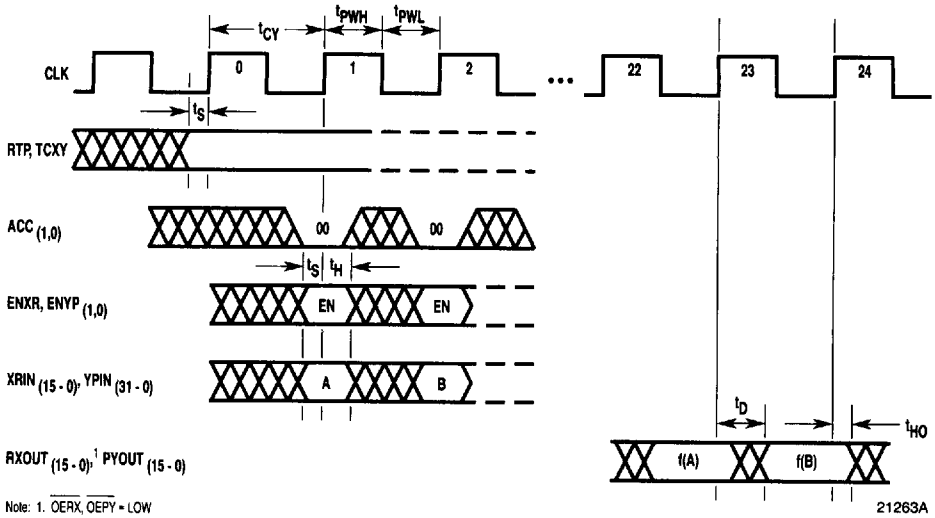
Table 2. Data Input/Output Formats – Fractional Format

Port	RTP	TCXY	31	30	29	. . .	16	Bit # 15	14	. . .	0	Format	
XRIN	0	X						2^{0}.	2^{-1}	. . .	2^{-15}		U
XRIN	1	0						NS.	2^{-1}	. . .	2^{-15}		S
XRIN	1	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	(xπ)T/U	
YPIN	1	0	NS.	2^{-1}	2^{-2}	. . .	2^{-15}						S
YPIN	1	1	-2^{0}	2^{-1}	2^{-2}	. . .	2^{-15}						T
RXOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
RXOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
RXOUT	1	X						2^{0}.	2^{-1}	. . .	2^{-15}		U
PYOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
PYOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	(xπ)T/U	

Notes:
1. -2^{15} denotes two's complement sign bit.
2. NS denotes negative sign, i.e., '1' negates the number.
3. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit – since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $+\pi$ or $-\pi$.
4. All phase angles are in terms of π radians, hence notation "xπ."
5. If A_{CC}=00, YPIN (15-0) are "don't cares."
6. Formats:
   T=Two's Complement
   S=Signed Magnitude
   U=Unsigned

HEX	U	T	S
FFFF	65535	–1	–32767
– –	– –	– –	– –
8001	32769	–32767	–1
8000	32768	–32768	0
7FFF	32767	32767	32767
– –	– –	– –	– –
0001	1	1	1
0000	0	0	0

Figure 1. Timing Diagram – No Accumulation



Note: 1. $\overline{OERX}$, $\overline{OEPY}$ = LOW

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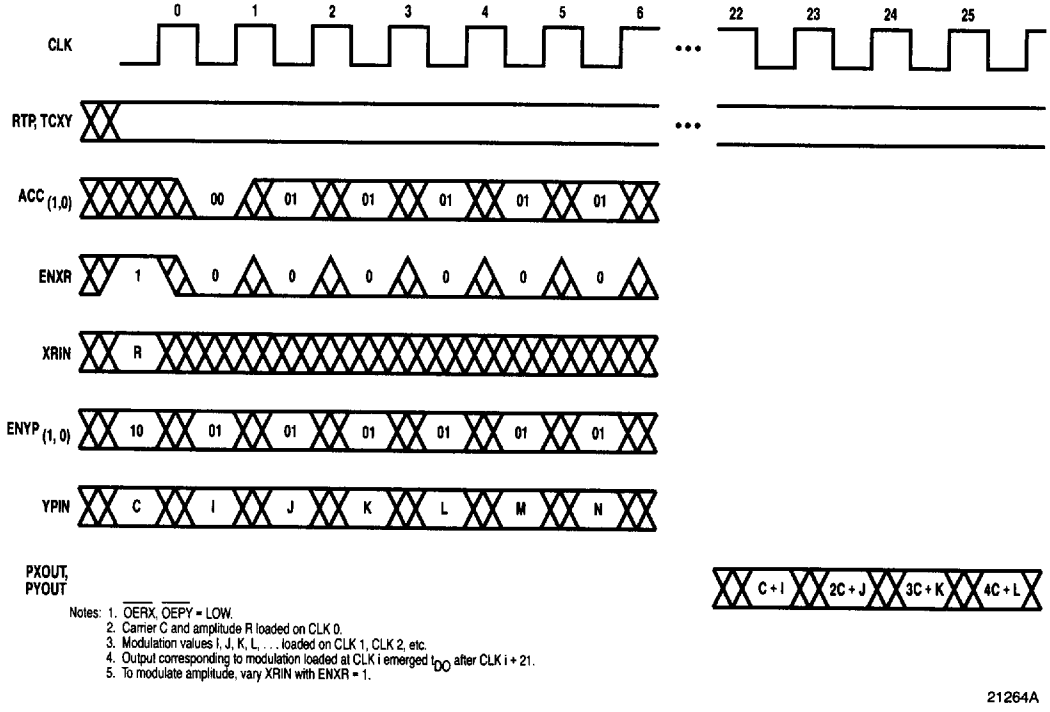
Figure 2. Timing Diagram – Phase Modulation



Notes: 1. $\overline{OERX}$, $\overline{OEPY}$ = LOW.
2. Carrier C and amplitude R loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary XRIN with ENXR = 1.

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Figure 3. Equivalent Input Circuit

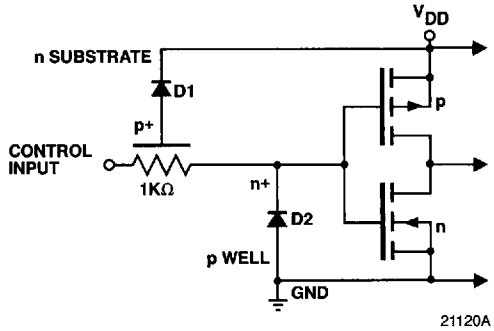


Figure 4. Equivalent Output Circuit

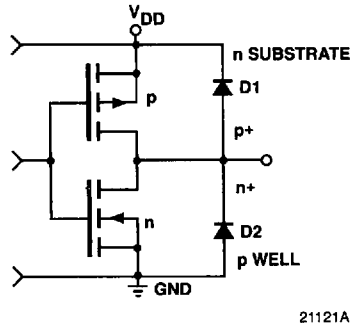
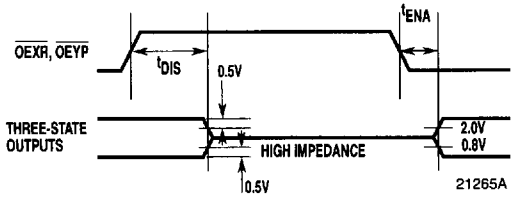


Figure 5. Transition Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output Voltage	
Applied voltage	−0.5 to (V_{DD} + 0.5)V [2]
Forced current	−6.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0		−4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min	50		55		ns
		TMC2330-1	40		45		ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	10		11		ns
		TMC2330-1	8		8		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	8		8		ns
		TMC2330-1	6		6		ns
t_S	Input Setup Time		12		13		ns
		TMC2330-1	10		11		ns
t_H	Input Hold Time		1		2		ns
		TMC2330-1	1		2		ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				−55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz $\overline{OERX}$ and $\overline{OEPY}$=V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		−10		−10	µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		10		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		−40		−40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		40		40	µA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	µA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=40pF		22		25	ns
		TMC2330-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=40pF		4		4	ns
		TMC2330-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD}=Min, C_{LOAD}=40pF		13		17	ns
		TMC2330-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD}=Min, C_{LOAD}=40pF		14		14	ns
		TMC2330-1		13		13	ns

Transforms

Applications Discussion

Numeric Overflow

Because the TMC2330 accommodates 16-bit unsigned radii and 16-bit signed Cartesian coordinates, Polar-To-Rectangular conversions can overflow for incoming radii greater than 32767=7FFFh and will overflow for all incoming radii greater than 46341=B505h. (In signed magnitude mode, a radius of 46340 = B504h will also overflow at all angles.) The regions of overflow and of correct conversion are illustrated in *Figure 6*.

In signed magnitude mode, overflows are circularly symmetrical – if a given radius overflows at an angle P, it will also overflow at the angles $\pi-P$, $\pi+P$, and $-P$. This is because $-X$ will overflow if and only if X overflows, and $-Y$ will overflow if and only if Y overflows.

In two's complement mode, the number system's asymmetry complicates the overflow conditions slightly. An input vector with an X component of −32768=8000h will not overflow, whereas one with an X component of +32768 will. *Table 3* summarizes several simple cases of overflow and near-overflow.

Numeric Underflow

In RTP=1 (Rectangular-To-Polar mode), if XRIN=YPIN=0, the angle is undefined. Under these conditions, the TMC2330 will output the expected radius of 0 (RXOUT=0000) and an angle of 1.744 radians (PYOUT=4707). This angle is an artifact of the CORDIC algorithm and is not flagged as an error, since the angle of any 0 length vector is arbitrary.

Table 3a. X-Dimensional Marginal Overflows

TC YPIN	OV RXOUT	CORRECT X
0 0000=0	1 0000=+0	+32768
0 8000=π	1 8000=−0	−32768
1 0000=0	1 8000=−32768	+32768
1 8000=π	0 8000=−32768	−32768

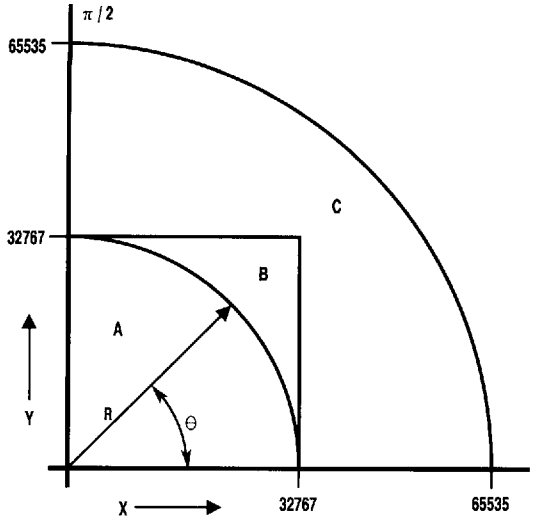
In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=8000 (incoming radius=32768).

Table 3b. Maximal Overflow (Radius In=65535)

TC YPIN	OV RXOUT	CORRECT X
0 0000=0	1 7FFF=+32767	+65535
0 8000=π	1 FFFF=−32767	−65535
1 0000=0	1 FFFF=−1	+65535
1 8000=π	1 0001=+1	−65535

In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=7FFF (incoming radius=65535, which will always overflow).

Figure 6. First Quadrant Coordinate Relationships



$X = R(\cos\Theta)$
$Y = R(\sin\Theta)$

and

$R = \sqrt{X^2 + Y^2}$
$\Theta = \tan^{-1}(Y/X)$

If R < 32768, overflow will not occur (region A).
If R > 32767, overflow will occur (region C) if |X| > 32767 or |Y| > 32767.
If R > 32767, overflow will not occur (region B) if |X| < 32768 and |Y| < 32768.

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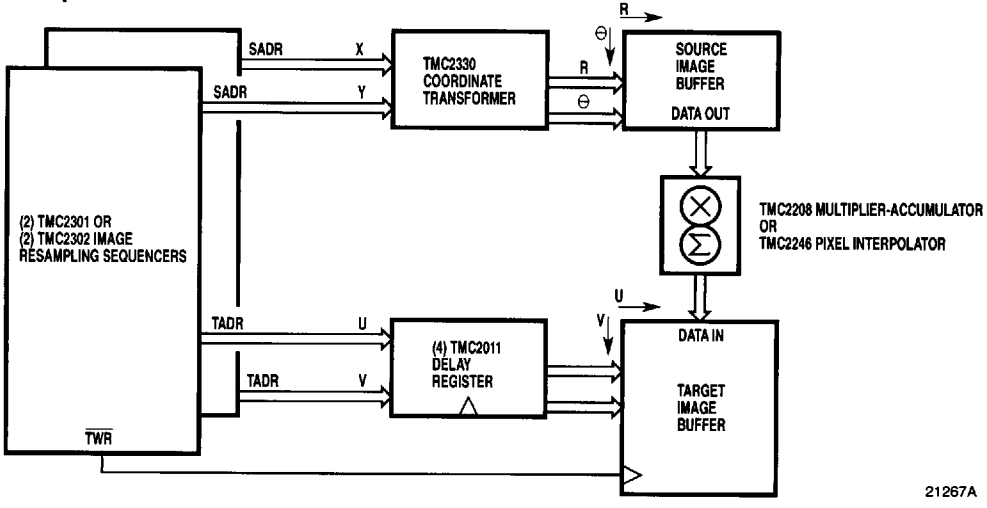
Performing Scan Conversion with the TMC2330

Medical Imaging Systems such as Ultrasound, MRI, and PET, and phased array Radar and Sonar systems generate radial-format coordinates (range or distance, and bearing) which must be converted into raster-scan format for further processing and display. Utilizing the TRW TMC2301 Image Resampling Sequencer, a minimum chipcount Scan Converter can be implemented which utilizes the trigonometric translation performed by the TMC2330 to backwards-map from a Cartesian coordinate set into the Polar source image buffer address space.

Figure 7. Block Diagram of Scan Converter Circuit Utilizing TMC2330 and TMC2301 Image Resampling Sequencer



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As shown in *Figure 7*, the TMC2330 transforms the Cartesian source image addresses from the TMC2301 directly to vector distance and angle coordinates, while the TMC2301 writes the resulting resampled pixel values into the target memory in raster fashion. Note that the ability to perform this spatial transformation in either direction gives the user the freedom to process images in either coordinate space, with little restriction. Image manipulation such as zooms or tilts can easily be included in the transformation by programming the desired image manipulation into the TMC2301's transformation parameter registers.

Statistical Evaluation of Double Conversion

In this empirical test, 10,000 random Cartesian vectors were converted to and from polar format by the TMC2330. The resulting Cartesian pairs were then compared against the original ones. The unrestricted data base represents uniform sampling over a square bounded by $-32769 < x < 32768$ and $-32769 < y < 32768$.

The results of the 10,000-vector study were as follows:

Mean Error (X)	= +0.0052 LSB
Mean Error (Y)	= +0.0031 LSB
Mean Absolute Error (X)	= 0.662 LSB
Mean Absolute Error (Y)	= 0.664 LSB
Root Mean Square Error (X)	= 1.025 LSB
Root Mean Square Error (Y)	= 1.020 LSB
Max Error (X)	= +4/−5 LSB
Max Error (Y)	= +5/−4 LSB

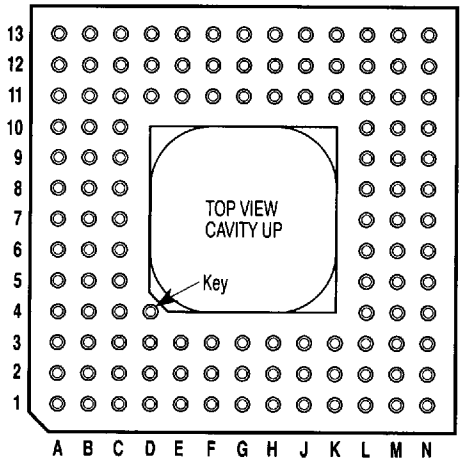
Since this is a double conversion (rectangular to polar and back) which includes a wide variety of "good case" and "bad case" vectors, the chip should perform even better in many actual systems. Repeating the experiment and restricting the original data set to an annulus defined by $8196 < R < 32768$ reduced the mean square error to 0.89 LSB and the peak error to ±4 LSB (x or y). These latter results are more germane to synthesizer, demodulator, and other applications in which the amplitude can be restricted to lie between quarter and full scale.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2330H5C1	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2330H5C1
TMC2330H5C	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2330H5C
TMC2330L5V1	EXT:T_C = -55°C to 125°C	MIL-STD-883	132-Leaded CERQUAD	2330L5V1
TMC2330L5V	EXT:T_C = -55°C to 125°C	MIL-STD-883	132-Leaded CERQUAD	2330L5V
TMC2330G1V1	EXT:T_C = -55°C to 125°C	MIL-STD-883	120-Pin Ceramic PGA	2330G1V1
TMC2330G1V	EXT:T_C = -55°C to 125°C	MIL-STD-883	120-Pin Ceramic PGA	2330G1V

Pin Assignments — 121-Pin Plastic Pin Grid Array, H5 Package; 120-Pin Ceramic PGA, G1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	$PYOUT_5$	B3	$PYOUT_6$	C5	GND	E1	RTP	G11	GND	K1	$YPIN_2$	L10	$YPIN_{31}$	M12	$XRIN_1$
A2	$PYOUT_7$	B4	$PYOUT_9$	C6	V_{DD}	E2	GND	G12	$XRIN_{12}$	K2	$YPIN_4$	L11	V_{DD}	M13	$XRIN_2$
A3	$PYOUT_8$	B5	$PYOUT_{11}$	C7	GND	E3	V_{DD}	G13	$XRIN_{13}$	K3	GND	L12	$XRIN_3$	N1	$YPIN_8$
A4	$PYOUT_{10}$	B6	$PYOUT_{13}$	C8	V_{DD}	E11	V_{DD}	H1	ACC_0	K11	GND	L13	$XRIN_4$	N2	$YPIN_{10}$
A5	$PYOUT_{12}$	B7	OVF	C9	GND	E12	GND	H2	ACC_1	K12	$XRIN_5$	M1	$YPIN_6$	N3	$YPIN_{12}$
A6	$PYOUT_{14}$	B8	$RXOUT_1$	C10	GND	E13	$\overline{OERX}$	H3	V_{DD}	K13	$XRIN_6$	M2	$YPIN_9$	N4	$YPIN_{15}$
A7	$PYOUT_{15}$	B9	$RXOUT_3$	C11	V_{DD}	F1	TCXY	H11	$XRIN_9$	L1	$YPIN_5$	M3	$YPIN_{11}$	N5	$YPIN_{17}$
A8	$RXOUT_0$	B10	$RXOUT_5$	C12	$RXOUT_{11}$	F2	GND	H12	$XRIN_{10}$	L2	$YPIN_7$	M4	$YPIN_{13}$	N6	$YPIN_{19}$
A9	$RXOUT_2$	B11	$RXOUT_7$	C13	$RXOUT_{13}$	F3	CLK	H13	$XRIN_{11}$	L3	GND	M5	$YPIN_{16}$	N7	$YPIN_{21}$
A10	$RXOUT_4$	B12	$RXOUT_9$	D1	$\overline{OEPY}$	F11	V_{DD}	J1	$YPIN_0$	L4	V_{DD}	M6	$YPIN_{18}$	N8	$YPIN_{22}$
A11	$RXOUT_6$	B13	$RXOUT_{12}$	D2	$PYOUT_0$	F12	$XRIN_{15}$	J2	$YPIN_1$	L5	$YPIN_{14}$	M7	$YPIN_{20}$	N9	$YPIN_{24}$
A12	$RXOUT_8$	C1	$PYOUT_1$	D3	GND	F13	$XRIN_{14}$	J3	$YPIN_3$	L6	V_{DD}	M8	$YPIN_{23}$	N10	$YPIN_{26}$
A13	$RXOUT_{10}$	C2	$PYOUT_2$	D11	GND	G1	$ENYP_1$	J11	GND	L7	GND	M9	$YPIN_{25}$	N11	$YPIN_{29}$
B1	$PYOUT_3$	C3	V_{DD}	D12	$RXOUT_{14}$	G2	$ENYP_0$	J12	$XRIN_7$	L8	V_{DD}	M10	$YPIN_{28}$	N12	$YPIN_{30}$
B2	$PYOUT_4$	C4	GND	D13	$RXOUT_{15}$	G3	GND	J13	$XRIN_8$	L9	$YPIN_{27}$	M11	ENXR	N13	$XRIN_0$



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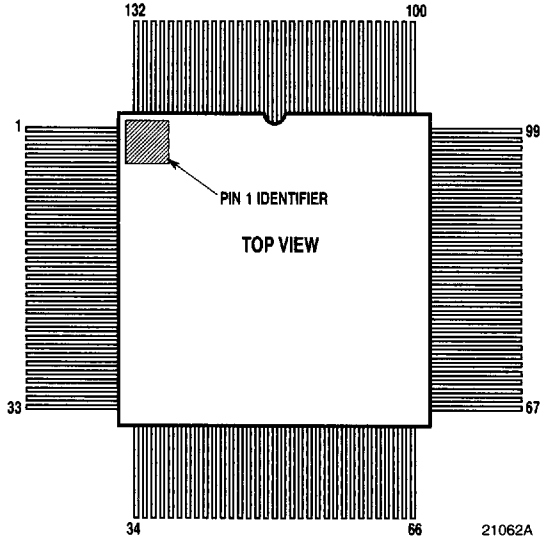
Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	$YPIN_1$	45	V_{DD}	67	V_{DD}	89	GND	111	$RXOUT_2$
2	NC	24	$YPIN_2$	46	$YPIN_{18}$	68	RXIN1	90	$RXOUT_{15}$	112	VDD
3	$PYOUT_4$	25	$YPIN_3$	47	$YPIN_{19}$	69	RXIN2	91	V_{DD}	113	$RXOUT_1$
4	$PYOUT_3$	26	$YPIN_4$	48	$YPIN_{20}$	70	GND	92	$RXOUT_{14}$	114	$RXOUT_0$
5	GND	27	$YPIN_5$	49	GND	71	$RXIN_3$	93	$RXOUT_{13}$	115	OVF
6	$PYOUT_2$	28	$YPIN_6$	50	$YPIN_{21}$	72	NC	94	$RXOUT_{12}$	116	GND
7	$PYOUT_1$	29	GND	51	$YPIN_{22}$	73	$RXIN_4$	95	GND	117	$PYOUT_{15}$
8	$PYOUT_0$	30	$YPIN_7$	52	$YPIN_{23}$	74	$RXIN_5$	96	$RXOUT_{11}$	118	$PYOUT_{14}$
9	V_{DD}	31	$YPIN_8$	53	V_{DD}	75	GND	97	$RXOUT_{10}$	119	$PYOUT_{13}$
10	$\overline{OEPY}$	32	NC	54	$YPIN_{24}$	76	$RXIN_6$	98	NC	120	V_{DD}
11	GND	33	GND	55	$YPIN_{25}$	77	$RXIN_7$	99	V_{DD}	121	$PYOUT_{12}$
12	RTP	34	$YPIN_9$	56	$YPIN_{26}$	78	$RXIN_8$	100	$RXOUT_9$	122	$PYOUT_{11}$
13	CLK	35	NC	57	$YPIN_{27}$	79	$RXIN_9$	101	NC	123	$PYOUT_{10}$
14	GND	36	$YPIN_{10}$	58	$YPIN_{28}$	80	$RXIN_{10}$	102	$RXOUT_8$	124	GND
15	TCXY	37	V_{DD}	59	$YPIN_{29}$	81	$RXIN_{11}$	103	NC	125	$PYOUT_9$
16	$ENYP_0$	38	$YPIN_{11}$	60	$YPIN_{30}$	82	$RXIN_{12}$	104	GND	126	$PYOUT_8$
17	GND	39	$YPIN_{12}$	61	$YPIN_{31}$	83	GND	105	$RXOUT_7$	127	$PYOUT_7$
18	$ENYP_1$	40	$YPIN_{13}$	62	NC	84	$RXIN_{13}$	106	$RXOUT_6$	128	NC
19	ACC_0	41	$YPIN_{14}$	63	ENXR	85	$RXIN_{14}$	107	$RXOUT_5$	129	GND
20	ACC_1	42	$YPIN_{15}$	64	NC	86	$RXIN_{15}$	108	GND	130	$PYOUT_6$
21	V_{DD}	43	$YPIN_{16}$	65	NC	87	V_{DD}	109	$RXOUT_4$	131	NC
22	$YPIN_0$	44	$YPIN_{17}$	66	$XRIN_0$	88	$\overline{OERX}$	110	$RXOUT_3$	132	$PYOUT_5$



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