PRELIMINARY
Notice This is not a final specification
Some parametric limits are subject to change

MH1M09SSP-25,-35,-45

9437184-BIT (1048576-WORD BY 9-BIT) CMOS STATIC RAM

DESCRIPTION

This is consists nine industry 1M × 1bit static RAMs in TSOP.

The mounting of TSOP on a dual in-line package provides any application where high densities and large quantities of memory are required.

FEATURES

- Fast access time MH1M09SSP-25 ····· 25ns(max)
  MH1M09SSP-35 ····· 35ns(max)
  MH1M09SSP-45 ····· 45ns(max)
- Low power dissipation Active ····· 3600mW(typ)
  Stand-by ····· 45mW(typ)
- Single + 5V(± 10%) supply operation
- 44-pins Dual-in-line package
- Power down by $\overline{S}$
- Fully static operation
- Requires neither ezternal clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory ezpansion by $\overline{S}$
- Solder corting lead

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW) [Single side]

A3	1	44	A2
A4	2	43	A1
A5	3	42	A0
A6	4	41	A19
A7	5	40	A18
A8	6	39	A17
A9	7	38	A16
A10	8	37	A15
A11	9	36	A13
A12	10	35	A14
Vcc	11	34	Vss
$\overline{W}$	12	33	$\overline{S}$
Vss	13	32	Vcc
Q1	14	31	D1
Q2	15	30	D2
Q3	16	29	D3
Q4	17	28	D4
Q5	18	27	D5
Q6	19	26	D6
Q7	20	25	D7
Q8	21	24	D8
QP	22	23	DP

Outline 44N1A

MITSUBISHI ELECTRIC

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FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low the Q terminal is maintained in the high impedance state, so it is possible to connect D and Q terminal directly.

In a read operation, after seting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at Q terminal.

When $\overline{S}$ is high, the chip is the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance) state, useful for OR-tie with other devices.

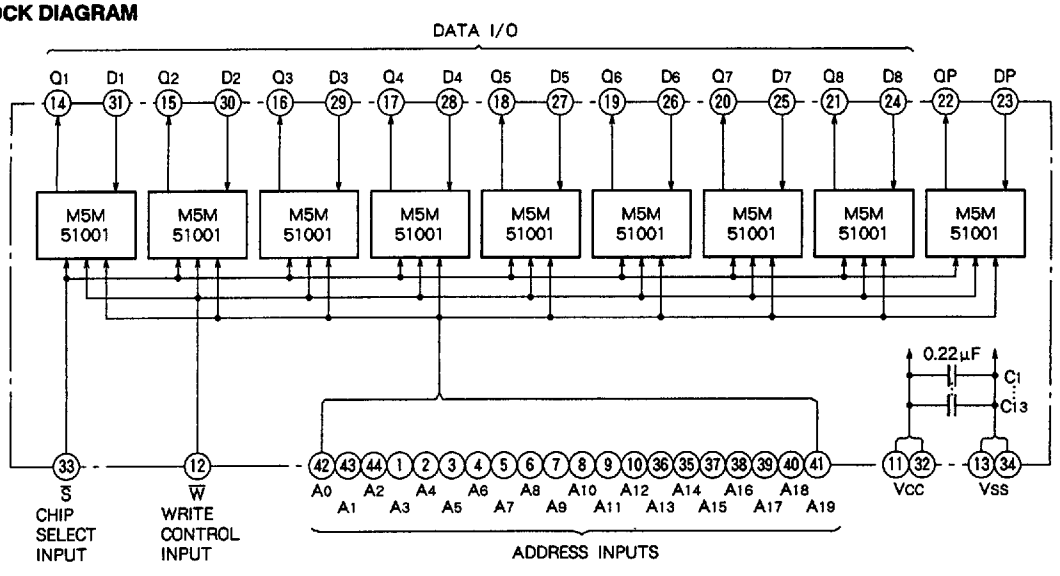
Signal $\overline{S}$ controls the power-down features. When $\overline{S}$ gose high, power dissipation is reduced extermely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	Mode	D	Q	Icc
H	X	Non-selection	High-impedance	High-impedance	Stand-by
L	L	Write	DIN	High-impedance	Active
L	H	Read	High-impedance	DOUT	Active

Note. H : VIH, L : VIL, X : Don't care

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Power dissipation		9	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage tempatue		−40~100	℃

* Pulse width ≤ 20ns, in case if DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				18	μA
| I_{OZ} |	Off-state output current	$V_{I(S)}$ = V_{IH}, V_O = 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(S)}$ = V_{IL} Output open	AC(Min cycle)			1260	mA
			DC		540	675	
I_{CC2}	Stand-by current	$V_{I(S)}$ = V_{IH}	AC(Min cycle)			360	mA
			DC			270	
I_{CC3}	Stand-by current	$V_{I(S)} \geq V_{CC}-0.2V$, other $V_I \leq 0.2V$ or $V_I \geq V_{CC}-0.2V$			9	90	mA

* −3.0V in case of AC (pulse width ≤ 20ns)

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz			55	pF
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz			15	pF

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AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V
Output timing reference levels ····· V_{OH} = 2.0V, V_{OL} = 0.8V
Output loads ····· Fig. 1, Fig. 2

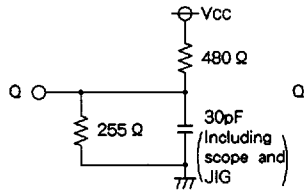

Fig. 1 Output load

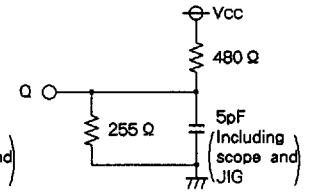

Fig. 2 Output load for t_{en}, t_{dis}

READ CYCLE

Symbol	Parameter	Limits						Unit
		MH1M09SSP-25		MH1M09SSP-35		MH1M09SSP-45		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	25		35		45		ns
$t_{a(A)}$	Address access time		25		35		45	ns
$t_{a(S)}$	Chip select access time		25		35		45	ns
$t_{v(A)}$	Data valid time after address	5		5		5		ns
$t_{en(S)}$	Chip selection to output active	5		5		5		ns
$t_{dis(S)}$	Output disable time from $\overline{S}$ high	0	15	0	20	0	20	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		25		35		45	ns

WRITE CYCLE

Symbol	Parameter	Limits						Unit
		MH1M09SSP-25		MH1M09SSP-35		MH1M09SSP-45		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	25		35		45		ns
$t_{su(S)}$	Chip select setup time	20		30		35		ns
$t_{su(A)1}$	Address setup time ($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time ($\overline{S}$)	0		0		0		ns
$t_{w(W)}$	Write pulse width	20		30		35		ns
$t_{rec(W)}$	Write recovery time	3		3		3		ns
$t_{su(D)}$	Data setup time	15		15		20		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$	0	10	0	15	0	15	ns
$t_{en(W)}$	Output enable time from $\overline{W}$	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	20		30		35		ns

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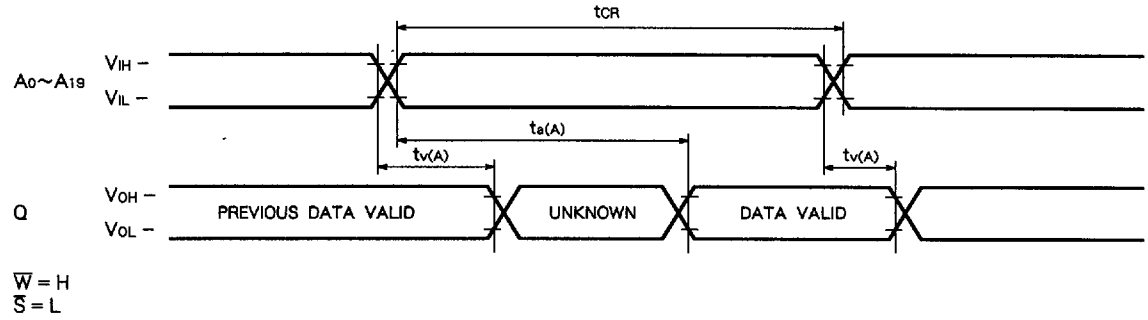
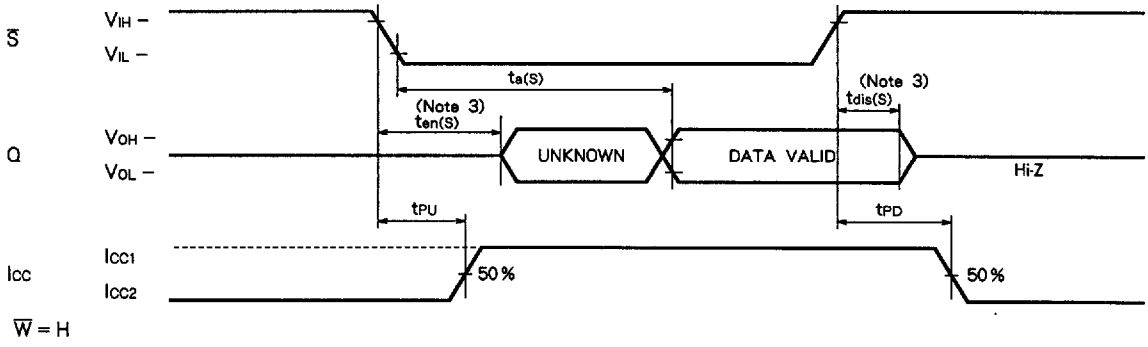
TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



Read cycle 2 (Note 2)



Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Fig. 2.

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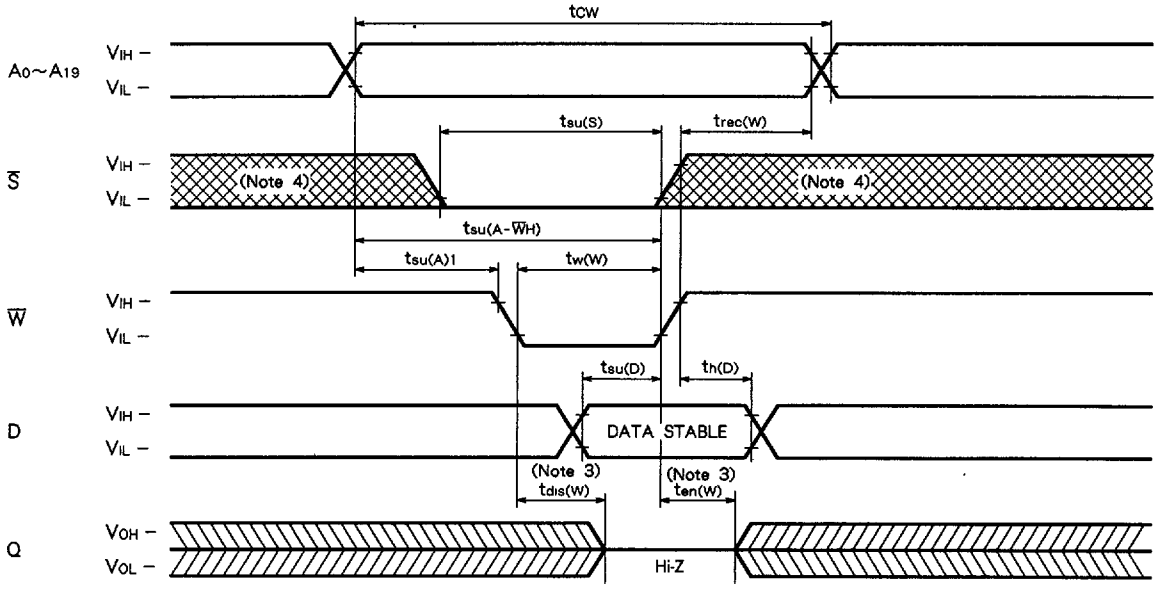
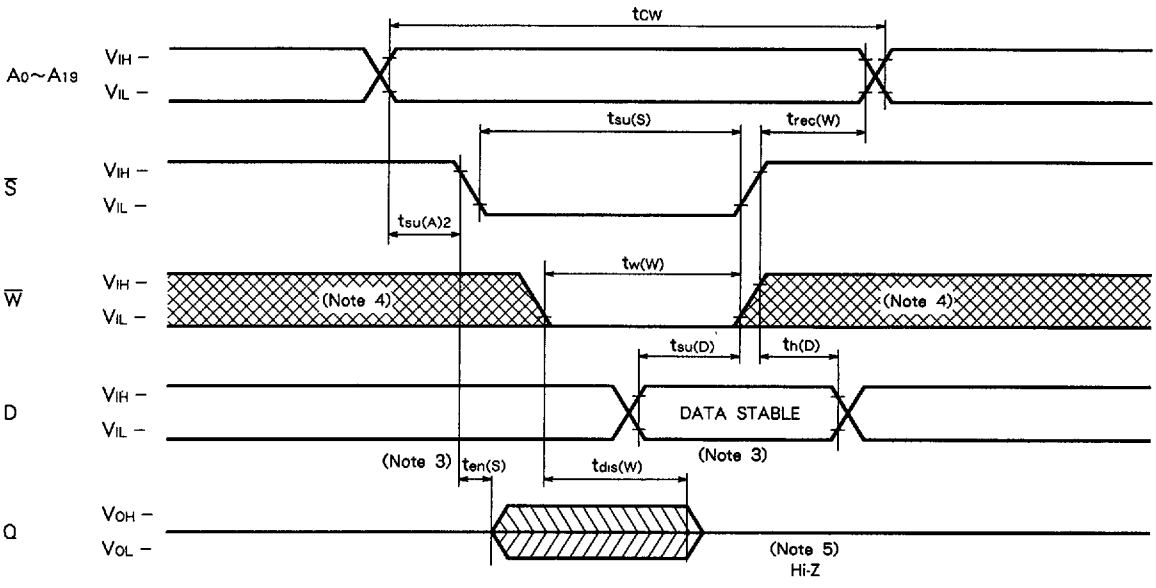
TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control)



Write cycle 2 ($\overline{S}$ control)



Note 4. Hatching indicates the states don't care.
5. When the falling edge of $\overline{W}$ is simultaneously or prior to the failing edge of $\overline{S}$, the outputs are maintained in the high impedance.