64-Channel Serial To Parallel Converter With Open Drain Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options				
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV03	220V	HV0322DG	HV0322PG	HV0322T	HV0322X	RBHV0322DG
	300V	HV0330DG	HV0330PG	HV0330T	HV0330X	—
HV05	220V	HV0522DG	HV0522PG	HV0522T	HV0522X	RBHV0522DG
	300V	HV0530DG	HV0530PG	HV0530T	HV0530X	—

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- HVCMOS® technology
- Output voltages up to 300V using a ramped supply
- Sink current minimum 100 mA
- Shift register speed 8 MHz
- Latched outputs
- Output polarity and blanking
- CMOS compatible inputs
- Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}[2]		-0.5V to +315V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		6.0A
Continuous total power dissipation[4]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. These devices have been designed to be used in applications which either switch the V_{PP} supply to ground before changing the state of the high voltage outputs or limit the current through each output.
3. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

The HV03 and HV05 are low voltage serial to high voltage parallel converters with open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic printheads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the high to low transition of the clock. The HV03 shifts in the counterclockwise direction when viewed from the top of the package and the HV05 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV03 and HV05 have been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or limit the current through each output.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current				100	µA	All outputs high, All SWS parallel
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_I = 0V
V_{OH}	High-Level Output Data Out		V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			15	V	IHV_{OUT} = +100mA
		Data Out			1	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				-1.5	V	I_{OL} = -100mA

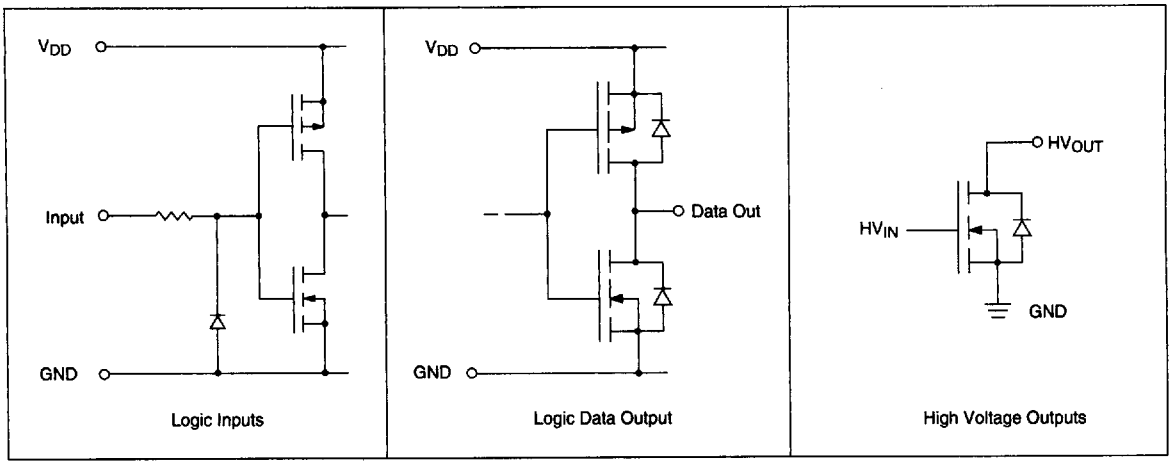
AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Falls	25			ns	
t_H	Data Hold Time After Clock Falls	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Falling Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Falling Edge of Clock	30			ns	
t_D	Delay Time from V_{PP} Low Until Change in $\overline{LE}$, $\overline{POL}$, $\overline{BL}$ Is Allowed	100			ns	
t_{SL}	Setup Time from Falling Edge $\overline{LE}$ to V_{PP} Rise	200			ns	
t_{SB}	Setup Time from $\overline{BL}$ Selected to V_{PP} Rise	150			ns	
t_{SP}	Setup Time from $\overline{POL}$ Selected to V_{PP} Rise	100			ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLK}	Delay Time Clock to Data Low to High			100	ns	

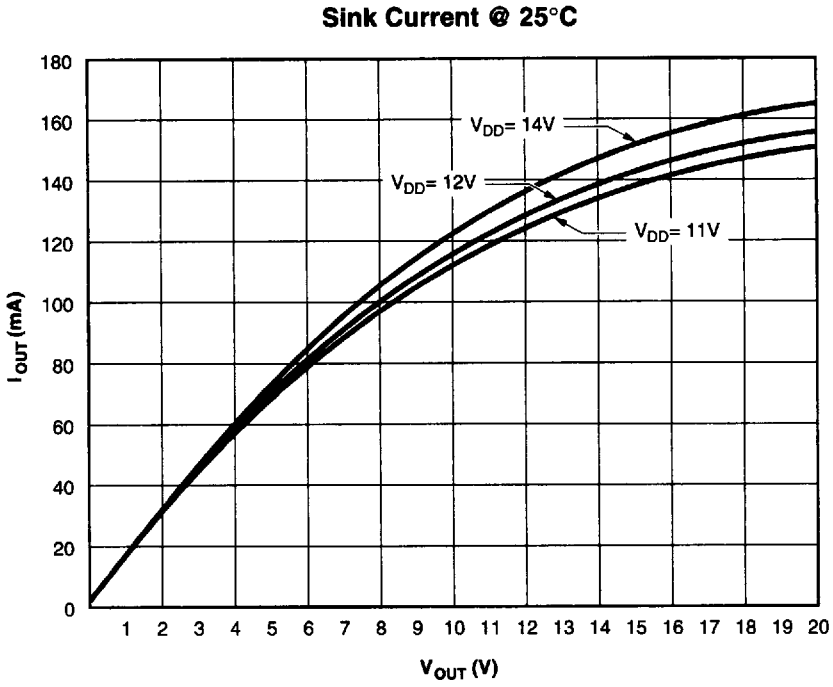
Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV0322/HV0522	-0.3		220	V
		HV0330/HV0530	-0.3		300	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
dV/dt	V_{PP} ramp rate				80	V/µs
T_A	Operating free-air temperature		-40		+85	°C

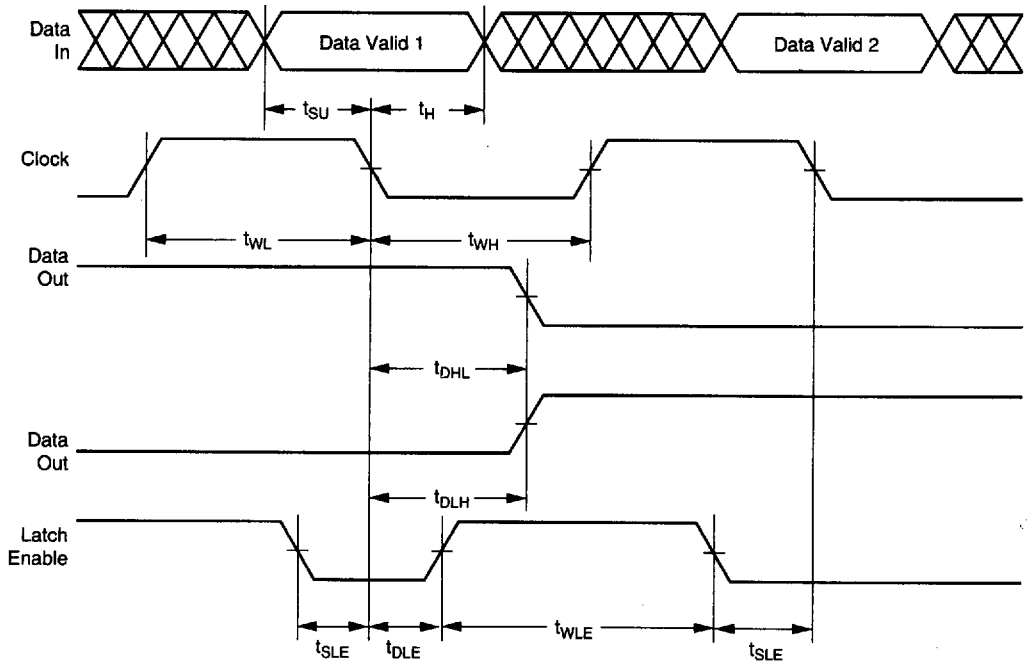
Input and Output Equivalent Circuit



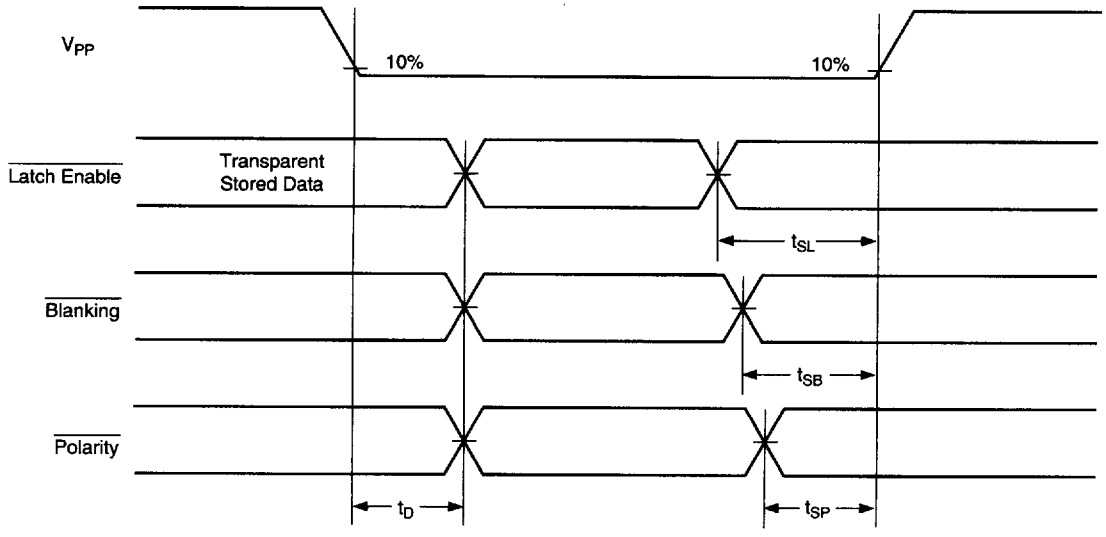
Typical Operating Conditions



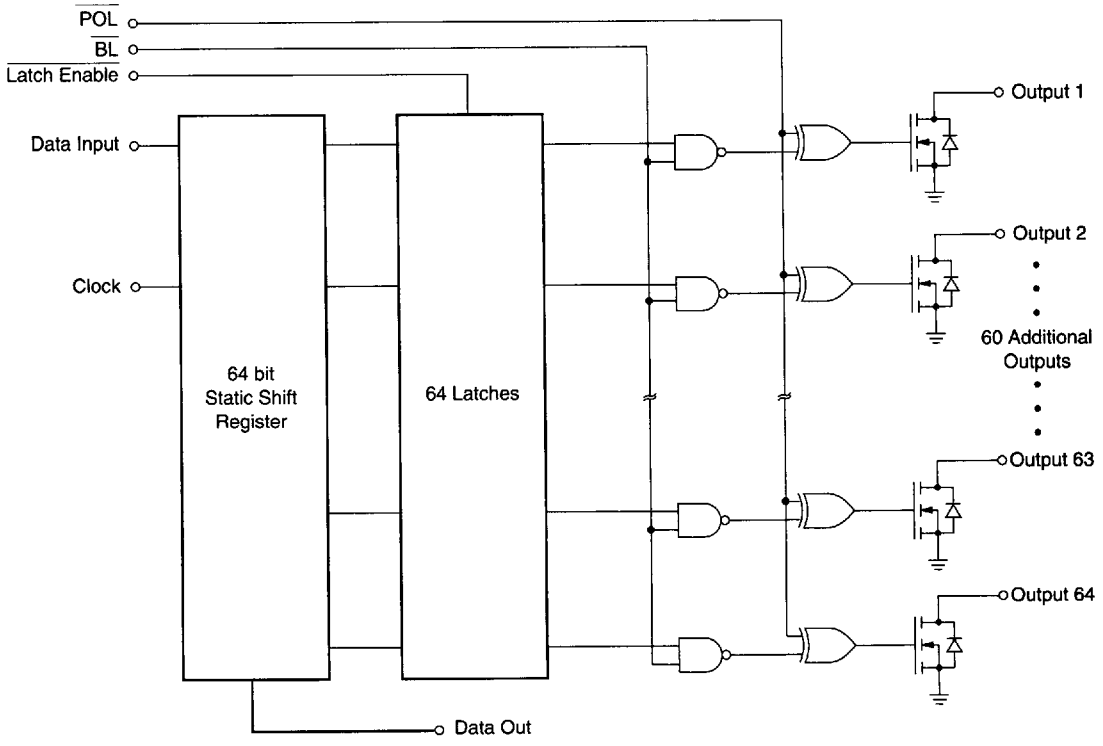
Switching Waveforms



Output Control Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...64	HV Outputs 1 2...64	Data Out *
All on	X	X	X	L	L	* *...*	L L...L	*
All off	X	X	X	L	H	* *...*	H H...H	*
Invert mode	X	X	L	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L *...*	* *...*	*
Load Latches	X	X	H	X	X	* *...*	* *...*	*
Transparent Latch mode	L	↓	H	H	H	L *...*	H *...*	*
	H	↓	H	H	H	H *...*	L *...*	*

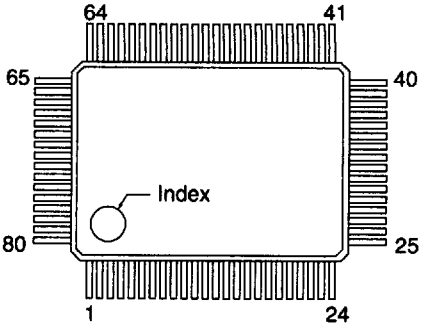
Notes:
H = high level, L = low level, X = irrelevant, ↓= high-to-low transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Pin Configurations

PG and DG Packages

HV03				HV05			
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	GND	41	GND	1	GND	41	GND
2	GND	42	GND	2	GND	42	GND
3	HV_{OUT} 59	43	HV_{OUT} 23	3	HV_{OUT} 6	43	HV_{OUT} 42
4	HV_{OUT} 60	44	HV_{OUT} 24	4	HV_{OUT} 5	44	HV_{OUT} 41
5	HV_{OUT} 61	45	HV_{OUT} 25	5	HV_{OUT} 4	45	HV_{OUT} 40
6	HV_{OUT} 62	46	HV_{OUT} 26	6	HV_{OUT} 3	46	HV_{OUT} 39
7	HV_{OUT} 63	47	HV_{OUT} 27	7	HV_{OUT} 2	47	HV_{OUT} 38
8	HV_{OUT} 64	48	HV_{OUT} 28	8	HV_{OUT} 1	48	HV_{OUT} 37
9	$\overline{POL}$	49	HV_{OUT} 29	9	$\overline{POL}$	49	HV_{OUT} 36
10	Data Out	50	HV_{OUT} 30	10	Data Out	50	HV_{OUT} 35
11	CLK	51	HV_{OUT} 31	11	CLK	51	HV_{OUT} 34
12	GND	52	HV_{OUT} 32	12	GND	52	HV_{OUT} 33
13	V_{DD}	53	HV_{OUT} 33	13	V_{DD}	53	HV_{OUT} 32
14	$\overline{LE}$	54	HV_{OUT} 34	14	$\overline{LE}$	54	HV_{OUT} 31
15	Data In	55	HV_{OUT} 35	15	Data In	55	HV_{OUT} 30
16	$\overline{BL}$	56	HV_{OUT} 36	16	$\overline{BL}$	56	HV_{OUT} 29
17	HV_{OUT} 1	57	HV_{OUT} 37	17	HV_{OUT} 64	57	HV_{OUT} 28
18	HV_{OUT} 2	58	HV_{OUT} 38	18	HV_{OUT} 63	58	HV_{OUT} 27
19	HV_{OUT} 3	59	HV_{OUT} 39	19	HV_{OUT} 62	59	HV_{OUT} 26
20	HV_{OUT} 4	60	HV_{OUT} 40	20	HV_{OUT} 61	60	HV_{OUT} 25
21	HV_{OUT} 5	61	HV_{OUT} 41	21	HV_{OUT} 60	61	HV_{OUT} 24
22	HV_{OUT} 6	62	HV_{OUT} 42	22	HV_{OUT} 59	62	HV_{OUT} 23
23	GND	63	GND	23	GND	63	GND
24	GND	64	GND	24	GND	64	GND
25	HV_{OUT} 7	65	HV_{OUT} 43	25	HV_{OUT} 58	65	HV_{OUT} 22
26	HV_{OUT} 8	66	HV_{OUT} 44	26	HV_{OUT} 57	66	HV_{OUT} 21
27	HV_{OUT} 9	67	HV_{OUT} 45	27	HV_{OUT} 56	67	HV_{OUT} 20
28	HV_{OUT} 10	68	HV_{OUT} 46	28	HV_{OUT} 55	68	HV_{OUT} 19
29	HV_{OUT} 11	69	HV_{OUT} 47	29	HV_{OUT} 54	69	HV_{OUT} 18
30	HV_{OUT} 12	70	HV_{OUT} 48	30	HV_{OUT} 53	70	HV_{OUT} 17
31	HV_{OUT} 13	71	HV_{OUT} 49	31	HV_{OUT} 52	71	HV_{OUT} 16
32	HV_{OUT} 14	72	HV_{OUT} 50	32	HV_{OUT} 51	72	HV_{OUT} 15
33	HV_{OUT} 15	73	HV_{OUT} 51	33	HV_{OUT} 50	73	HV_{OUT} 14
34	HV_{OUT} 16	74	HV_{OUT} 52	34	HV_{OUT} 49	74	HV_{OUT} 13
35	HV_{OUT} 17	75	HV_{OUT} 53	35	HV_{OUT} 48	75	HV_{OUT} 12
36	HV_{OUT} 18	76	HV_{OUT} 54	36	HV_{OUT} 47	76	HV_{OUT} 11
37	HV_{OUT} 19	77	HV_{OUT} 55	37	HV_{OUT} 46	77	HV_{OUT} 10
38	HV_{OUT} 20	78	HV_{OUT} 56	38	HV_{OUT} 45	78	HV_{OUT} 9
39	HV_{OUT} 21	79	HV_{OUT} 57	39	HV_{OUT} 44	79	HV_{OUT} 8
40	HV_{OUT} 22	80	HV_{OUT} 58	40	HV_{OUT} 43	80	HV_{OUT} 7

Package Outline



top view

80-pin Gullwing Package