

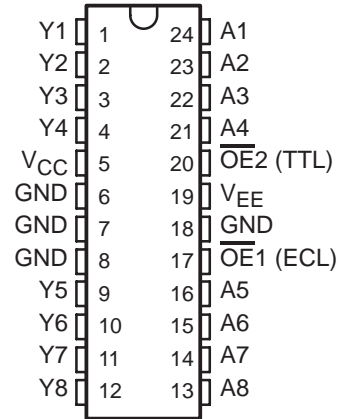
SN100KT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

SDZS008 – JANUARY 1990 – REVISED OCTOBER 1990

- 100K Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} , V_{EE} , and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include “Small Outline” Packages and Standard Plastic 300-mil DIPs

R NT PACKAGE

(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

Two pins $\overline{OE1}$ and $\overline{OE2}$ are provided for output-enable control. These control inputs are ANDed together with $\overline{OE1}$ being ECL-compatible and $\overline{OE2}$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5539 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
$\overline{OE1}$	$\overline{OE2}$	A	Y
H	X	X	H
X	H	X	H
L	L	L	L
L	L	H	H

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	TTL supply voltage	4.5	5	5.5	V
V _{EE}	ECL supply voltage	-4.2	-4.5	-4.8	V
V _{IH}	TTL high-level input voltage	2			V
V _{IL}	TTL low-level input voltage			0.8	V
V _{IH}	ECL high-level input voltage†	-1150		-840	mV
V _{IL}	ECL low-level input voltage†	-1810		-1490	mV
V _{OH}	TTL high-level output voltage			5.5	V
I _{OL}	TTL low-level output current			48	mA
I _{IK}	TTL input clamp current			-18	mA
T _A	Operating free-air temperature range	0		85	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V _{IK}	OE2 only	V _{CC} = 4.5 V,	V _{EE} = -4.2 V,	I _I = -18 mA			-1.2	V
I _{OH}		V _{CC} = 4.5 V,	V _{EE} = -4.2 V,	V _{OH} = 5.5 V			250	μA
V _{OL}		V _{CC} = 4.5 V,	V _{EE} = -4.5 V ± 0.3 V,	I _{OL} = 48 mA		0.38	0.55	V
I _I	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _I = 7 V			0.1	mA
I _{IH}	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _I = 2.7 V			20	μA
	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _I = -840 mV			350	μA
I _{IL}	OE2 only	V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _I = 0.5 V			-0.5	mA
	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _I = -1810 mV	0.5			μA
I _{CCH}		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			63	91	mA
I _{CCL}		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			79	114	mA
I _{EE}		V _{CC} = 5.5 V,	V _{EE} = -4.2 V			-22	-32	mA
C _i		V _{CC} = 5 V,	V _{EE} = -4.5 V			6		pF
C _o		V _{CC} = 5 V,	V _{EE} = -4.5 V			5		pF

‡ All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

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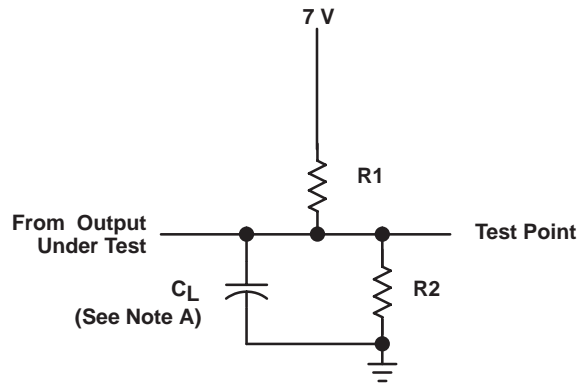
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

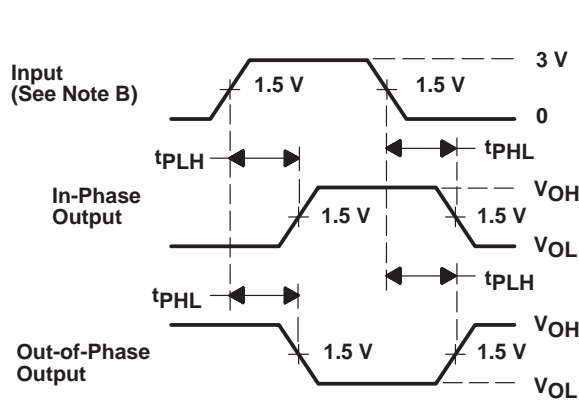
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
t _{PLH}	Any A	Y	6.2	9.3	12.4	ns
t _{PHL}			2.6	4.9	7.3	
t _{PLH}	$\overline{OE}1$ (ECL)	Y	7.1	10.3	13.5	ns
t _{PHL}			3.2	5.8	8.4	
t _{PLH}	$\overline{OE}2$ (TTL)	Y	6.5	9.5	12.4	ns
t _{PHL}			2.7	5.3	8	

All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

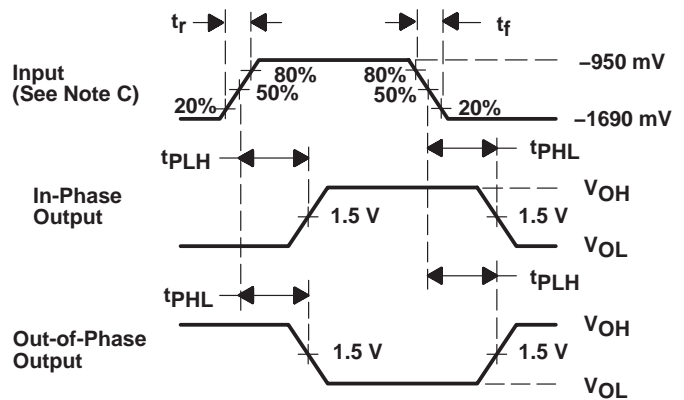
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



TTL-INPUT PROPAGATION DELAY TIMES



ECL-INPUT PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. For TTL inputs, input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. For ECL inputs, input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 0.7$ ns, $t_f \leq 0.7$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN100KT5539DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN100KT5539NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN100KT5539NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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