T-51-10-12

BURR-BROWN®

ADC80KD DIE

12-BIT ANALOG-TO-DIGITAL CONVERTER DIE

FEATURES

- INDUSTRY-STANDARD 12-BIT ADC IN DIE FORM
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V OR ±15V OPERATION
- NO MISSING CODES 0°C TO +70°C
- PARALLEL OR SERIAL OUTPUTS

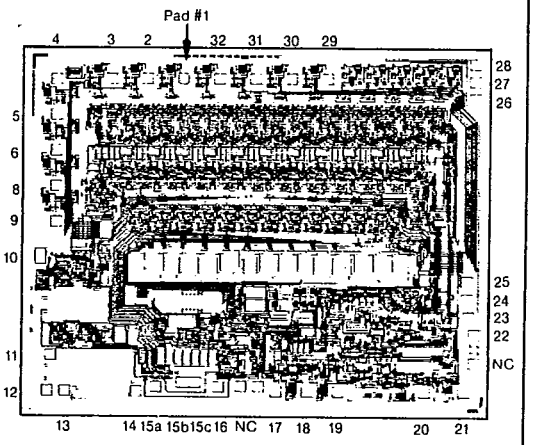
DESCRIPTION

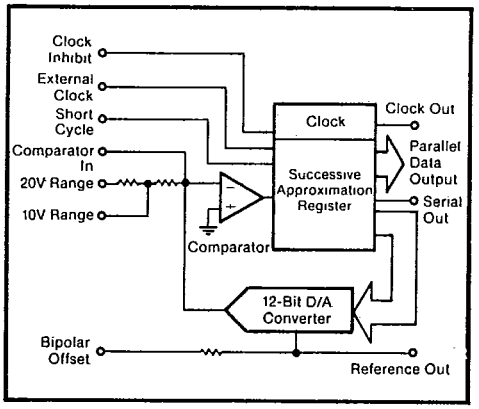
The ADC80KD is a complete 12-bit resolution, 12LSB linear analog-to-digital converter die. The die is manufactured on a high speed thin-film compatible bipolar process and all dice are laser-trimmed at the wafer level to guarantee key performance.

Internal scaling resistors are provided to give the user the options of input ranges of ±10V, ±5V, ±2.5V, 0 to 10V, or 0 to 5V full-scale range.

The ADC80KD is a successive approximation type ADC with a factory-set conversion time of 25μs. The ADC may be run from an external clock or short-cycled. All digital signals are TTL CMOS-compatible over the specified temperature range. The ADC requires power supplies of ±12V to ±15V and +5V.

The die size is 167 × 210 mils. Bond pads are 5 × 5 mils typical.





International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-732

T-51-10-12

SPECIFICATIONS

ELECTRICAL PROBE LIMITS[1]

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified.

MODEL	ADC80KD			
	MIN	TYP	MAX	UNITS
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		±2.5, ±5, ±10		V
Impedance: 0 to +5V, ±2.5V	2.45	2.5	2.55	kΩ
0 to +10V, ±5V	4.9	5	5.1	kΩ
±10V	9.8	10	10.2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0.8	V
I_{IH} (V_{IN} = +2.7V)			20	µA
I_{IL} (V_{IN} = +0.4V)	−20			µA
Convert Command Pulse Width[2]	0.1		20	µs
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[3]		±0.1	±0.3	% of 20V FSR[4]
Offset Error[3]: Unipolar		±0.05	±0.2	% of 20V FSR
Bipolar		±0.1	±0.3	% of 20V FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11.4V ≤ ± V_{CC} ≤ 16.5V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[5]		±10		ppm/°C
Gain		±15		ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7		ppm of FSR/°C
Linearity Error Drift		±1		ppm of FSR/°C
Differential Linearity over Temperature Range				LSB
No Missing Code Temperature Range	0		70	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[6]		22	25	µs
OUTPUT				
DIGITAL (Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[7]				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[8]		CSB, COB		
Logic Levels: Logic 0 (I_{SINK} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{SOURCE} ≤ 80µA)	+2.4			V
Internal Clock Frequency		520		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6.28	+6.3	+6.32	V
Source Current Available for External Loads[9]	200			µA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Rated Supply Voltages		+5, ±12 or ±15		V
Supply Ranges: ±V_{CC}	±11.4		±16.5	V
V_{DD}	+4.5		+5.5	V
Supply Drain: +I_{CC} (+V_{CC} = 15V)		8.5	11	mA
−I_{CC} (−V_{CC} = 15V)		21	24	mA
I_{DD} (V_{CC} = 5V)		30	36	mA
Power Dissipation (±V_{CC} = 15V, V_{DD} = 5V)		593	705	mW

NOTES: (1) All dice are probe tested and guaranteed to meet the above probe limits. These parameters may be adversely affected by packaging methods, and cannot be guaranteed in the application. (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 20µs (max) to assure the specified conversion time. (3) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drifts. (6) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (8) NRZ means Non-Return-to-Zero coding. (9) External loading must be constant during conversion, and must not exceed 200µA for guaranteed specification.

T-51-10-12

ASSEMBLY

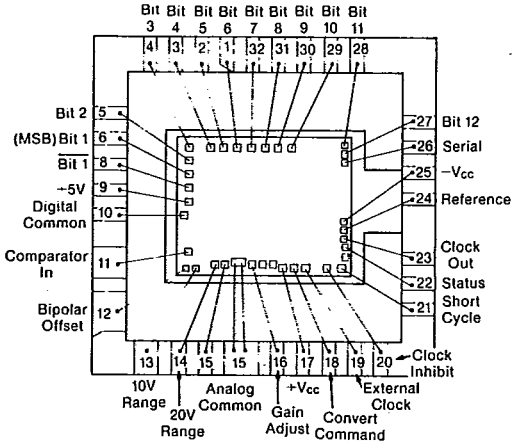
We suggest the use of a conductive polyimide or equivalent epoxy for die attach. The backside of the die must be connected to $-V_{CC}$ to ensure proper performance. Wire bond may be done with 1 to 1.5 mil gold or aluminum wire.

The resistors on the ADC80 are composed of a very stable, very low temperature coefficient, laser trimmed NiCr resistor material. Any excess moisture in the package will adversely affect the short and long term stability of the resistors. If moisture levels are allowed to become extreme, then the long term reliability of the product may also be in jeopardy. Careful design of the packaging techniques, and periodic checks of the manufacturing processes will guarantee moisture levels well below the 5000ppm moisture level. With controlled moisture levels, the long term stability (MTTF) of the product has been demonstrated to several million hours.

PACKAGING

The die are inspected to MIL-STD-883B, method 2010 and sealed in a waffle pack by a certified QC inspector-stamped seal. The waffle pack is dated and initialed by the inspector.

BONDING DIAGRAM



ORDERING INFORMATION*

ADC80 K D

Basic Model Number

Grade/Temperature Range
K = 0°C to +70°C

Package Code
D = Die

*Dice sold in 36-die waffle packs.

PAD ASSIGNMENTS

Pad 1 —Bit 6	Pad 32—Bit 7
Pad 2 —Bit 5	Pad 31—Bit 8
Pad 3 —Bit 4	Pad 30—Bit 9
Pad 4 —Bit 3	Pad 29—Bit 10 (LSB—10 Bits)
Pad 5 —Bit 2	Pad 28—Bit 11
Pad 6 —Bit 1 (MSB)	Pad 27—Bit 12 (LSB—12 Bits)
Pad 7 —NC	Pad 26—Serial Out
Pad 8 —$\overline{\text{Bit 1 (MSB)}}$	Pad 25—$-V_{CC}$
Pad 9 —+5V Digital Supply	Pad 24—Reference Out (+6.3V)
Pad 10—Digital Common	Pad 23—Clock Out
Pad 11—Comparator In	Pad 22—Status
Pad 12—Bipolar Offset	Pad 21—Short Cycle
Pad 13—R1 10V Range	Pad 20—Clock Inhibit
Pad 14—R2 20V Range	Pad 19—External Clock
Pad 15—Analog Common	Pad 18—Convert Command
Pad 16—Gain Adjust	Pad 17—$+V_{CC}$

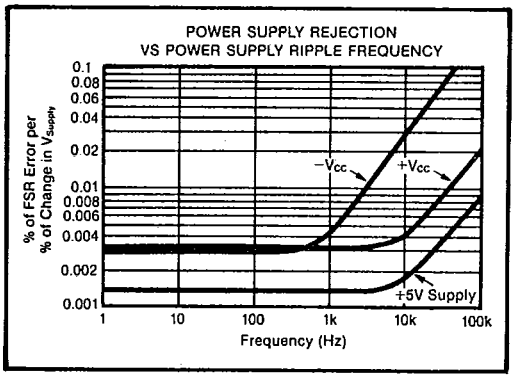
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16.5V
$-V_{CC}$ to Analog Common	0 to −16.5V
V_{DD} to Digital Common	0 to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common	−0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset) to Analog Common	±16.5V
Reference Output	Indefinite Short to Common, Momentary Short to V_{CC}
Process Temperature Extremes	+280°C, 1 minute
Maximum Junction Temperature	+160°C

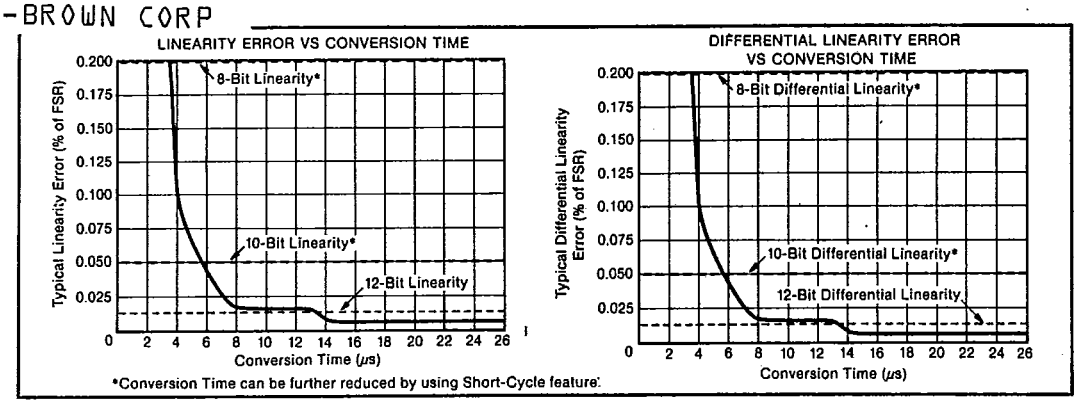
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

TYPICAL PERFORMANCE CURVES



ADC80KD DIE



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

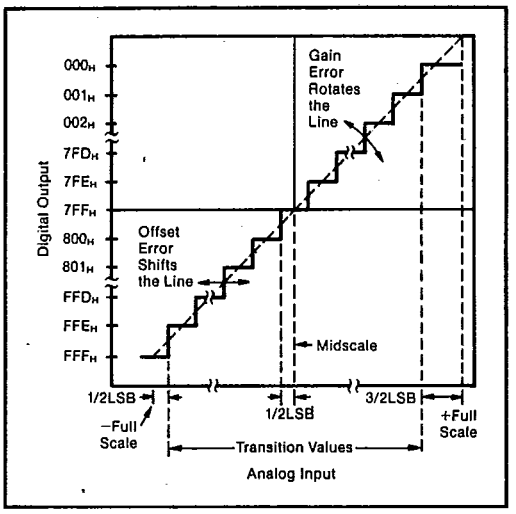


FIGURE 1. Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table I.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB or CTC	COB or CTC	CSB[3]	CSB
One Least Significant Bit (LSB)	$FSR/2^n$	$20V/2^n$	$10V/2^n$	$5V/2^n$	$10V/2^n$	$5V/2^n$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
001_H to 000_H	+ Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2.5V − 3/2LSB	+10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+2.5V
FFF_H to FFE_H	− Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit (MSB). MSB is available on pin 8. (3) CSB = Complementary Straight Binary.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output-code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual +25°C value to the value at the extremes of the specification temperature range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

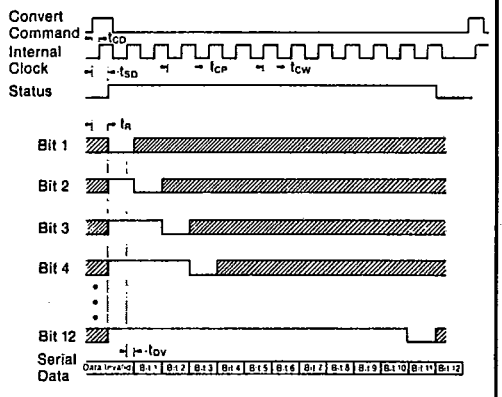
TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the falling edge of the 13th clock pulse, and with valid output data ready to be read at that time.

Additional convert commands applied during conversion will be ignored.

Status remains high until after the falling edge of the 13th clock pulse. This allows direct use of status for latching parallel data.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	153	ns
t_{CP}	Nominal clock period	1.81	µs
t_{CW}	Nominal clock pulse width	0.87	µs
t_{SD}	Status delay from convert command	186	ns
t_R	All bits reset delay from convert command	141	ns
t_{DV}	Data valid time from clock pulse high	−15	ns

FIGURE 2. Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pad 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the die as possible, preferably to an analog common ground plane. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible. Capacitive loading on comparator and input pads should be kept to a minimum to maintain convertor performance.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External padding resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pad 12 To Pad	Connect Pad 14 To Pad	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pad 11	13
0 to +5V	CSB	15	Pad 11	13
0 to +10V	CSB	15	Open	13

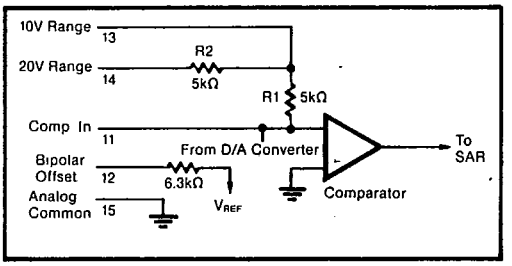


FIGURE 3. Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim resistors connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Adjustment resistors with 100ppm/°C or better TCR are recommended for minimum drift over

temperature and time. These resistors may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pad 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

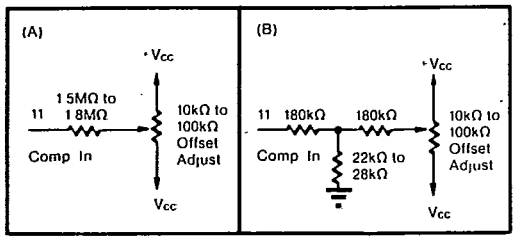


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

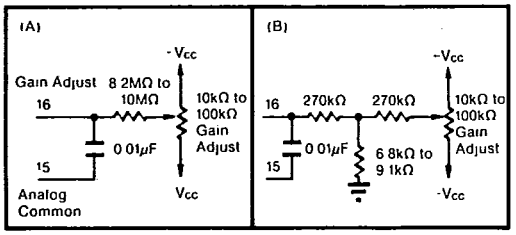


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometric resistors as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transitions to a precisely known value.

CLOCK OPTIONS AND SHORT CYCLE FEATURE

The ADC80 is extremely versatile in that it can be operated in several different modes with either an internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. Pad 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pad 19.

A short-cycle input (pad 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pad should be connected to the bit output pad of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pad 21 is connected to pad 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pad connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Shorter conversion times are possible with an external clock applied to pad 19. With increasing clock speed, linearity performance will begin to degrade as indicated in the Typical Performance Curves. These curves should be used only as guidelines because guaranteed performance is specified and tested only with the internal clock.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80KD

Resolution (Bits)	12	10	8
Connect pad 21 to	Pad 9 or NC	Pad 28	Pad 30
Maximum Conversion Time[1] Internal Clock (μs)	25	22	18
Maximum Linearity Error at +25°C (% of FSR)	0.012	0.048	0.20

NOTE: (1) Conversion time to maintain ±1/2LSB linearity error.

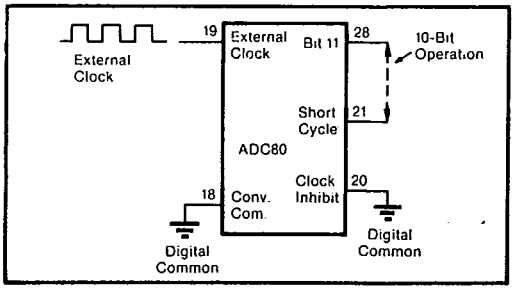


FIGURE 6. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

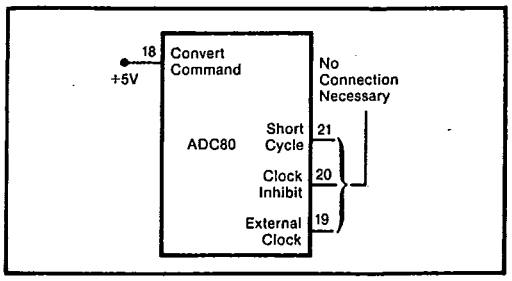


FIGURE 7. Continuous Conversion.

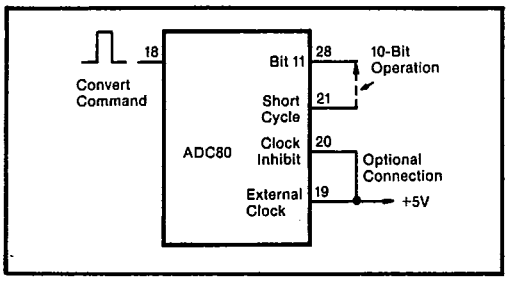


FIGURE 8. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

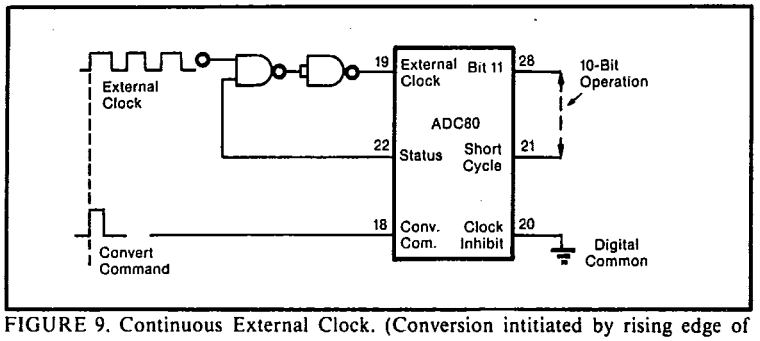


FIGURE 9. Continuous External Clock. (Conversion intitiated by rising edge of convert command. The convert command must be synchronized with clock.)