

SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

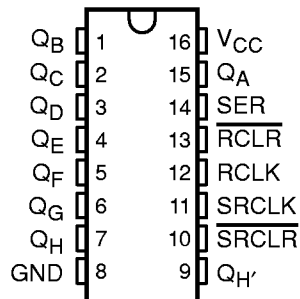
description

The 'AHCT594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{\text{SRCLR}}$, $\overline{\text{RCLR}}$) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

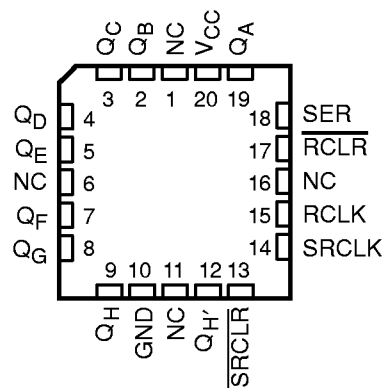
Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

The SN54AHCT594 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT594 is characterized for operation from -40°C to 85°C .

SN54AHCT594 . . . J OR W PACKAGE
SN74AHCT594 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



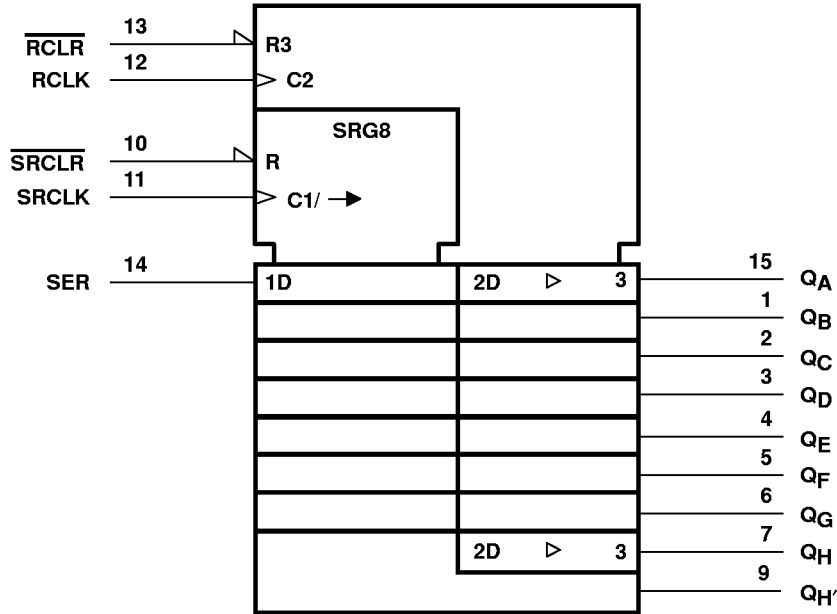
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

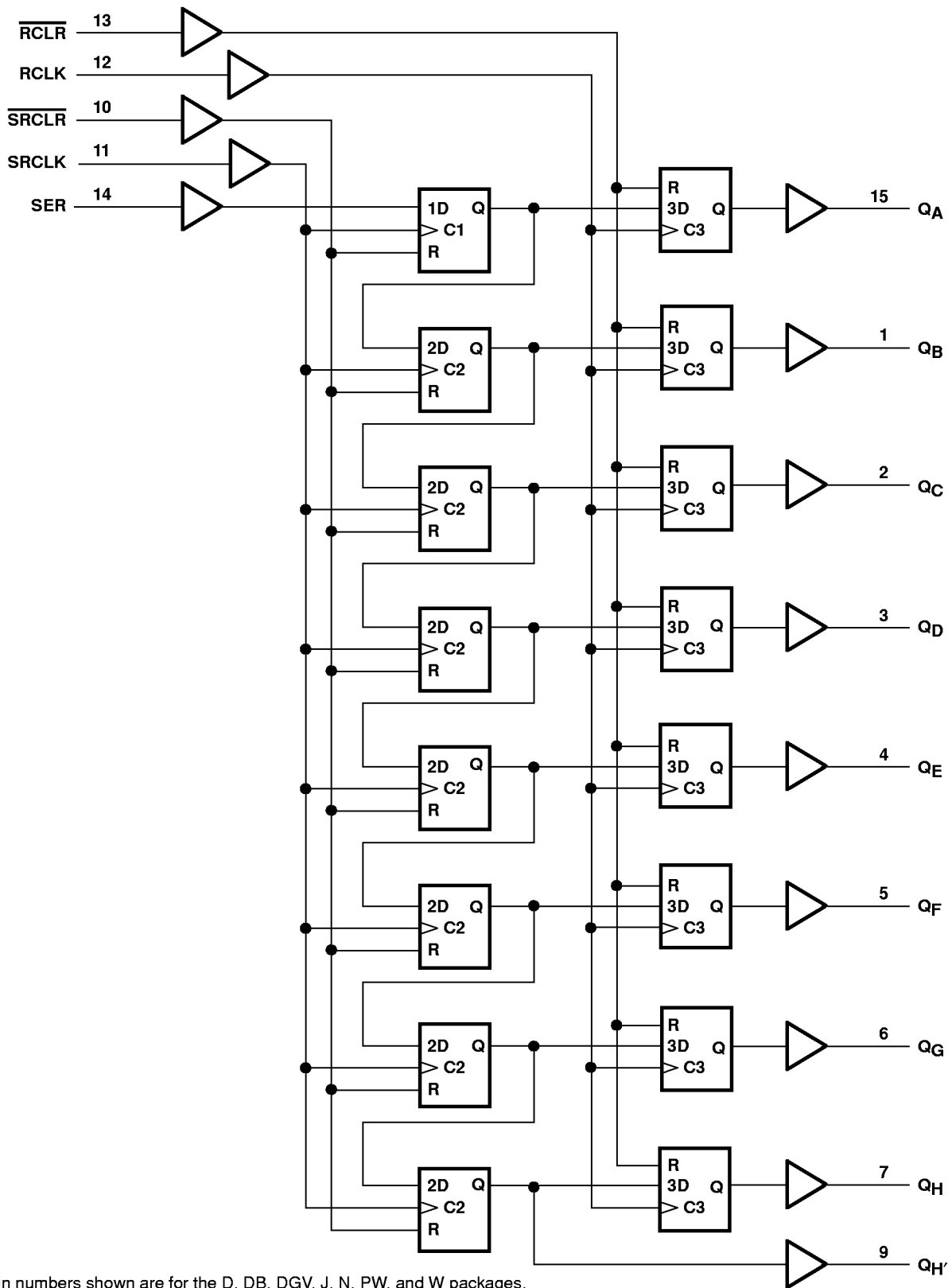
PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594
8-BIT SHIFT REGISTERS
WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
DB package	131°C/W
DGV package	180°C/W
N package	78°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

	SN54AHCT594		SN74AHCT594		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	5.5	0	5.5	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-8		-8	mA
I_{OL} Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20		20	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		SN54AHCT594		SN74AHCT594		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	Q _H [†]	-4		-4	mA
		Q _A -Q _H	-8		-8	
I _{OL}	Low-level output current	Q _H [†]	4		4	mA
		Q _A -Q _H	8		8	
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHCT594		SN74AHCT594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	RCLK or SRCLK high or low						ns
		RCLR or SRCLR low						
t _{su}	Setup time	SER before SRCLK↑						ns
		SRCLK↑ before RCLK↑†						
		SRCLR low before RCLK↑						
		SRCLR high (inactive) before SRCLK↑						
		RCLR high (inactive) before RCLK↑						
t _h	Hold time	SER after SRCLK↑					ns	

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594

8-BIT SHIFT REGISTERS

WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT594					UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			$C_L = 15\text{ pF}^*$						MHz
			$C_L = 50\text{ pF}$						
t_{PLH}^*	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$						ns
t_{PHL}^*									
t_{PLH}^*	SRCLK	$Q_{H'}$	$C_L = 15\text{ pF}$						ns
t_{PHL}^*									
t_{PHL}^*	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 15\text{ pF}$						ns
t_{PHL}^*	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 15\text{ pF}$						ns
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$						ns
t_{PHL}									
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$						ns
t_{PHL}									
t_{PHL}	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 50\text{ pF}$						ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$						ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT594					UNIT
				$T_A = 25^\circ\text{C}$			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			$C_L = 15\text{ pF}$						MHz
			$C_L = 50\text{ pF}$						
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$						ns
t_{PHL}									
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15\text{ pF}$						ns
t_{PHL}									
t_{PHL}	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 15\text{ pF}$						ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 15\text{ pF}$						ns
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$						ns
t_{PHL}									
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$						ns
t_{PHL}									
t_{PHL}	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 50\text{ pF}$						ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$						ns
$t_{\text{sk(o)}}^\dagger$			$C_L = 50\text{ pF}$						ns

† Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594
8-BIT SHIFT REGISTERS
WITH OUTPUT REGISTERS

SCLS417 – JUNE 1998

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHCT594			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$ High-level dynamic input voltage				V
$V_{IL(D)}$ Low-level dynamic input voltage				V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$		pF

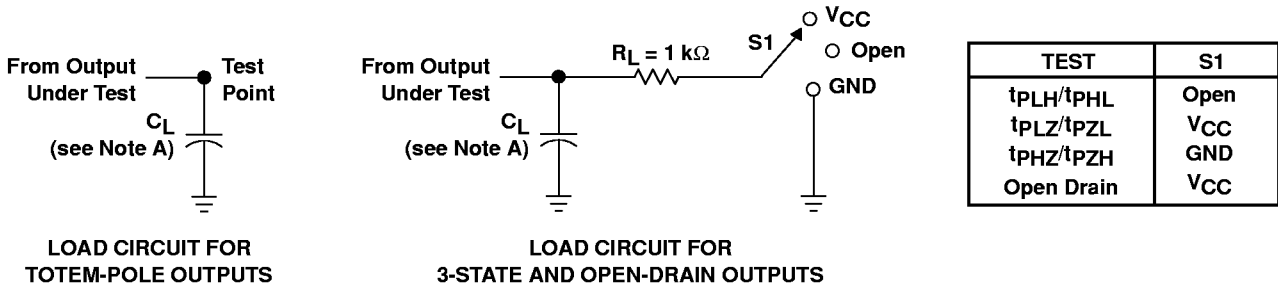
PRODUCT PREVIEW



SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

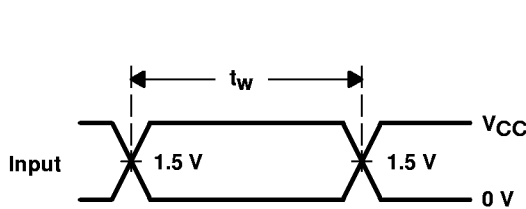
SCLS417 – JUNE 1998

PARAMETER MEASUREMENT INFORMATION

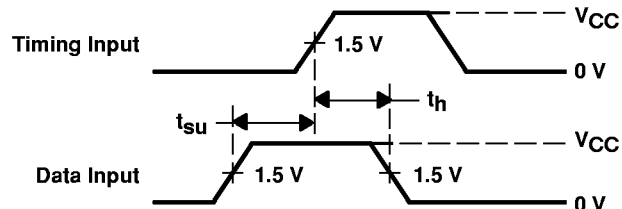


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

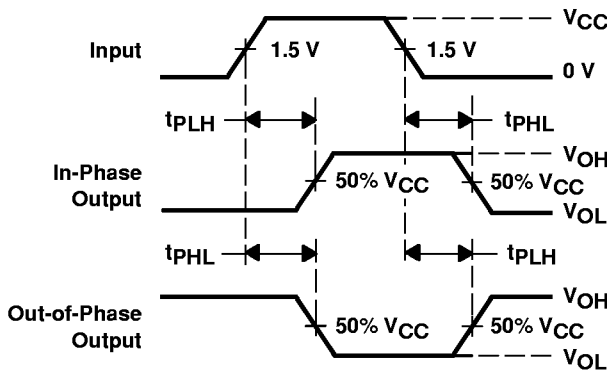
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



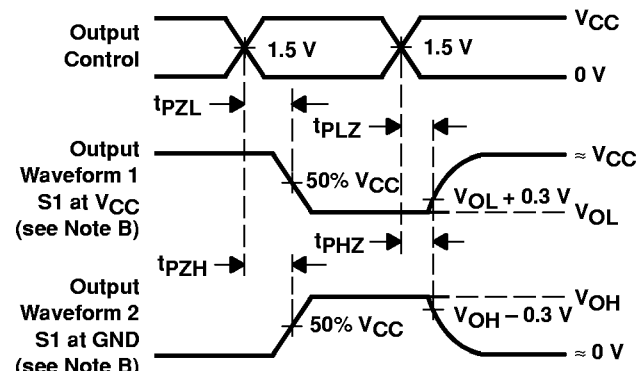
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.