High Speed CMOS Bus Exchange Switches with Extended Voltage Range

QS3386

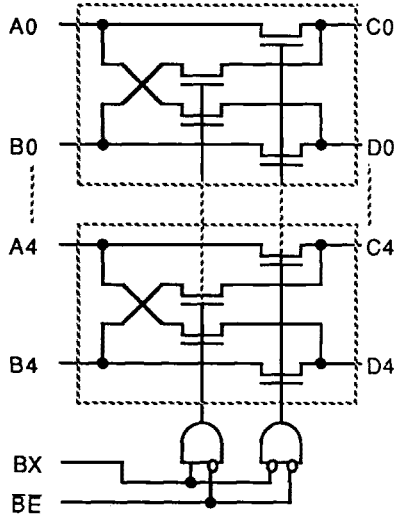
FEATURES/BENEFITS

- 7Ω switches connect inputs to outputs
- Uses Vcc of +5 and Vee of -2
- Zero propagation delay
- Undershoot Clamp diodes on all inputs
- Low power CMOS proprietary technology
- Provides routing of ECL signals
- Bus exchange allows nibble swap
- Zero ground bounce in flow-through mode
- TTL compatible control inputs
- Available in 24-pin DIP, ZIP, SOIC, and QSOP

DESCRIPTION

The QS3386 each provide two sets of ten high-speed CMOS bus switches with a signal range of +5 to -2 volts, allowing routing of ECL signals. These devices can also be used to route video and RF signals with voltage ranges of ±2 volts (4 volts peak to peak). The low on resistance (7Ω) of the 3386 allows inputs to be connected to outputs without adding propagation delay and without generating additional noise. Control inputs operate at TTL levels. The bus enable (BE) signal turns the switches on. The bus exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

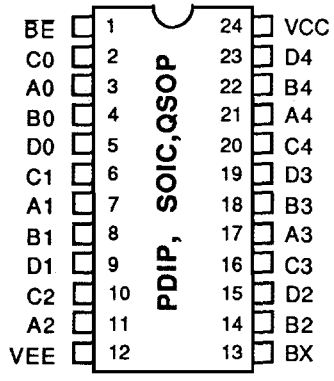
Name	I/O	Function
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

FUNCTION TABLE

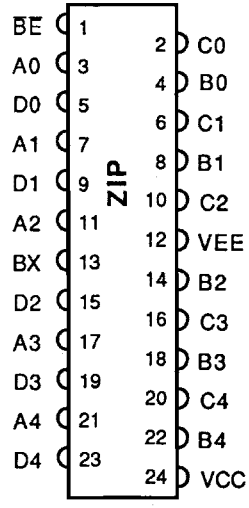
$\overline{BE}$	BX	A0-4	B0-4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

7

PIN CONFIGURATIONS



ALL PINS TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Vee..... -0.5V to +7.5V
DC Switch Voltage V_S ..... V_{ee} -0.5V to V_{ee} + 7.5V
DC Input Voltage V_I ..... V_{ee} -0.5V to V_{ee} + 7.5V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Channel Current Max. sink current/pin.....120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG}Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC		QSOP		PDIP,PLCC		ZIP		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Controls	3	4	3	4	4	5	6	7	pF
QuickSwitch Channels	7	8	7	8	8	9	10	11	pF

Note: Capacitance is characterized but not tested

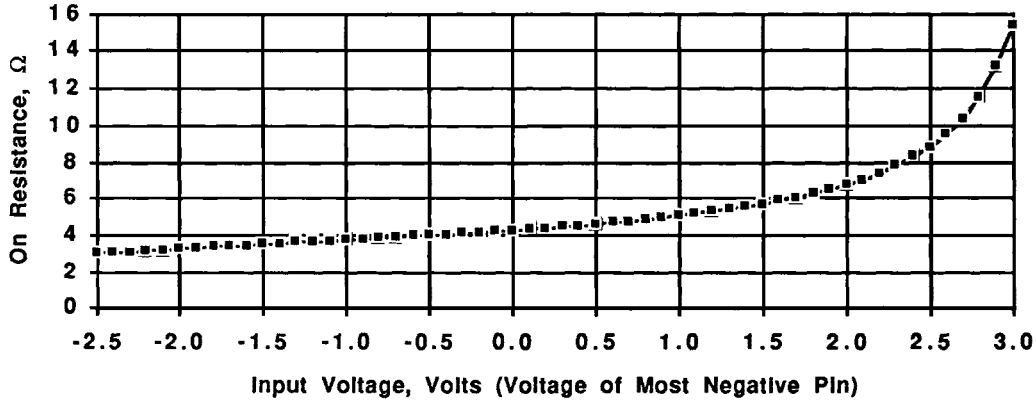
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Paramete	Test	Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs Vee=-2V	2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs Vee=-2V	-	-	0.8	Volts
| Iin |	Input Leakage Current	Vee ≤ Vin ≤ Vcc	-	-	1	µA
| Ioz |	Off State Current (Hi-Z)	Vee ≤ A, B ≤ Vcc	-	.001	1	µA
| Ios |	Short Circuit Current (2)	A (B) = 0V, B (A) = Vcc	-	300	-	mA
Vic	Clamp Diode Voltage	Vcc = Min, Iin = -18 mA	-	Vee -0.7	Vee -1.2	Volts
Ron	Switch On Resistance (Note 3)	Vcc = Min, Vin = 0.0 Volts Ion = 30 mA	-	7	9	Ω
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	-	12	17	Ω

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤1 second.
3. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A, B) pins.

On Resistance vs Input Voltage at 4.75 Volts Vcc



7

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, Vi = GND or Vcc, f = 0	-	-	3.0	mA
ΔIcc	Pwr Supply Current, per Input High (2)	Vcc = MAX, Input = 3.4 V, f = 0 Per control input	-	-	5.0	mA
Qccd	Dynamic Pwr Supply Current per mHz (3)	Vcc = MAX, A & B pins open, Control input toggling @ 50% duty cycle	-	-	0.5	mA/ mHz
Ic	Total Power Supply Current (4,5)	Vcc = MAX, A & B pins at 0.0V, Control inputs toggling @ 50% duty cycle Vih = 3.4V, f clock = 10 mHz	-	-	18	mA

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V, control inputs only). A and B pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.
4. Calculated parameter, applies to control inputs only.
   Ic= I Quiescent + I Inputs+ I Dynamic
   Ic=Icc+ ΔIccDhNt+ Qccd (fiNi)
   Icc= Quiescent Current
   ΔIcc= Power Supply Current for each TTL High input (Vi=3.4V, control inputs only)
   Dh= Duty Cycle for each TTL input that is High (control inputs only).
   Nt= Number of TTL inputs that are at DH (control inputs only).
   fi= frequency that the inputs are toggled (control inputs only).
5. Note that activity on A and/or B inputs do not contribute to Ic if A and B inputs are between gnd and Vcc. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A and B pins.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5% Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t PLH t PHL	Data Propagation Delay Ai to Bi, Bi to Ai	2,3		0.25		0.25	ns
t PZH t PZL	Switch Turn On Delay BE to Ai, Bi		1.5	6.5	1.5	7.5	ns
t PLZ t PHZ	Switch Turn Off Delay BE to Ai, Bi	2	1.5	5.5	1.5	6.5	ns
t BX	Switch Multiplex Delay BX to Ai, Bi		1.5	6.5	1.5	7.5	ns
| Qci |	Charge Injection, Typical	2, 4		2.0		2.0	pC
| Qdci |	Differential Charge Injection, Typical	2, 5		<.5		<.5	pC

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pf load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4) Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
5) Measured at switch turn off through bus multiplex, A to C => A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.