

FEATURES

- Function, Pinout and Drive Compatible with the FCT and F Logic
- FCT-A speed at 5.1ns max (MIL)
- Output levels compatible with TTL and CMOS
- Edge-rate control circuitry for significantly improved noise characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- 48 mA sink current, 12 mA source current (MIL)



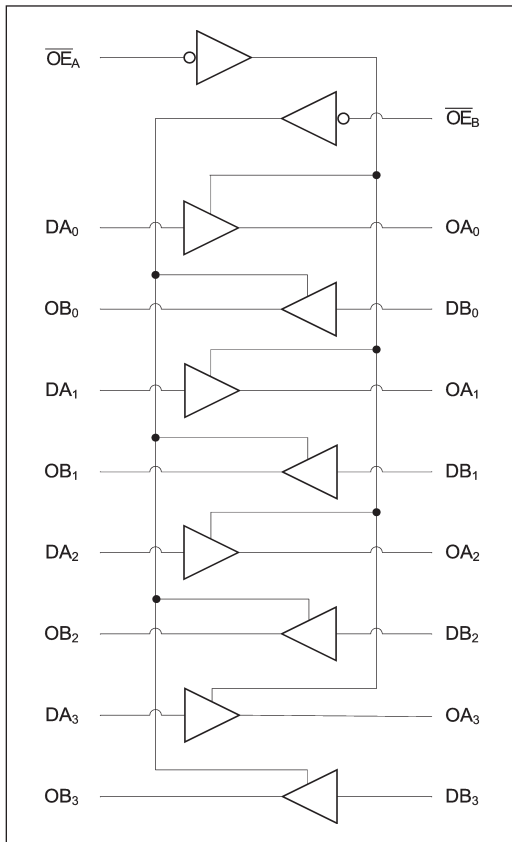
DESCRIPTION

The P54/74FCT244 is a non-inverting octal buffer and line driver designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. The device provides speed and drive capabilities equivalent to the fastest bipolar logic counterparts while reducing

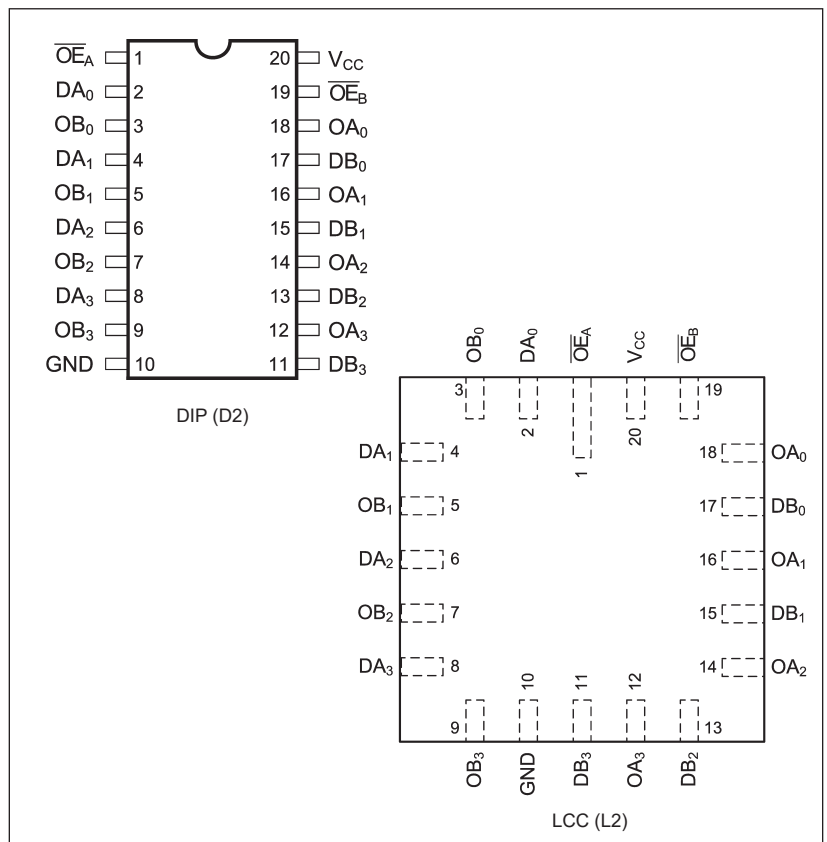
power dissipation by using advanced CMOS technology. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without external components.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



**MAXIMUM RATINGS**^(1,2)

Sym	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-65 to +135	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
P _T	Power Dissipation	0.5	W
I _{OUTPUT}	Current Applied to Output	120	mA
V _{IN}	Input Voltage	-0.5 to +7.0	V
V _{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Grade	Ambient Temp	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 5%

CAPACITANCES(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	Test Conditions	Min	Max	Unit
V _{OH}	High Level Output Voltage	V _{CC} = 3.0V, V _{IH} = 2.8 V, V _{IL} = 0.2V I _{OH} = -32 µA	2.8		V
		V _{CC} = V _{CC} (Min) V _{IH} = 2.0 V, V _{IL} = 0.8 V	4.3		
		I _{OH} = -300 µA I _{OH} = -12 mA	2.4		
V _{OL}	Low Level Output Voltage	V _{CC} = 3.0V, V _{IH} = 2.8 V, V _{IL} = 0.2V I _{OH} = 300 µA		0.2	V
		V _{CC} = V _{CC} (Min) V _{IH} = 2.0 V, V _{IL} = 0.8 V		0.2	
		I _{OL} = 300 µA I _{OL} = 48 mA		0.55	
V _{IK}	Input Clamp Voltage	V _{CC} = V _{CC} (Min), I _{IN} = -18mA		-1.2	V
I _{IH}	High Level Input Current	V _{CC} = V _{CC} (Max), V _{IN} = V _{CC}		5.0	µA
I _{IL}	Low Level Input Current	V _{CC} = V _{CC} (Max), V _{IN} = GND		-5.0	µA
I _{OZH}	High Impedance Output Current	V _{CC} = V _{CC} (Max), V _{IN} = V _{CC}		10	µA
I _{OZL}		V _{CC} = V _{CC} (Max), V _{IN} = GND		-10	
I _{OS}	Short Circuit Output Current	V _{CC} = V _{CC} (Max)	-60		mA
I _{CCQ}	Quiescent Power Supply Current (CMOS inputs)	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V V _{CC} = V _{CC} (Max) f _i = 0 MHz		1.5	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} = V _{CC} (Max) V _{IN} = 3.4 V		2.0	mA
I _{CCD}	Dynamic Power Supply Current	V _{CC} = V _{CC} (Max) Outputs open One bit toggling 50% duty cycle V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V OE _A = OE _B = GND		0.4	mA/ MHz

Notes:

- Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

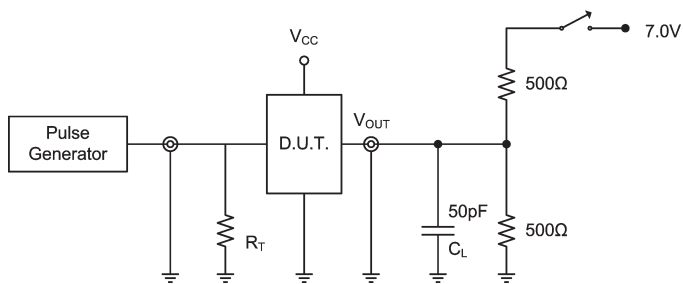


Sym	Parameter	Test Conditions	Min	Max	Unit	
I _{CC}	Total Power Supply Current	V _{CC} = V _{CC} (Max) Outputs open, OE _A = OE _B = GND 50% duty cycle	f _i = 10 MHz One bit toggling	V _{IN} ≥ 5.3 V or V _{IN} ≤ 0.2 V	5.5	mA
				V _{IN} = 3.4 V or V _{IN} = GND	6.0	mA
			f _i = 2.5 MHz Eight bits toggling	V _{IN} ≥ 5.3 V or V _{IN} ≤ 0.2 V	6.5	mA
				V _{IN} = 3.4 V or V _{IN} = GND	14.5	mA
C _{IN}	Input Capacitance	T _C = +25°C, V _{CC} = GND, F = 1 MHz		10	pF	
C _{OUT}	Output Capacitance	T _C = +25°C, V _{CC} = GND, F = 1 MHz		12	pF	

AC CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

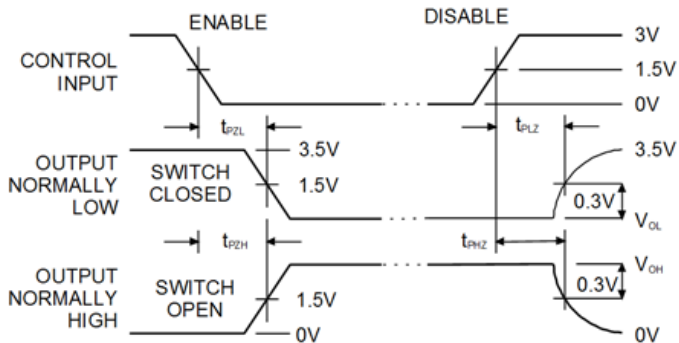
Sym	Parameter	Condition	54/74FCT244				54/74FCT244A				Unit
			Ind		Mil		Ind		Mil		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _x to O _x	C _L = 50pF R _L = 500Ω	1.5	6.5	1.5	7.5	1.5	4.8	1.5	5.1	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	8.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.6	1.5	5.9	ns



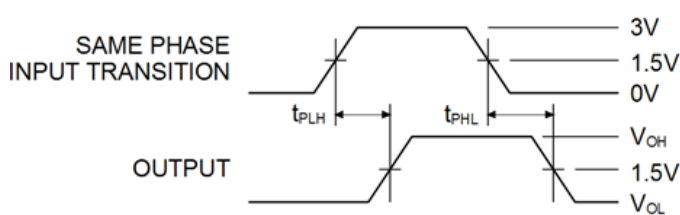
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open



ENABLE/DISABLE TIMES



PROPAGATION DELAY



PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	Output Enable Inputs (Active LOW)
Dxx	Inputs
Oxx	Outputs

FUNCTION TABLE

Inputs			Outputs
\overline{OE}_A	\overline{OE}_B	D	Oxx
L	L	L	L
L	L	H	H
H	H	X	Z

H = High Voltage Level
 X = Don't Care
 L = Low Voltage Level
 Z = High Impedance

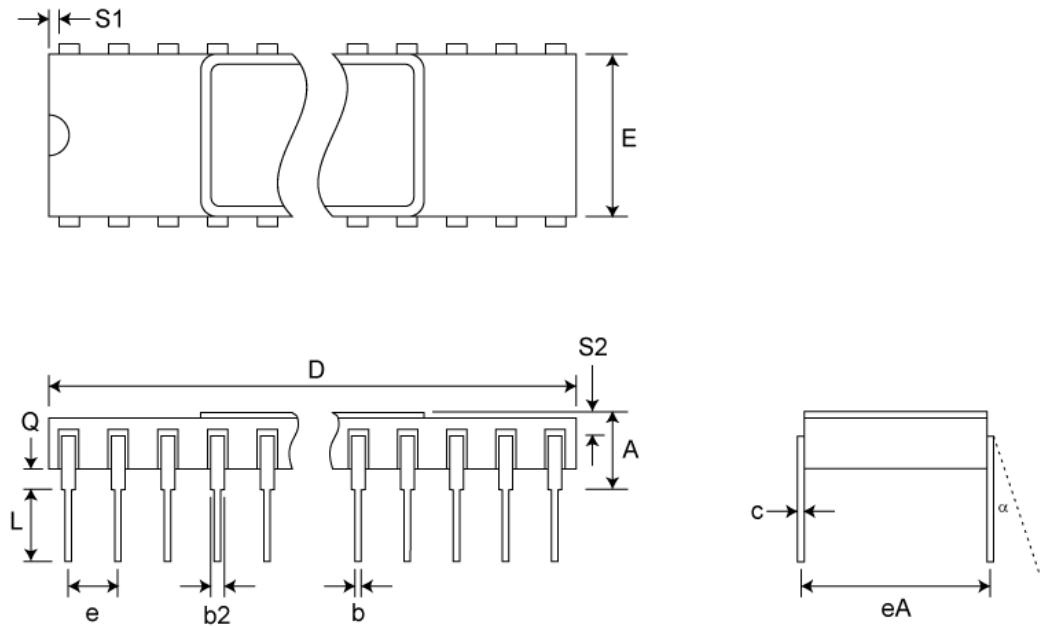
ORDERING INFORMATION

PxxFCT	xx	x	x	
Temp. Class	Device Type	Package	Processing	
			I	-40°C to +85°C
			M	-55°C to +125°C
			MB	Mil Temp with MIL-STD-883 Class B Compliance
			C	Ceramic side brazed DIP, 300 mil
			L	Square LCC (350x350 mil)
			244	Octal Buffer/Line Driver
			244A	Fast Octal Buffer/Line Driver
			74	Industrial
			54	Military



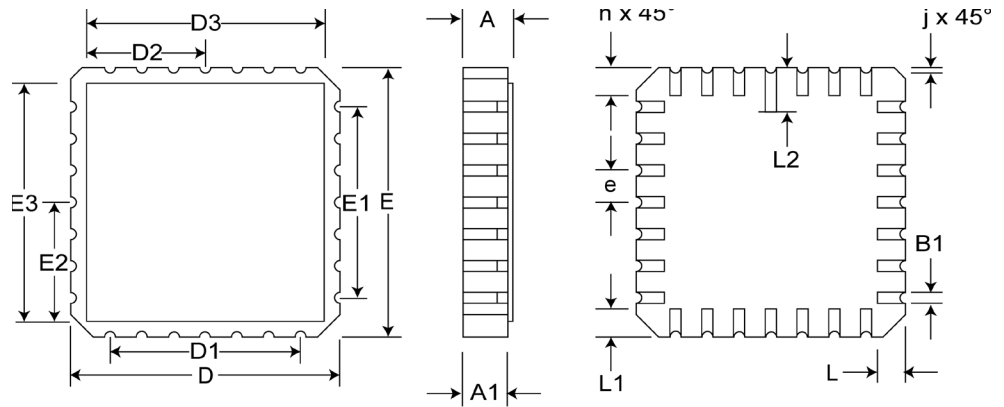
SIDEBRAZED DUAL INLINE PACKAGE

Pkg #	D2	
# Pins	20 (300 mil)	
Symbol	Min	Max
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	-	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-
α	0°	15°



SQUARE LEADLESS CHIP CARRIER

Pkg #	L2	
# Pins	20	
Symbol	Min	Max
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.342	0.358
D1/E1	0.200 BSC	
D2/E2	0.100 BSC	
D3/E3	-	0.358
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	5	



**REVISIONS**

DOCUMENT NUMBER	LOGIC102
DOCUMENT TITLE	P54FCT244 - OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Sep 2015	JDB	New Data Sheet
01	Feb 2016	JDB	Corrections on DC Electrical Characteristics
02	Feb 2016	JDB	Corrections on DC Electrical Characteristics
03	Feb 2016	JDB	Updated DIP package drawing
04	Mar 2016	JDB	Pin Description table
05	Mar 2016	JDB	DC Electrical Characteristics