ARITHMETIC LOGIC UNIT/FUNCTION GENERATORS

The TC74HC181A is a high speed CMOS ARITHMETIC LOGIC UNIT(ALU)/FUNCTION GENERATOR fabricated with silicon gate C^2MOS technology.

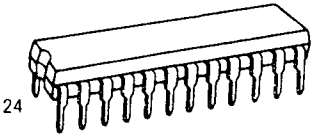
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. The operations are selected by the four function select line (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transter. When performing arithmetic manipulatations, the internal carries must be enabled by setting the Mode Control (M) input low. A full carry look-ahead scheme is provided for fast, simultaneous carry generation by means of two cascade outputs (pins 15 and 17) for the four bits in the device. When used in conjunction with the TC74 HC182A FULL CARRY LOOK-AHEAD device, high speed arithmetic operations can be performed.

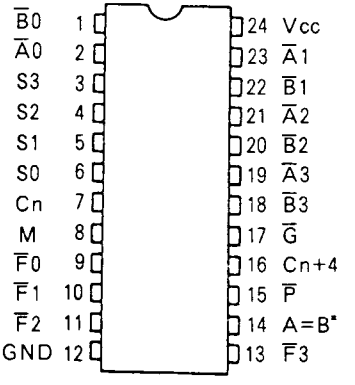
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=23ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS181



PIN ASSIGNMENT



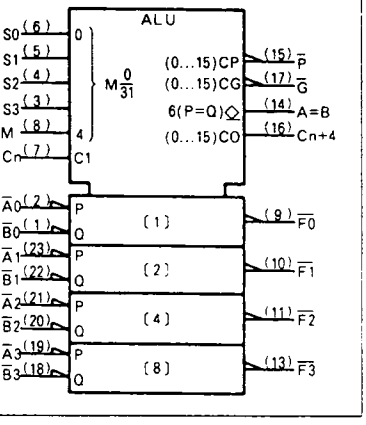
(TOP VIEW)

•OPEN DRAIN OUTPUT STRUCTURE

PIN DESIGNAIONS

Designations	Pin No.	Function
$\overline{A}0,\overline{A}1,\overline{A}2,\overline{A}3$	2,23,21,19	Word A Inputs
$\overline{B}0,\overline{B}1,\overline{B}2,\overline{B}3$	1,22,20,18	Word B Inputs
S0,S1,S2,S3	6,5,4,3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F}0,\overline{F}1,\overline{F}2,\overline{F}3$	9,10,11,13	Function Outputs
A=B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
Vcc	24	Supply Voltage
GND	12	Ground

IEC LOGIC SYMBOL



FUNCTION DESCRIPTION

The TC74HC181A will accomodate active-high or active-low data, if the pin designations are interpreted as shown below.

Pin No.	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn+4	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{Cn}$	$\overline{Cn+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to produce A-B.

The TC74HC181A can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with Cn = high when performing this comparison. The A = B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn + 4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by setting the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output Cn+4	Active-Low data (Figure 1)	Active-High data (Figure 2)
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function select inputs (S0, S1, S2. S3) with the mode control input (M) at a high level to disable the internal carry.

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1 ; those obtained with signal designations of Figure 2 are given in Table 2.

FUNCTION DESCRIPTION (Continued)

Figure 1

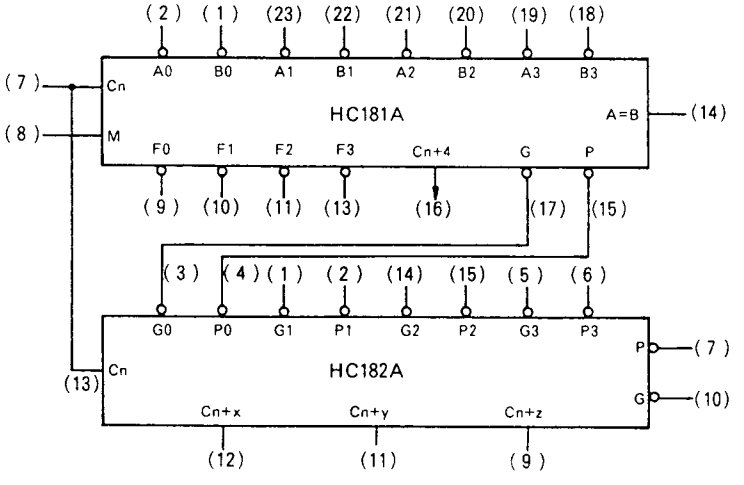


Table 1

Selection				Active Low Data		
				M=H	M=L : Arithmetic Operations	
S3	S2	S1	S0	Logic Function	Cn=L(no carry)	Cn=H(with carry)
L	L	L	L	$F=\overline{A}$	F=A Minus 1	F=A
L	L	L	H	$F=\overline{A\,B}$	F=AB Minus 1	F=AB
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ Minus 1	$F=(A\overline{B})$
L	L	H	H	F=1	F=Minus 1 (2' S Compl)	F=Zero
L	H	L	L	$F=\overline{A+B}$	F=A Plus $(A+\overline{B})$	F=A Plus $(A+\overline{B})$ Plus 1
L	H	L	H	$F=\overline{B}$	F=AB Plus (A+B)	F=AB Plus $(A+\overline{B})$ Plus 1
L	H	H	L	$F=\overline{A\oplus B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	$F=(A+\overline{B})$ Plus 1
H	L	L	L	$F=\overline{A}B$	F=A Plus (A+B)	F=A Plus (A+B) Plus 1
H	L	L	H	$F=A\oplus B$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	$F=A\overline{B}$ Plus (A+B)	$F=A\overline{B}$ Plus (A+B) Plus 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) Plus 1
H	H	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	$F=A\overline{B}$	F=AB Plus A	F=AB Plus A Plus 1
H	H	H	L	F=AB	$F=A\overline{B}$ Plus A	$F=A\overline{B}$ Plus A Plus 1
H	H	H	H	F=A	F=A	F=A Plus 1

* Each bit is shifted to the next more significant position.

FUNCTION DESCRIPTION (Continued)

Figure 2

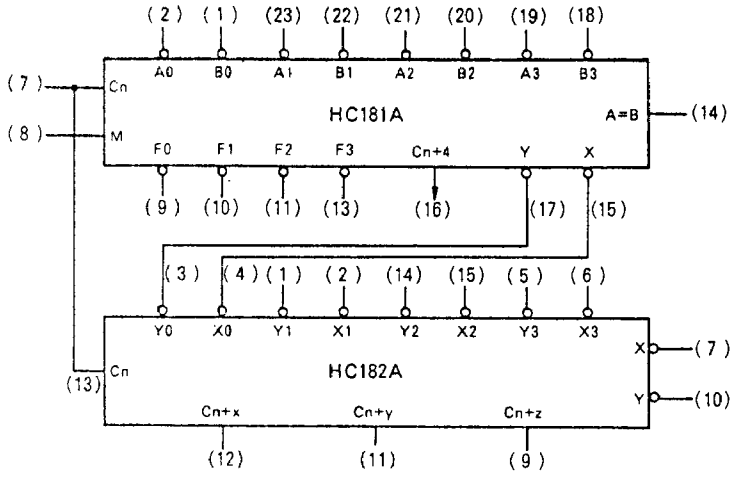
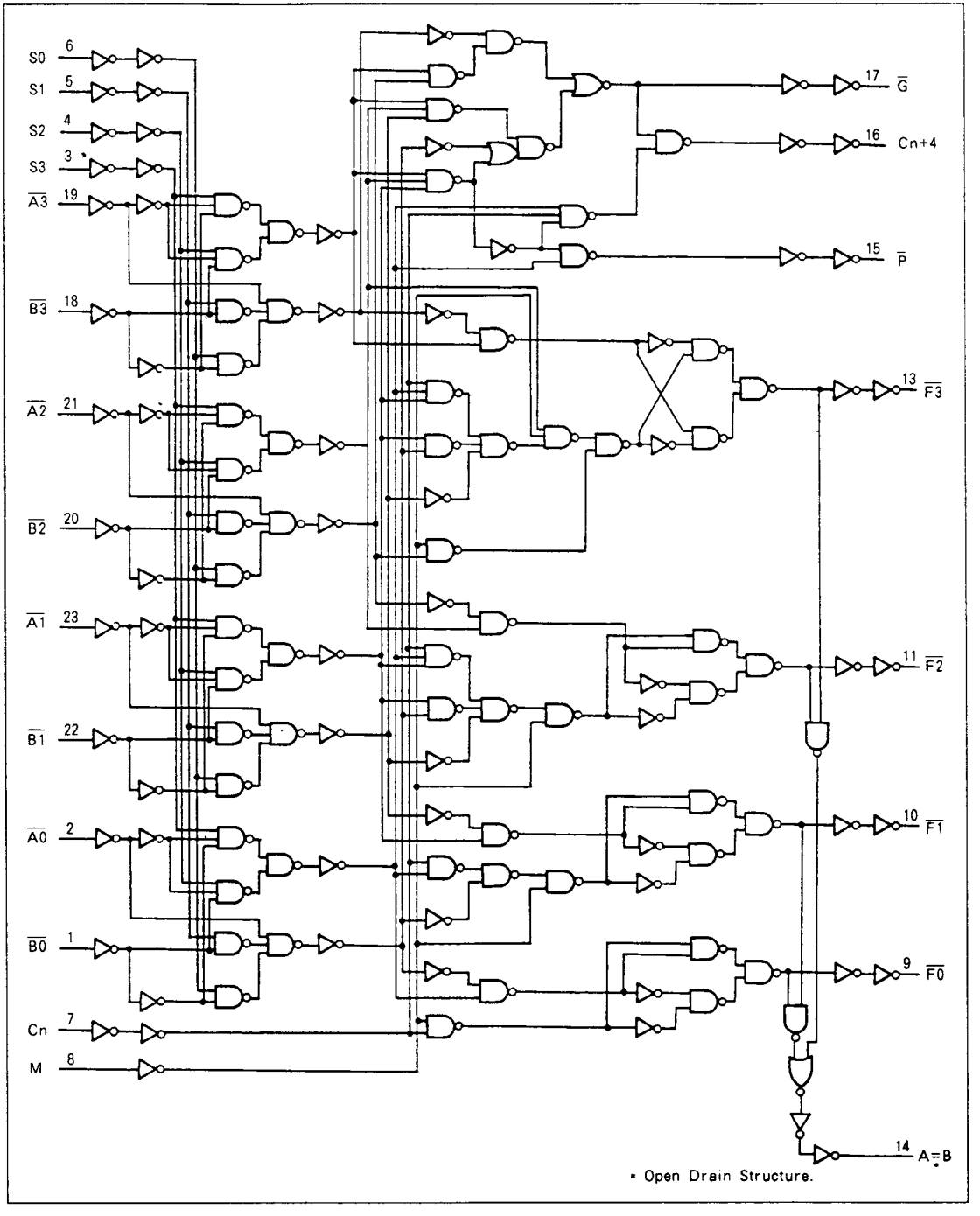


Table 2

Selection				Active Low Data		
				M=H	M=L : Arithmetic Operations	
S3	S2	S1	S0	Logic Function	Cn=H(no carry)	Cn=L(with carry)
L	L	L	L	$F=\overline{A}$	F=A	F=A Plus 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) Plus 1
L	L	H	L	$F=\overline{A}B$	F=A+$\overline{B}$	F=(A+$\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Compl)	F=Zero
L	H	L	L	$F=\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	$F=\overline{B}$	F=(A+B) Plus A$\overline{B}$	F=(A+B) Plus A$\overline{B}$ Plus 1
L	H	H	L	$F=A\oplus B$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A+$\overline{B}$) Plus AB	F=(A+$\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A+$\overline{B}$	F=(A+B) Plus A	F=(A+B) Plus A Plus 1
H	H	H	L	F=A+B	F=(A+$\overline{B}$) Plus A	F=(A+$\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

* Each bit is shifted to the next more significant position.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (1)	t_{pLH} t_{pHL}		–	13	20	
Propagation Delay Time (2)	t_{pLH} t_{pHL}		–	22	37	
Propagation Delay Time (3)	t_{pLH} t_{pHL}		–	23	37	
Propagation Delay Time (4)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (5)	t_{pLH} t_{pHL}		–	20	33	
Propagation Delay Time (6)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (7)	t_{pLH} t_{pHL}		–	19	29	
Propagation Delay Time (8)	t_{pLH} t_{pHL}		–	19	29	
Propagation Delay Time (9)	t_{pLH} t_{pHL}		–	23	38	
Propagation Delay Time (10)	t_{pLH} t_{pHL}		–	23	38	
Propagation Delay Time (11)	t_{pLH} t_{pHL}		–	20	35	
3 State Output Enable Time (12)	t_{pZL}	R_L = 1kΩ	–	25	36	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (1)	t_{pLH} t_{pHL}		2.0	−	54	120	−	150	
			4.5	−	16	24	−	30	
			6.0	−	13	20	−	26	
Propagation Delay Time (2)	t_{pLH} t_{pHL}		2.0	−	90	215	−	270	
			4.5	−	26	43	−	54	
			6.0	−	20	37	−	46	
Propagation Delay Time (3)	t_{pLH} t_{pHL}		2.0	−	97	215	−	270	
			4.5	−	27	43	−	54	
			6.0	−	21	37	−	46	
Propagation Delay Time (4)	t_{pLH} t_{pHL}		2.0	−	80	180	−	225	
			4.5	−	23	36	−	45	
			6.0	−	18	31	−	38	
Propagation Delay Time (5)	t_{pLH} t_{pHL}		2.0	−	81	190	−	240	
			4.5	−	24	38	−	48	
			6.0	−	19	32	−	41	
Propagation Delay Time (6)	t_{pLH} t_{pHL}		2.0	−	80	180	−	225	
			4.5	−	23	36	−	45	
			6.0	−	18	31	−	38	
Propagation Delay Time (7)	t_{pLH} t_{pHL}		2.0	−	80	170	−	215	
			4.5	−	23	34	−	43	
			6.0	−	18	29	−	37	
Propagation Delay Time (8)	t_{pLH} t_{pHL}		2.0	−	80	170	−	215	
			4.5	−	23	34	−	43	
			6.0	−	18	29	−	37	
Propagation Delay Time (9)	t_{pLH} t_{pHL}		2.0	−	95	220	−	275	
			4.5	−	27	44	−	55	
			6.0	−	21	37	−	47	
Propagation Delay Time (10)	t_{pLH} t_{pHL}		2.0	−	95	220	−	275	
			4.5	−	27	44	−	55	
			6.0	−	21	37	−	47	
Propagation Delay Time (11)	t_{pLH} t_{pHL}		2.0	−	86	200	−	250	
			4.5	−	24	40	−	50	
			6.0	−	18	34	−	43	
3-State Output Disable Time (12)	t_{pLZ}	R_L=1kΩ	2.0	−	95	210	−	265	
			4.5	−	29	42	−	53	
			6.0	−	23	36	−	45	
3-State Output Enable Time (12)	t_{pZL}	R_L=1kΩ	2.0	−	92	210	−	265	
			4.5	−	27	42	−	53	
			6.0	−	22	36	−	45	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	195	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC\,(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TEST No.	INPUT	OUTPUT	TEST CONDITIONS
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND,S0=S3=Vcc,S1=S2=GND($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND,S0=S3=GND,S1=S2=Vcc($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M=GND($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND,S0=S3=Vcc,S1=S2=GND($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND,S0=S3=GND,S1=S2=Vcc($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND,S0=S3=Vcc,S1=S2=GND($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND,S0=S3=GND,S1=S2=Vcc($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND,S0=S3=Vcc,S1=S2=GND($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND,S0=S3=GND,S1=S2=Vcc($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=Vcc(Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A=B	M=GND,S0=S3=GND,S1=S2=Vcc($\overline{DIFF}$ mode)