MC10154

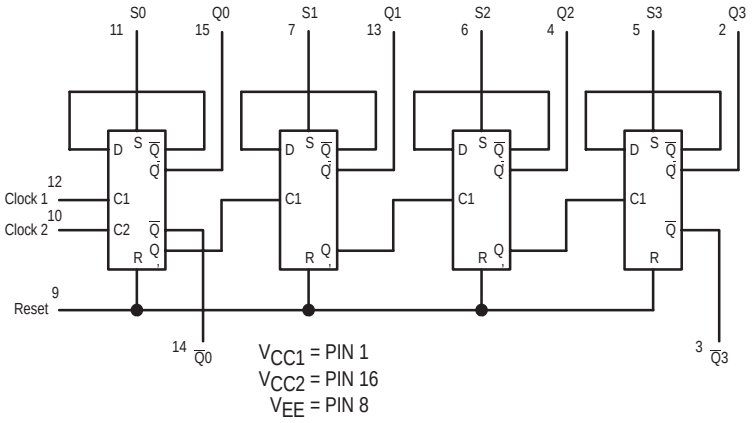
Binary Counter

The MC10154 is a four–bit counter capable of divide–by–two, divide–by– four, divide–by–eight or a divide–by–sixteen function.

Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous “set” or “clear.” Individual Set and common Reset inputs are provided, as well as complemen– tary outputs for the first and fourth bits. True outputs are available at all bits.

- P_D=370 mW typ/pkg (No Load)
- f_{toggle}= 150 MHz (typ)
- t_{pd}=3.5 ns typ (C to Q_0)
- t_{pd}=11 ns typ (C to Q_3)

LOGIC DIAGRAM



TRUTH TABLE

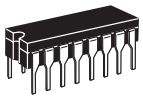
INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	No Count			
L	L	L	L	L	X	H	No Count			
L	L	L	L	L	*	*	H	H	H	H
L	L	L	L	L	*	*	L	H	H	H
L	L	L	L	L	*	*	H	L	H	H
L	L	L	L	L	*	*	L	L	H	H
L	L	L	L	L	*	*	H	H	L	H
L	L	L	L	L	*	*	L	H	L	H
L	L	L	L	L	*	*	H	L	L	H
L	L	L	L	L	*	*	L	L	L	H
L	L	L	L	L	*	*	H	H	H	L
L	L	L	L	L	*	*	L	H	H	L
L	L	L	L	L	*	*	H	L	H	L
L	L	L	L	L	*	*	L	L	H	L
L	L	L	L	L	*	*	H	H	L	L
L	L	L	L	L	*	*	L	H	L	L
L	L	L	L	L	*	*	H	L	L	L
L	L	L	L	L	*	*	L	L	L	L

* Clock transitions from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

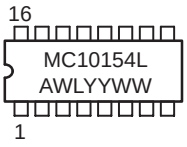
ON Semiconductor

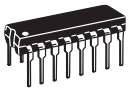
http://onsemi.com

MARKING DIAGRAMS

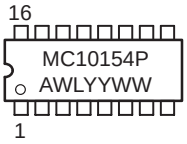


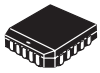
CDIP–16
L SUFFIX
CASE 620



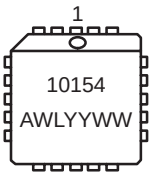


PDIP–16
P SUFFIX
CASE 648



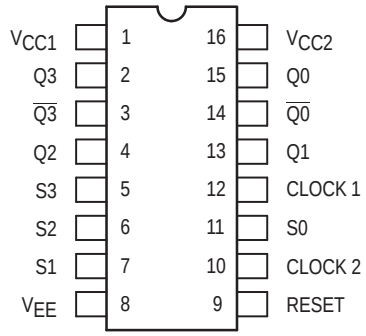


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10154L	CDIP–16	25 Units / Rail
MC10154P	PDIP–16	25 Units / Rail
MC10154FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		97			88		97	mAdc
Input Current	I_{inH}	12 11 9		390 350 650			245 220 410		245 220 410	µAdc
	I_{inL}	*	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 15	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 15	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	3 14 15	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3 14 15		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Clock Input Propagation Delay	t_{12+15+} t_{12-13-} t_{12+4-} t_{12-3+}	15 13 4 3	1.4 1.9 2.9 3.9	5.0 9.4 12.3 14.9	1.5 2.0 3.0 4.0	3.5 6.0 8.5 11.0	4.8 9.2 12.0 14.5	1.5 2.0 3.0 4.0	5.3 9.8 12.8 15.5	
Rise Time (20 to 80%)	t_{15+}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Fall Time (20 to 80%)	t_{15-}	15	1.1	4.7	1.1	2.5	4.5	1.1	5.0	
Set Input Reset Input	t_{11-15+} t_{9-15+}	15 15	1.4 1.4	5.2 5.2	1.5 1.5		5.0 5.0	1.5 1.5	5.5 5.5	
Counting Frequency	f_{count}	15	125		125	150		125		MHz

* Individually test each input applying V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8	9				8	1, 16
Input Current		I_{inH}	12 11 9	12 11 9				8 8 8	1, 16 1, 16 1, 16
		I_{inL}	*		*			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 15	9 11				8 8	1, 16 1, 16
Output Voltage	Logic 0	V_{OL}	14 15	11 9				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V_{OHA}	3 14 15			5 11 9		8 8 8	1, 16 1, 16 1, 16
Threshold Voltage	Logic 0	V_{OLA}	3 14 15				5 11 9	8 8 8	1, 16 1, 16 1, 16
Switching Times	(50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0V**
Clock Input Propagation Delay		t_{12+15+} $t_{12–13–}$ $t_{12+4–}$ $t_{12–3+}$	15 13 4 3			12 12 12 12	15 13 4 3	8 8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t_{15+}	15			12	15	8	1, 16
Fall Time	(20 to 80%)	$t_{15–}$	15			12	15	8	1, 16
Set Input		$t_{11–15+}$	15			11	15	8	1, 16
Reset Input		$t_{9–15+}$	15			9	15	8	1, 16
Counting Frequency		f_{count}	15			12	15	8	1, 16

* Individually test each input applying V_{IL} to input under test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.