International
IOR Rectifier

PRELIMINARY

Data Sheet No. PD60264 revA

IRS2133D/IRS2135D(J&S)PbF

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V /12 V to 20 V DC and up to 25 V for transient
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Three Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5 V logic compatible
- Outputs out of phase with inputs
- All parts are LEAD-FREE
- Integrated bootstrap diode function

Product Summary

V_{OFFSET}	600 V max.
I_O+/- (min.)	200 mA / 420 mA
V_{OUT}	10 V – 20 V or 12 – 20 V
$t_{on/off}$ (typ.)	500 ns
Deadtime (typ.)	230 ns

Applications:

*Motor Control
*Air Conditioners/ Washing Machines
*General Purpose Inverters
*Micro/Mini Inverter Drives

Packages

28-Lead SOIC

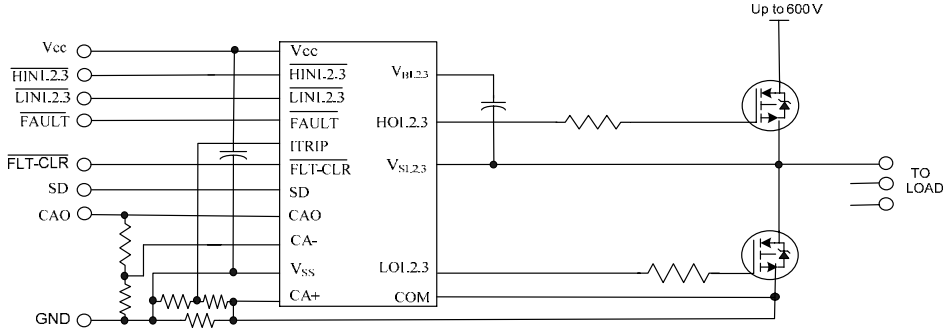
28-Lead PDIP

44-Lead PLCC w/o 12 Leads

Description

The IRS213(3, 5)D are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5 V logic. An independent operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the $\overline{\text{FLT-CLR}}$ lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequencies applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Zener clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20V), and V_{Bx} & V_{Sx} (20 V).

Symbol	Definition		Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage		-0.3	625	V
$V_{S1,2,3}$	High side floating offset voltage		$V_{B1,2,3}$ - 20	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Fixed supply voltage		-0.3	25	
V_{SS}	Logic ground		V_{CC} - 20	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$ ITRIP, SD & $\overline{FLT\text{-}CLR}$)		V_{SS} -0.3	V_{CC} + 0.3	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)		V_{SS} -0.3	V_{CC} +0.3	
$V_{OUT,AMP}$	Op amp output voltage (CAO)		V_{SS} -0.3	V_{CC} +0.3	
V_{FLT}	$\overline{FAULT}$ output voltage		V_{SS} -0.3	V_{CC} +0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
$R_{th,JA}$	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to COM. The V_S offset rating is tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ +10/12	$V_{S1,2,3}$ +20	V
$V_{S1,2,3}$	High side floating offset voltage	Note 1	600	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Fixed supply voltage	10 or 12	20	
V_{SS}	Low side driver return	-5	5	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$ ITRIP, SD & $\overline{FLT\text{-}CLR}$)	V_{SS}	V_{SS} + 5	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS}	V_{SS} + 5	
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	

Note 1: Logic operational for V_S of (COM - 8 V) to (COM + 600 V). Logic state held for V_S of (COM - 8 V) to (COM – V_{BS}). (Please refer to the Design Tip DT97-3 for more details).
Note 2: The CAO pin and all input pins (except CA+ & CA-) are internally clamped with a 5.2 V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, unless otherwise specified and T_A = 25 °C. All static parameters other than I_O and V_O are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" input voltage (OUT = LO)		2.2	—	—	V	
V_{IL}	Logic "1" input voltage (OUT = HI)		—	—	0.8		
$V_{FCLR,IH}$	Logic "0" fault clear input voltage		2.2	—	—		
$V_{FCLR,IL}$	Logic "1" fault clear input voltage		—	—	0.8		
$V_{SD,TH+}$	SD input positive going threshold		1.6	1.9	2.2		
$V_{SD,TH-}$	SD input negative going threshold		1.4	1.7	2.0		
$V_{IT,TH+}$	ITRIP input positive going threshold		470	570	670	mV	
$V_{IT,TH-}$	ITRIP input negative going threshold		360	460	560		
V_{OH}	High level output voltage, V_{BIAS} - V_O		—	—	1	V	V_{IN} = 0 V, I_O = 20 mA
V_{OL}	Low level output voltage, V_O		—	—	400	mV	V_{IN} = 5 V, I_O = 20 mA
I_{LK}	Offset supply leakage current IRS213(3,5)D		—	—	50	µA	$V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V
I_{QBS}	Quiescent V_{BS} supply current		—	45	70		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current		—	4	6	mA	V_{IN} = 0 V or 5 V
I_{IN+}	Logic "1" input bias current (OUT = HI)		—	150	200	µA	V_{IN} = 0 V
I_{IN-}	Logic "0" input bias current (OUT = LO)		—	110	150		V_{IN} = 5 V
I_{SD+}	"High" shutdown bias current		—	5	10		SD = 5 V
I_{SD-}	"Low" shutdown bias current		—	—	100	nA	SD = 0 V
I_{ITRIP+}	"High" ITRIP bias current		—	5	10	µA	ITRIP = 5 V
I_{ITRIP-}	"Low" ITRIP bias current		—	—	100	nA	ITRIP = 0 V
$I_{FLTCLR+}$	"High" fault clear input bias current		—	150	200	µA	$\overline{\text{FLT-CLR}}$ = 0 V
$I_{FLTCLR-}$	"Low" fault clear Input bias current		—	110	150		$\overline{\text{FLT-CLR}}$ = 5 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	IRS2133D	7.6	8.6	9.6	V	
		IRS2135D	9.2	10.4	11.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	IRS2133D	7.2	8.2	9.2		
		IRS2135D	8.3	9.4	10.5		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	IRS2133D	—	0.4	—		
		IRS2135D	—	1	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	IRS2133D	7.6	8.6	9.6		
		IRS2135D	9.2	10.4	11.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	IRS2133D	7.2	8.2	9.2		
		IRS2135D	8.3	9.4	10.5		
V_{CCUVH}	V_{CC} supply undervoltage lockout hysteresis	IRS2133D	—	0.4	—		
		IRS2135D	—	1	—		
$R_{on,\ FLT}$	$\overline{\text{FAULT}}$ low on-resistance		—	55	75	Ω	
I_{O+}	Output high short circuit pulsed current		200	250	—	mA	V_{OUT} = 0 V, V_{IN} = 0 V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		420	500	—		V_{OUT} = 15 V, V_{IN} = 5 V PW ≤ 10 µs

Static Electrical Characteristics – (Continued)

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, unless otherwise specified and T_A = 25 °C. All static parameters other than I_O and V_O are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
R_{BS}	Integrated bootstrap diode resistance	—	200	—	Ω	
V_{OS}	Amplifier input offset voltage	—	—	10	mV	CA+ = 0.2 V, CA- = CAO
$I_{IN,AMP}$	Amplifier input bias current	—	—	50	nA	CA+ = CA- = 2.5 V
CMRR	Amplifier common mode rejection ratio	TBD	80	—	dB	CA+ = 0.1 V & 5 V, CA- = CAO
PSRR	Amplifier power supply rejection ratio	TBD	75	—		CA+ = 0.2 V, CA- = CAO, V_{CC} = 10 V & 20 V
$V_{OH,AMP}$	Operational amplifier high level output voltage	4.9	5.2	5.4	V	CA+ = 1 V, CA- = 0 V
$V_{OL,AMP}$	Operational amplifier low level output voltage	—	—	30	mV	CA+ = 0 V, CA- = 1 V
$I_{SRC,AMP}$	Operational amplifier output source current	4	7	—	mA	CA+ = 1 V, CA- = 0 V, CAO = 4 V
$I_{SNK,AMP}$	Operational amplifier output sink current	1	2.1	—		CA+ = 0 V, CA- = 1 V, CAO = 2 V
$I_{O+,AMP}$	Operational amplifier output high short circuit current	—	10	—		CA+ = 5 V, CA- = 0 V, CAO = 0 V
$I_{O-,AMP}$	Operational amplifier output low short circuit current	—	4	—		CA+ = 0 V, CA- = 5 V, CAO = 5 V

Note 1: Please refer to Feature Description section for integrated bootstrap functionality information.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{S1,2,3}$ = V_{SS} , T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	500	700	ns	V_{IN} = 0 V & 5 V, $V_{S1,2,3}$ = 0 V to 600 V
t_{off}	Turn-off propagation delay	400	500	700		
t_r	Turn-on rise time	—	80	125		
t_f	Turn-off fall time	—	35	55		
t_{sd}	SD to output shutdown propagation delay	400	550	750		
t_{itrip}	ITRIP to output shutdown propagation delay	400	660	920		
t_{bl}	ITRIP blanking time	—	400	—		
t_{flt}	ITRIP to $\overline{\text{FAULT}}$ propagation delay	350	550	870		
$t_{flt,\ in}$	Input filter time ($\overline{\text{HIN}}$, $\overline{\text{LIN}}$, and SD)	—	325	—		
t_{fltclr}	$\overline{\text{FLT-CLR}}$ to $\overline{\text{FAULT}}$ clear time	600	850	1100		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	150	230	350		
SR+	Operational amplifier slew rate (+)	5	10	—	V/µs	1 V step input
SR-	Operational amplifier slew rate (-)	2.4	3.2	—		

NOTE 2: For high side PWM, HIN pulse width must be $\geq$ 1 µs.

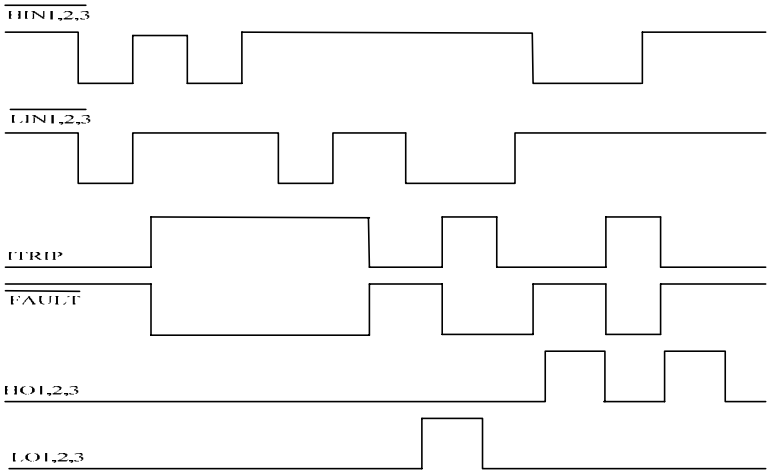


Fig. 1. Input/Output Timing Diagram

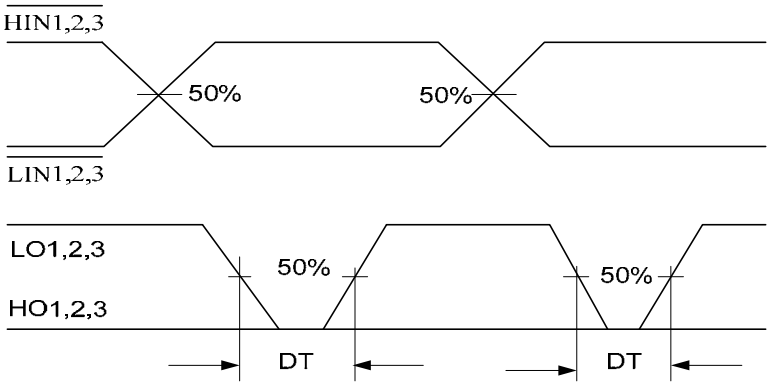


Fig. 2. Deadtime Waveform Definitions

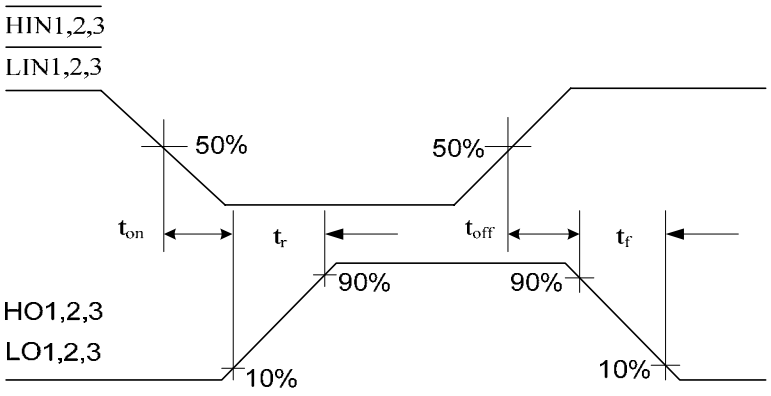


Fig. 3. Input/Output Switching Time Waveform Definitions

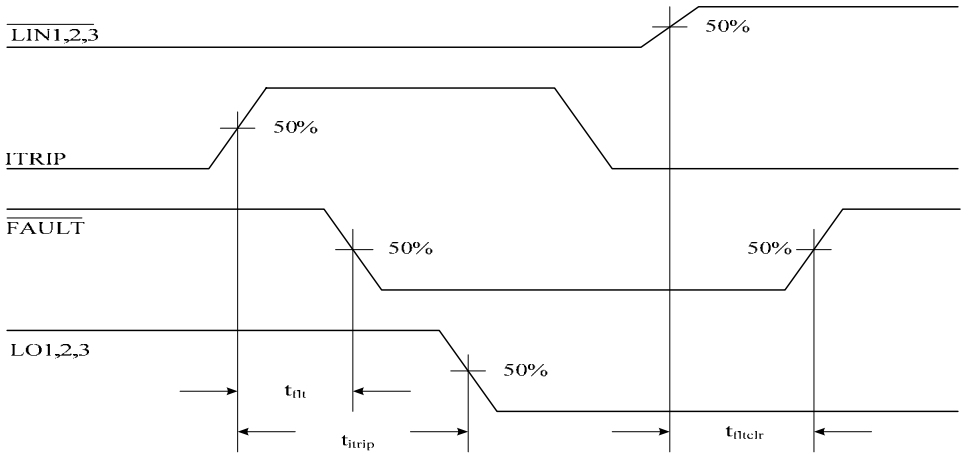


Fig. 4. Overcurrent Shutdown Switching Time Waveform Definitions

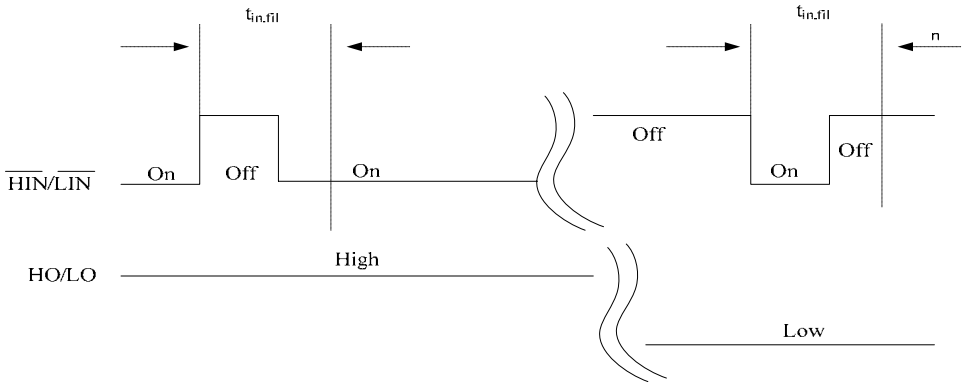


Fig. 5. Input Filter Function

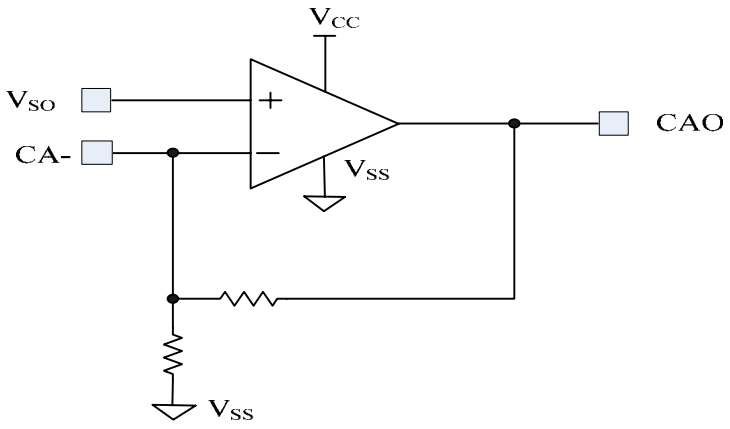
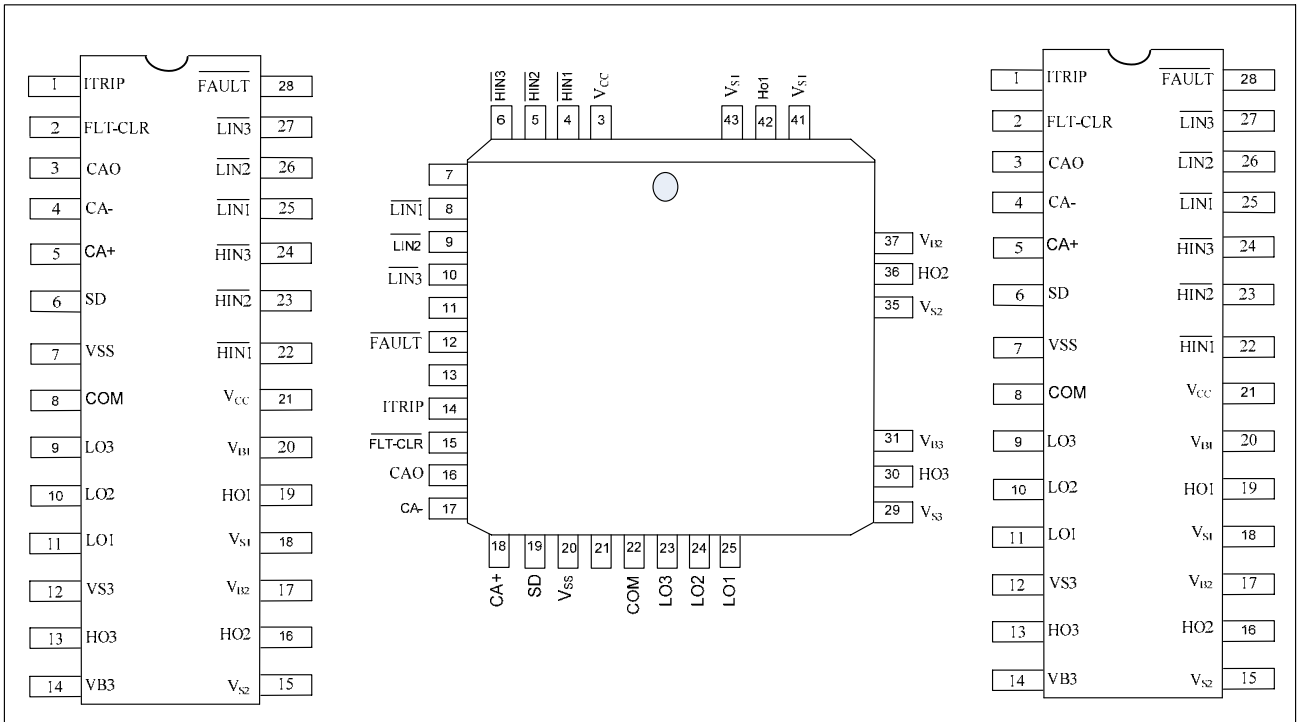


Fig. 6. Diagnostic Feedback Operational Amplifier Circuit

Lead Definitions

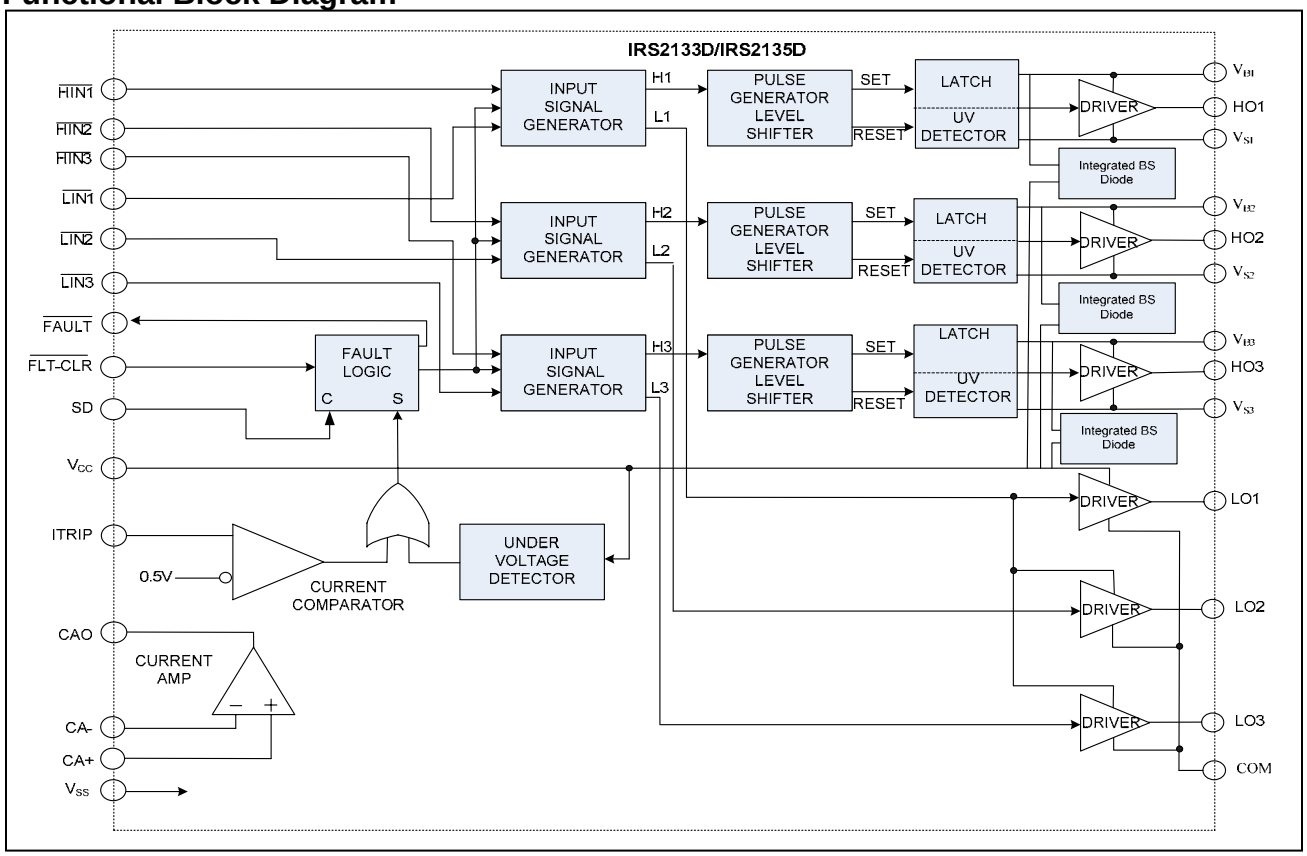
Symbol	Description
$\overline{HIN1,2,3}$	Logic input for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic input for low side gate driver outputs (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Logic and low side fixed supply
ITRIP	Input for over-current shut down
$\overline{FLT\text{-}CLR}$	Logic input for fault clear, negative logic
SD	Logic input for shut down
CAO	Output of current amplifier
CA-	Negative input of current amplifier
CA+	Positive input of current amplifier
V_{SS}	Logic ground
Com	Low side return
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs

Lead Assignments



28 Lead PDIP	44 Lead PLCC w/o 12 Leads	28 Lead SOIC (Wide Body)
IRS213(3,5)D	IRS213(3,5)DJ	IRS213(3,5)DS
	Part Number	

Functional Block Diagram



1 Features Description

1.1 Integrated Bootstrap Functionality

The IRS213(3,5)D family embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.

There is one bootstrap FET for each channel and it is connected between each of the floating supply (V_{B1}, V_{B2}, V_{B3}) and V_{CC} (see Fig. 7).

The bootstrap FET of each channel follows the state of the respective low side output stage (i.e., bootFet is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 1.1(V_{CC}). In that case the bootstrap FET stays off until the V_B voltage returns below that threshold (see Fig. 8).

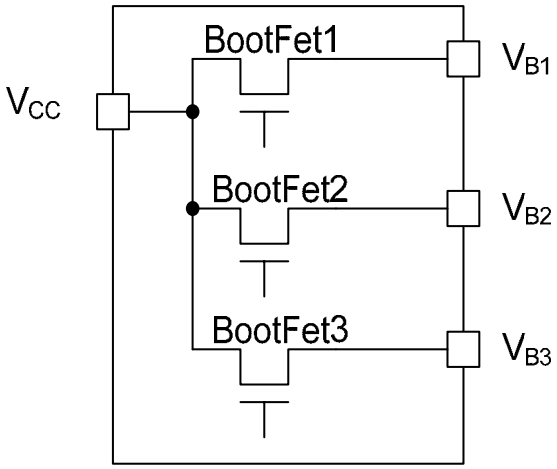


Fig. 7. Simplified BootFet Connection

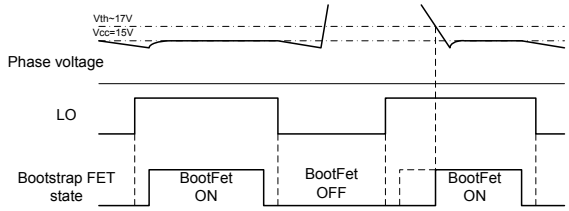


Fig. 8. State Diagram

The bootstrap FET is suitable for most PWM modulation schemes and can be used either in parallel with the external bootstrap network (diode+resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- when used in non-complementary PWM schemes (typically 6-step modulations)
- at a very high PWM duty cycle due to the bootstrap FET equivalent resistance (R_{BS}, see page 4).

In these cases, better performances can be achieved by using the IRS213(3,5) non D version with an external bootstrap network.

2 PCB Layout Tips

2.1 Distance from H to L Voltage

The IRS213(3,5)J package lacks some pins (see page 6) in order to maximizing the distance between the high voltage and low voltage pins. It's strongly recommended to place the components tied to the floating voltage in the respective high voltage portions of the device ($V_{B1,2,3}$, $V_{S1,2,3}$) side.

2.2 Ground Plane

To minimize noise coupling the ground plane must not be placed under or near the high voltage floating side.

2.3 Gate Drive Loops

Current loops behave like an antenna, which are able to receive and transmit EM noise (see Fig. 9). In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect.

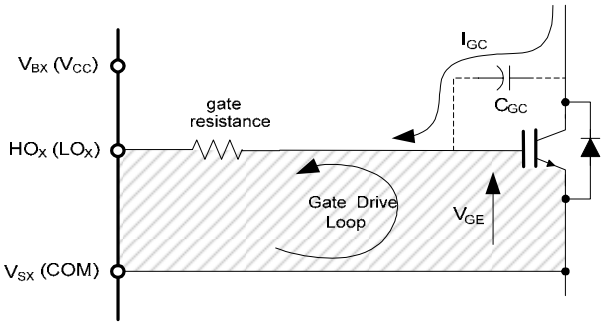


Fig. 9. Antenna Loops

2.4 Supply Capacitors

Supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/resistance.

2.5 Routing and Placement

Power stage PCB parasitic may generate dangerous voltage transients for the gate driver and the control logic. In particular it's recommended to limit phase voltage negative transients.

In order to avoid such undervoltage it is highly recommended to minimize high side emitter to low side collector distance and low side emitter to negative bus rail stray inductance. See DT04-4 at www.irf.com for more detailed information.

Figures 10-40 provide information on the experimental performance of the IRS2133DS HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

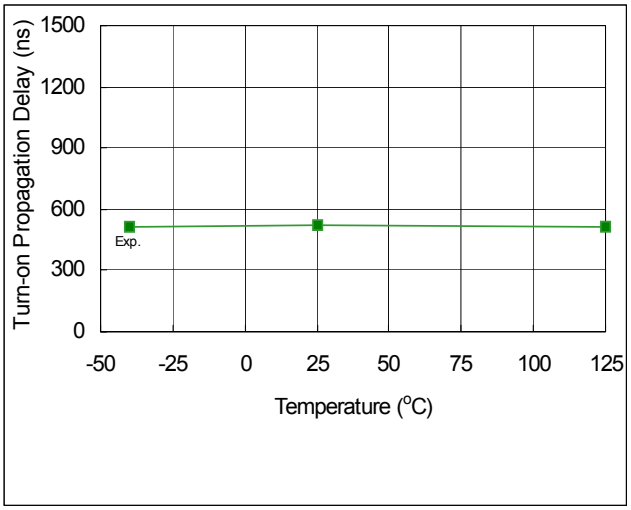


Fig. 10. Turn-On Propagation Delay vs. Temperature

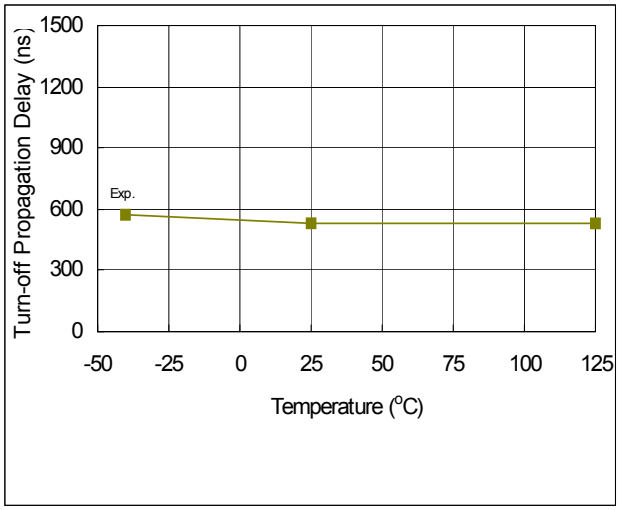


Fig. 11. Turn-Off Propagation Delay vs. Temperature

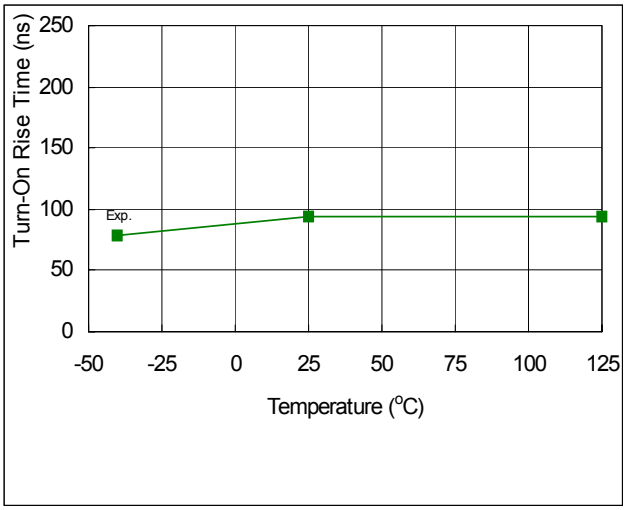


Fig. 12. Turn-On Rise Time vs. Temperature

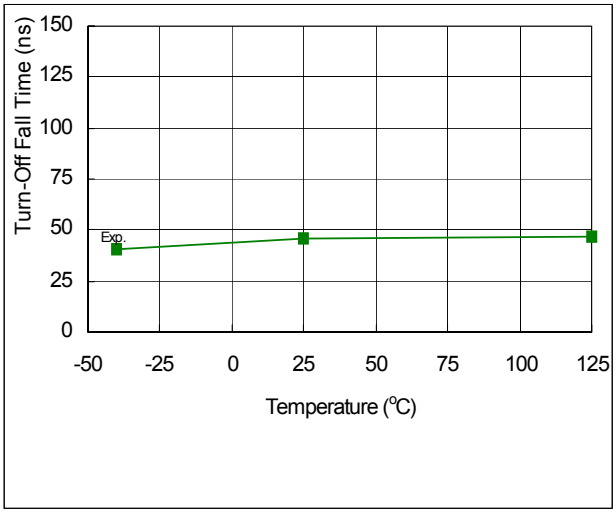


Fig. 13. Turn-Off Fall Time vs. Temperature

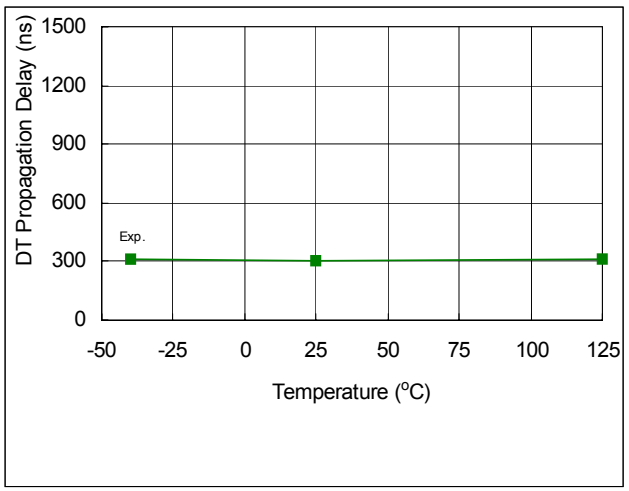


Fig. 14. DT Propagation Delay vs. Temperature

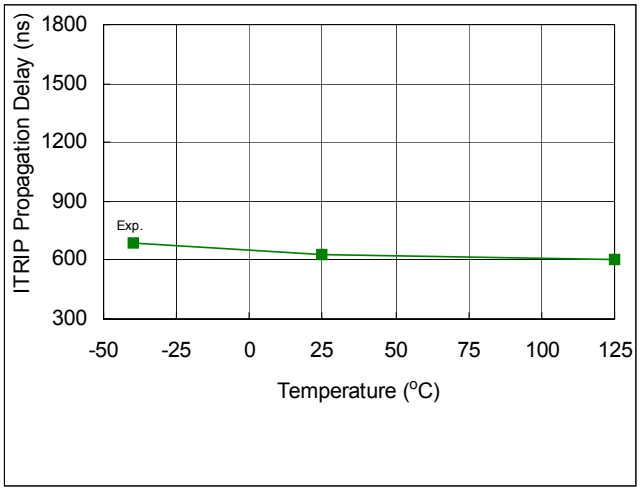


Fig. 15. T_{ITRIP} Propagation Delay vs. Temperature

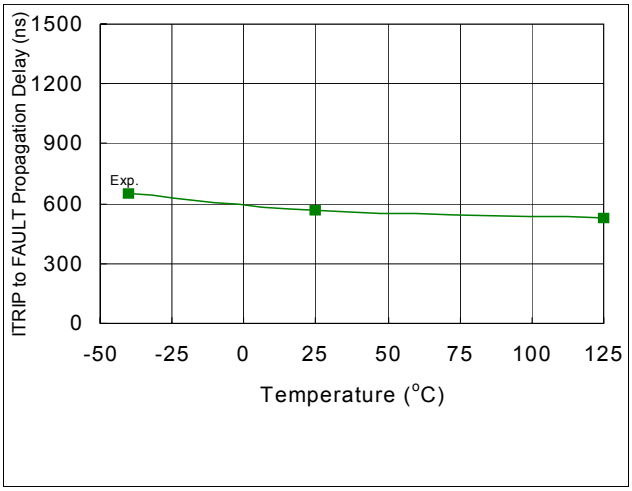


Fig. 16. ITRIP to $\overline{FAULT}$ Propagation Delay vs. Temperature

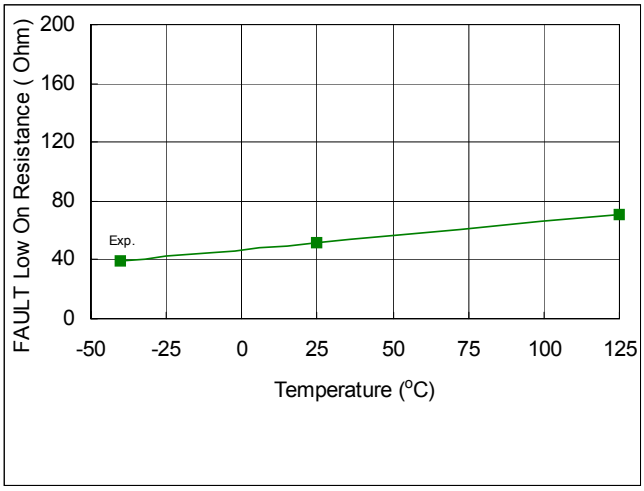


Fig. 17. $\overline{FAULT}$ Low On Resistance vs. Temperature

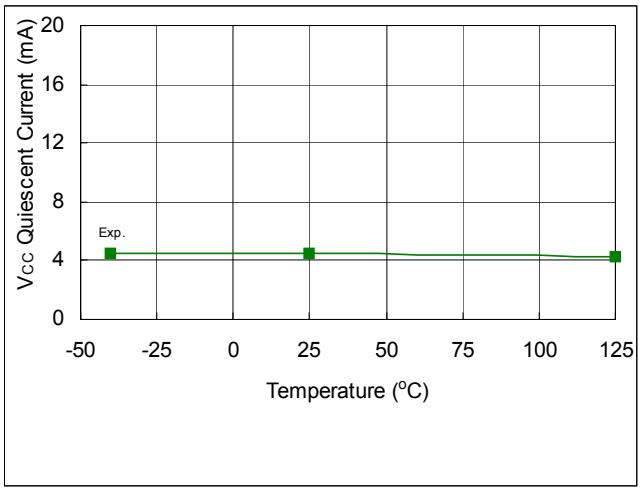


Fig. 18. V_{CC} Quiescent Current vs. Temperature

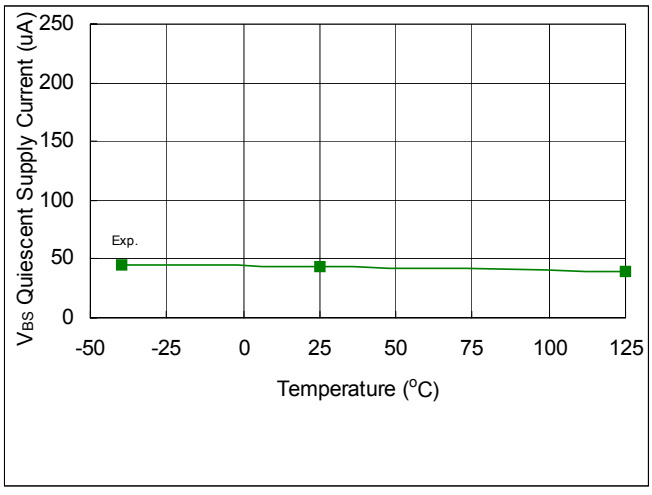


Fig. 19. V_{BS} Quiescent Current vs. Temperature

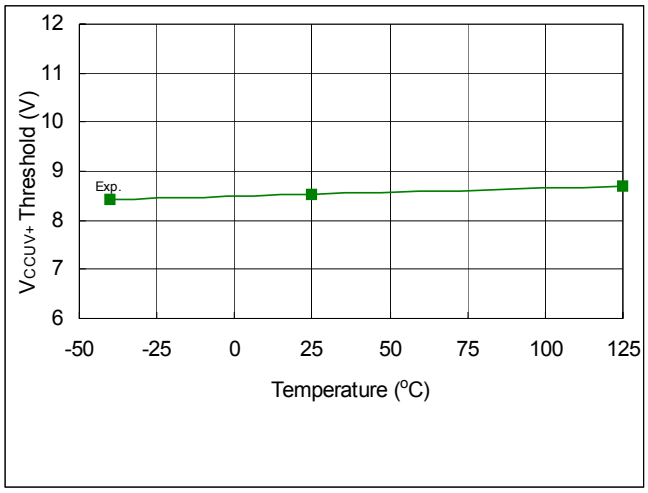


Fig. 20. V_{CCUV+} Threshold vs. Temperature

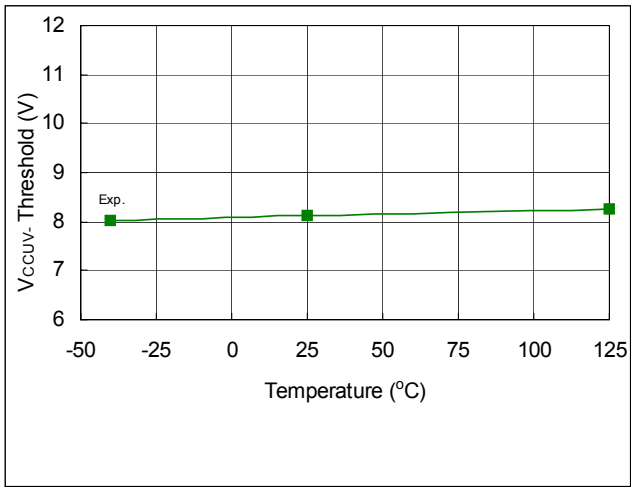


Fig. 21. V_{CCUV-} Threshold vs. Temperature

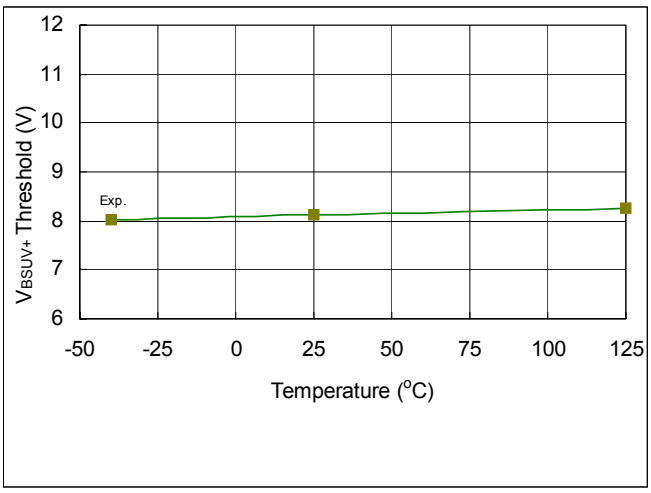


Fig. 22. V_{BSUV+} Threshold vs. Temperature

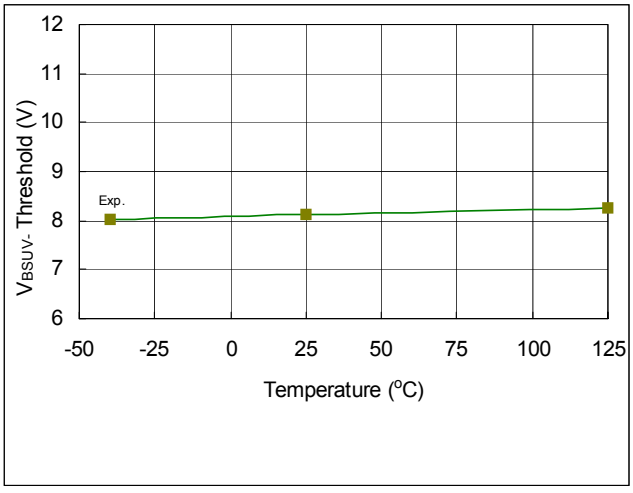


Fig. 23. V_{BSUV-} Threshold vs. Temperature

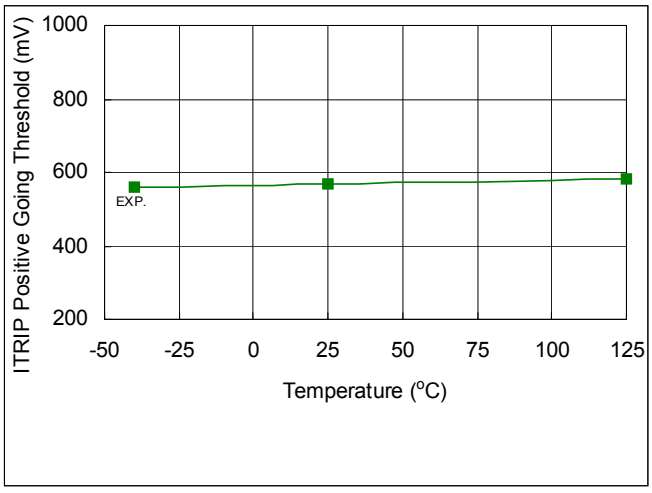


Fig. 24. ITRIP Positive Going Threshold vs. Temperature

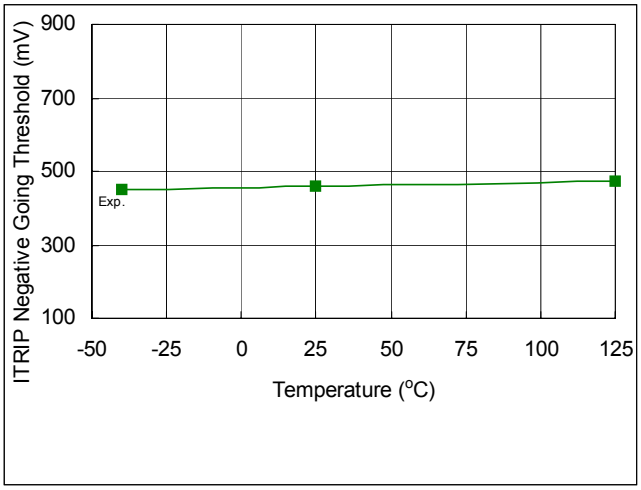


Fig. 25. ITRIP Negative Going Threshold vs. Temperature

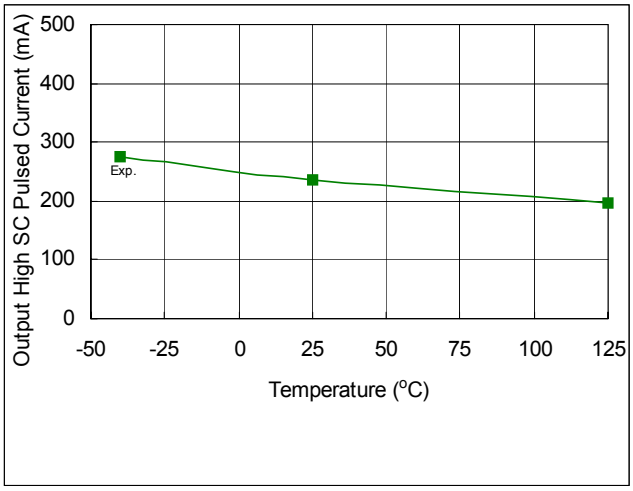


Fig. 26. Output High SC Pulsed Current vs. Temperature

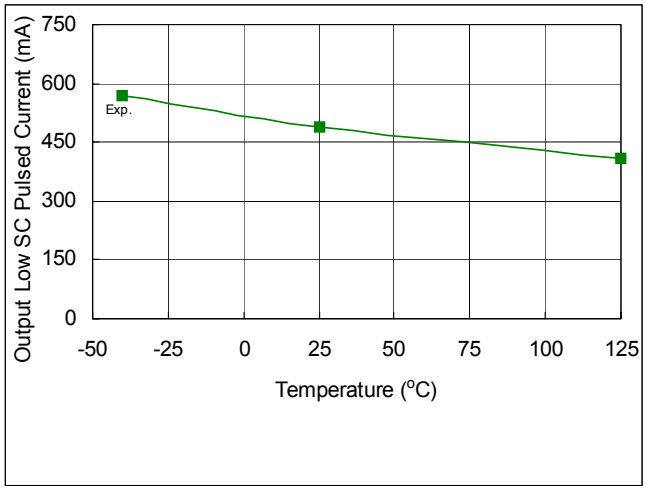


Fig. 27. Output Low SC Pulsed Current vs. Temperature

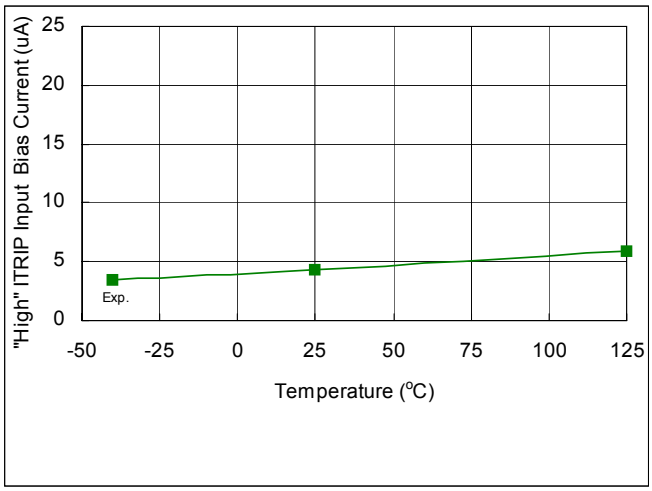


Fig. 28. "High" ITRIP Bias Current vs. Temperature

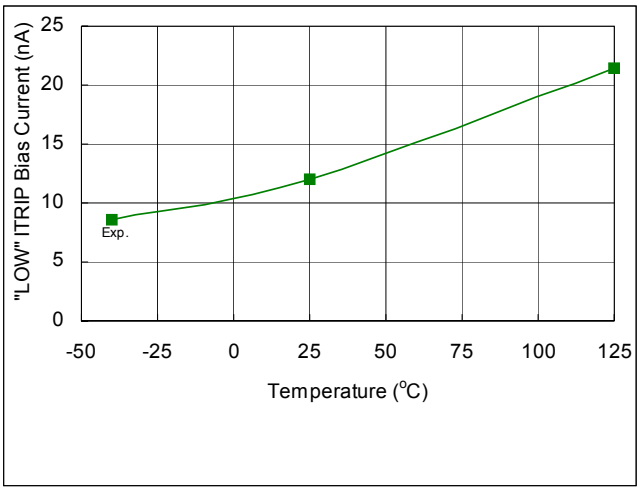


Fig. 29. "Low" ITRIP Bias Current vs. Temperature

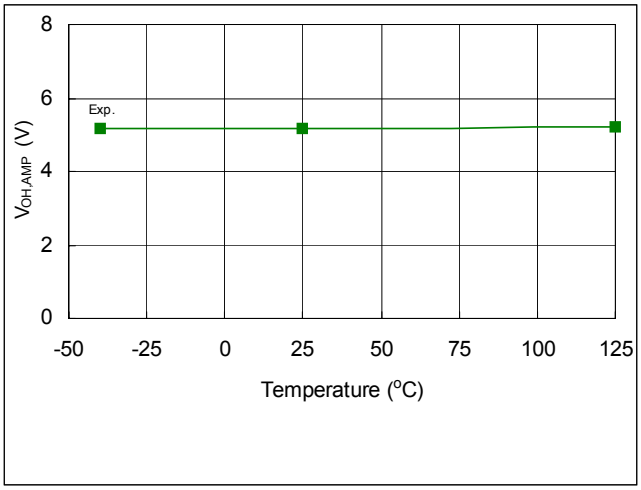


Fig. 30. $V_{OH,AMP}$ vs. Temperature

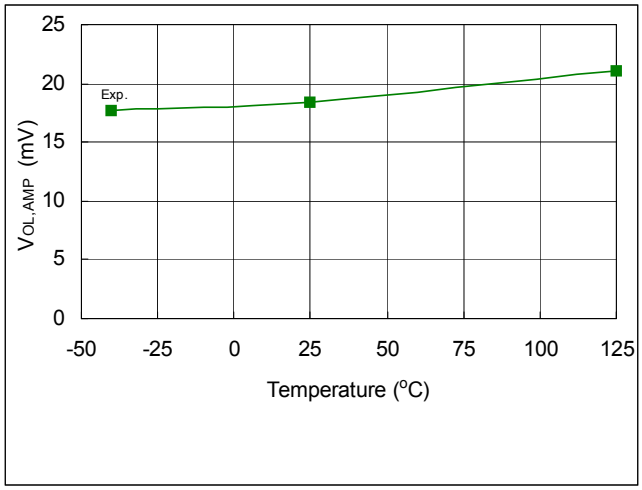


Fig. 31. $V_{OL,AMP}$ vs. Temperature

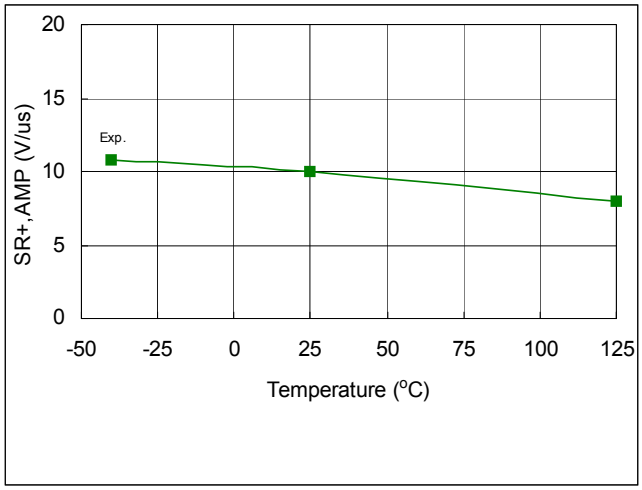


Fig. 32. SR+,AMP vs. Temperature

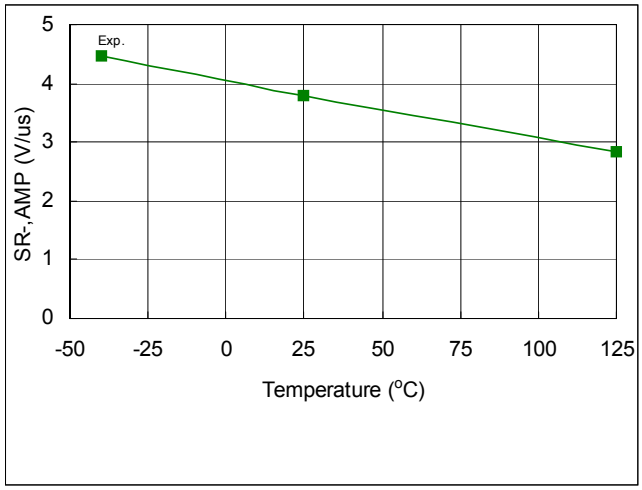


Fig. 33. SR-,AMP vs. Temperature

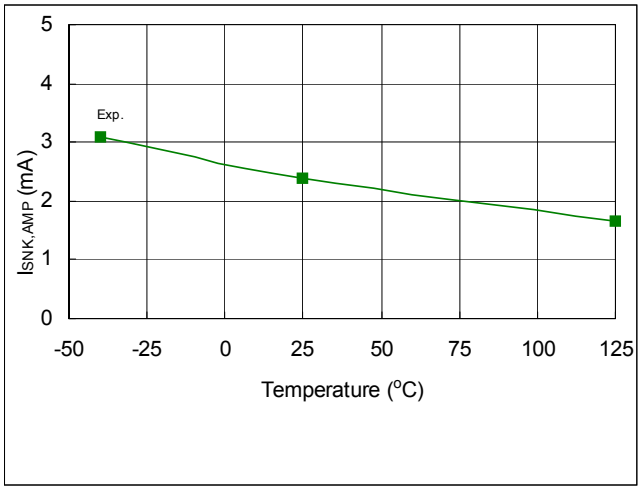


Fig. 34. $I_{SNK,AMP}$ vs. Temperature

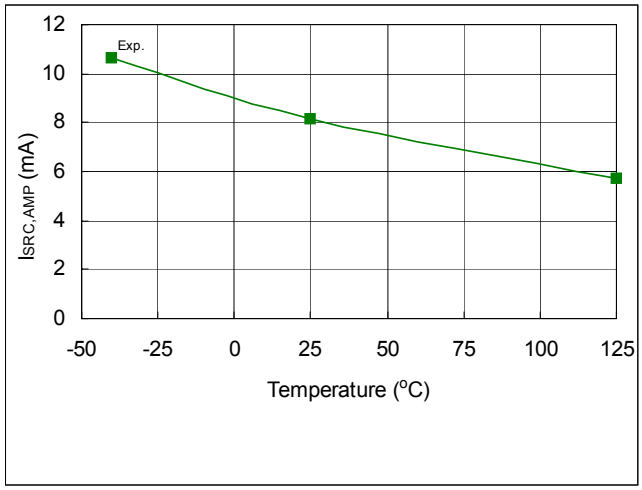


Fig. 35. $I_{SRC,AMP}$ vs. Temperature

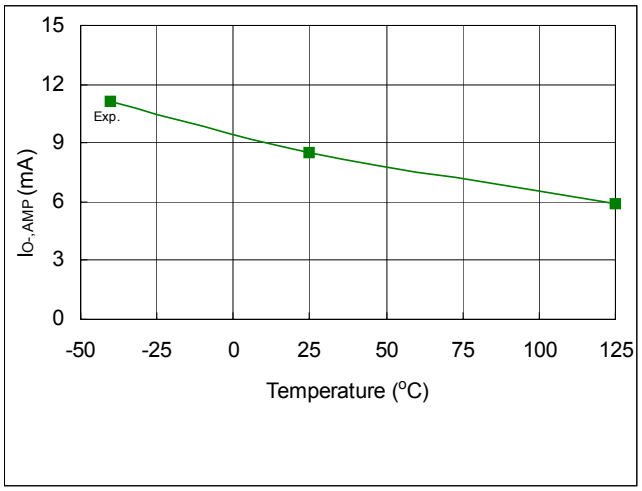


Fig. 36. $I_{O-,AMP}$ vs. Temperature

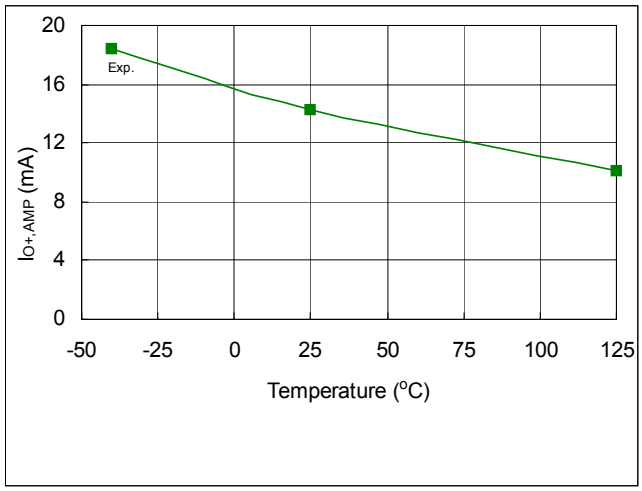


Fig. 37. $I_{O+,AMP}$ vs. Temperature

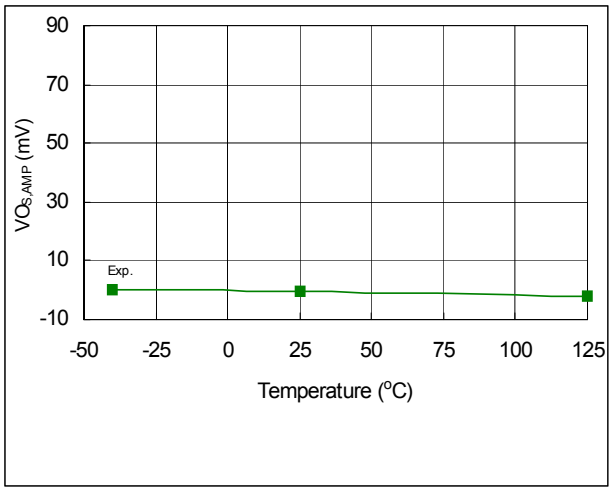


Fig. 38. $V_{OS,AMP}$ vs. Temperature

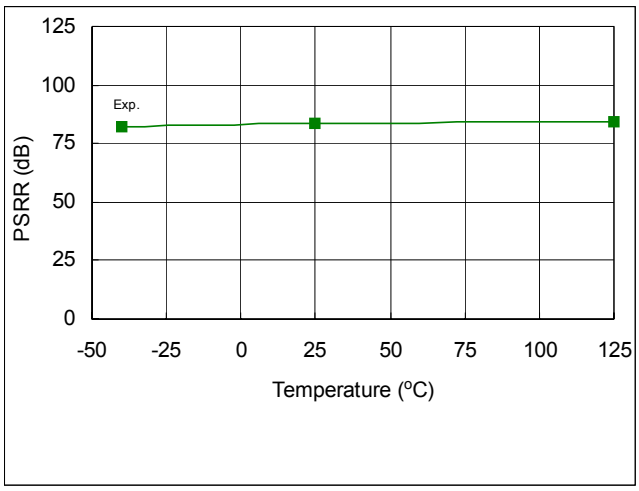


Fig. 39. PSRR vs. Temperature

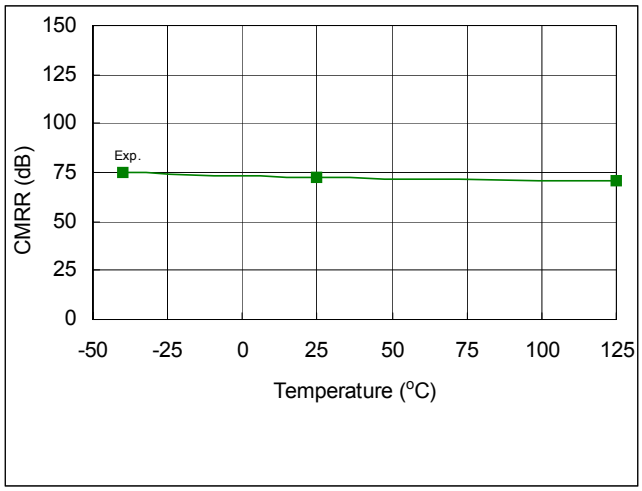
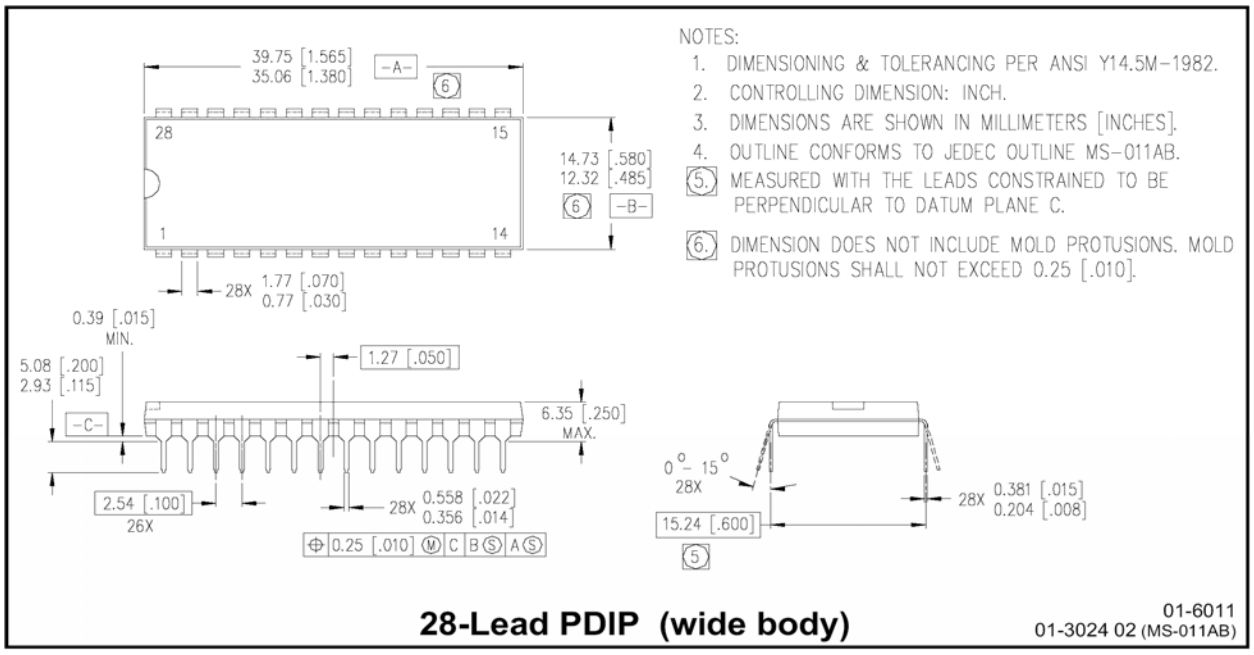
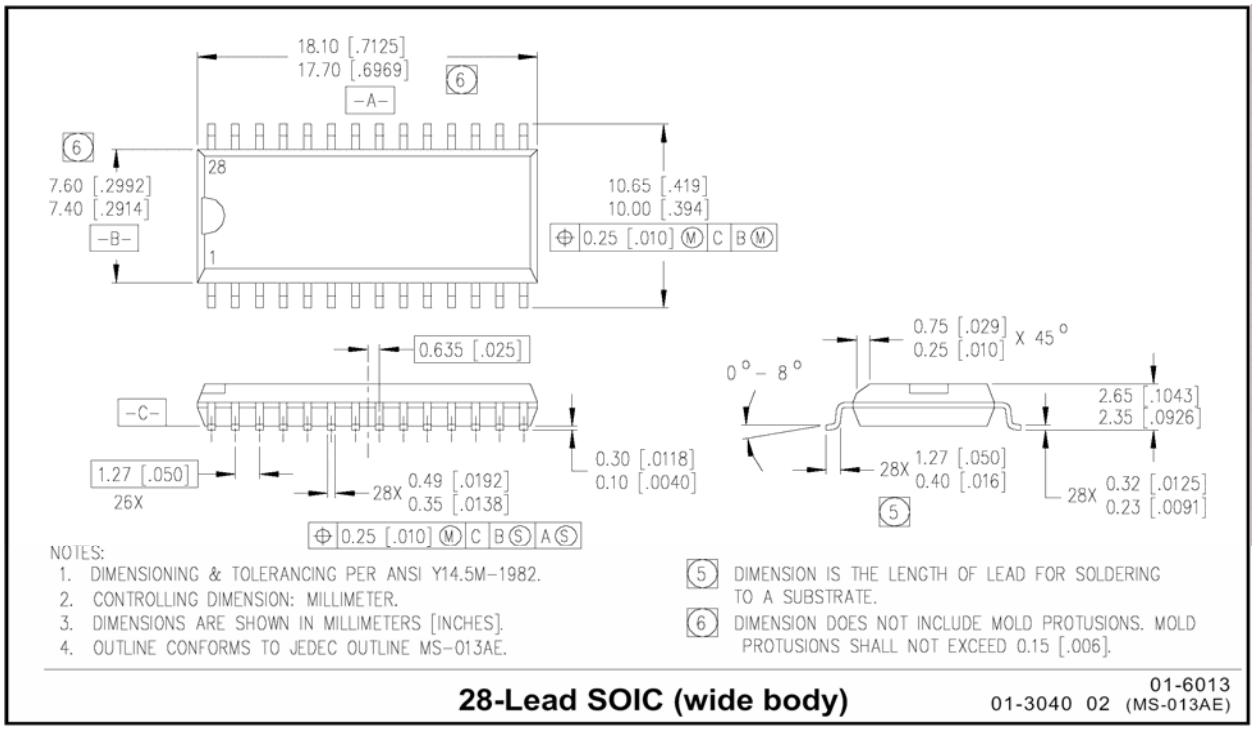


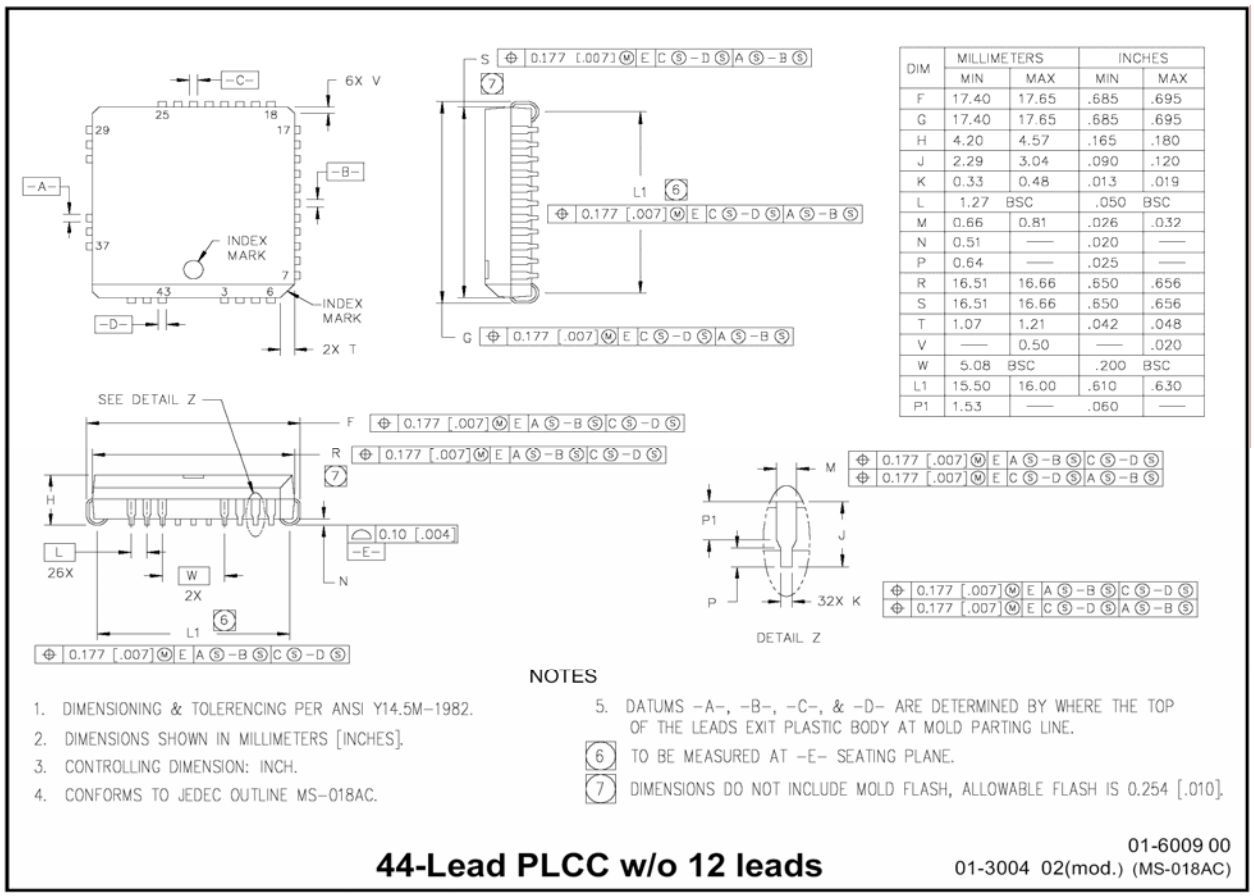
Fig. 40. CMRR vs. Temperature

Case Outlines





Case Outlines



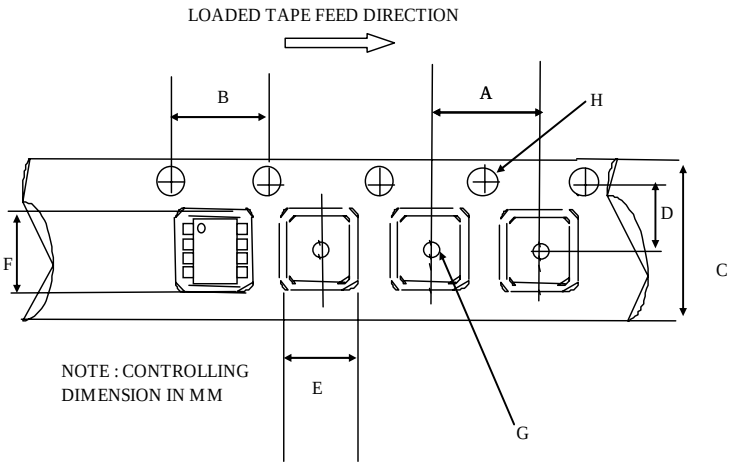
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

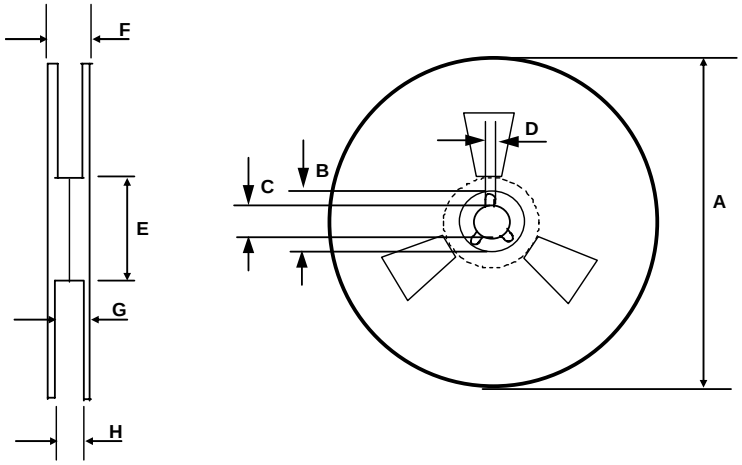
44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)



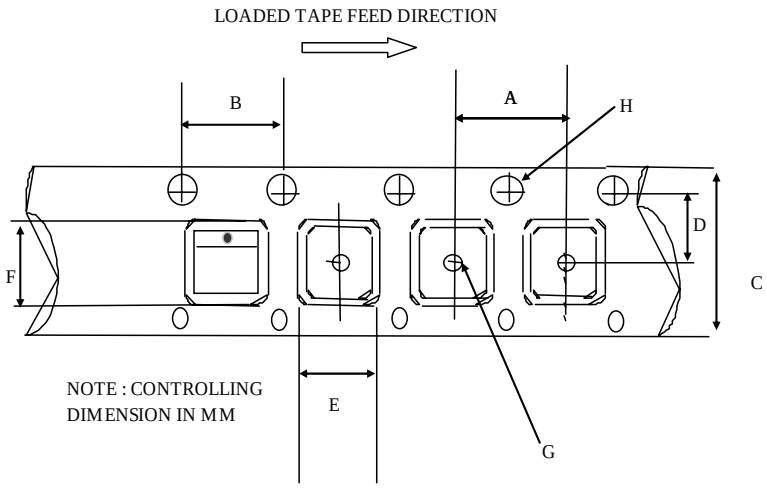
CARRIER TAPE DIMENSION FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



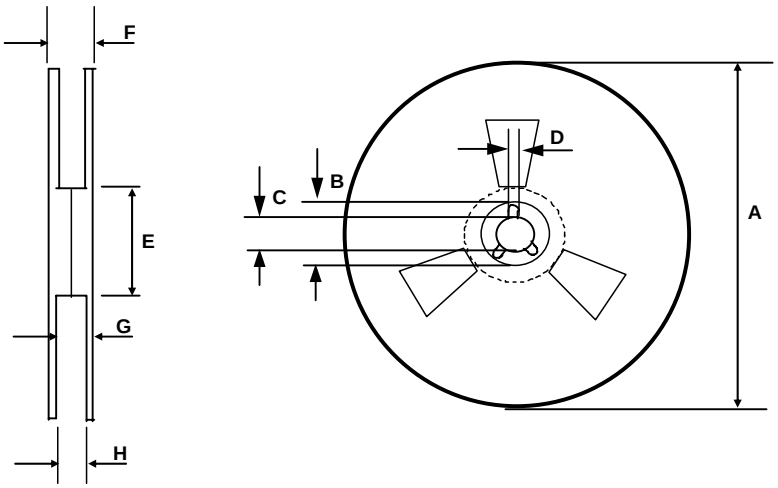
REEL DIMENSIONS FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039



CARRIER TAPE DIMENSION FOR 44PLCC

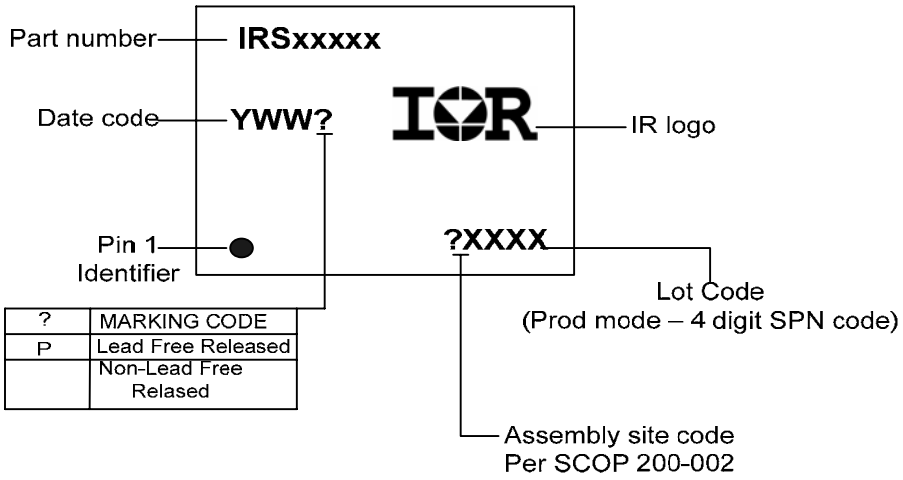
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

28-Lead PDIP IRS2133DPbF
28-Lead PDIP IRS2135DPbF
28-Lead SOIC IRS2133DSPbF
28-Lead SOIC IRS2135DSPbF
44-Lead PLCC IRS2133DJPbF
44-Lead PLCC IRS2135DJPbF

28-Lead SOIC Tape & Reel IRS2133DSTRPbF
28-Lead SOIC Tape & Reel IRS2135DSTRPbF
44-Lead PLCC Tape & Reel IRS2133DJTRPbF
44-Lead PLCC Tape & Reel IRS2135DJTRPbF