Signetics

Military Logic Products

# 54F148
## Encoder

**8-Input Priority Encoder**

***Product Specification***

### FEATURES

- **Code conversions**
- **Multi-channel D/A converter**
- **Decimal-to-BCD converter**
- **Cascading for priority encoding of "N" bits**
- **Input enable capability**
- **Priority encoding — automatic selection of highest priority-input line**
- **Output enable — active Low when all inputs High**
- **Group signal output — active when any input is Low**

### DESCRIPTION

The 54F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority.

A High on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs.

### ORDERING INFORMATION

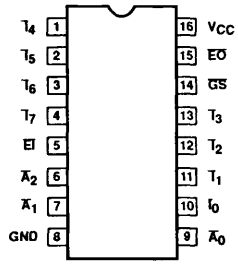
| DESCRIPTION | ORDER CODE |
|---|---|
| 16-Pin Ceramic DIP | 54F148/BEA |
| 16-Pin Ceramic FlatPack | 54F148/BFA |
| 20-Pin Ceramic LLCC | 54F148/B2A |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 54F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $\overline{I}_0$ - $\overline{I}_7$ | Priority inputs (active Low) | 1.0/1.0 | 20μA/1.2mA |
| $\overline{I}_0$ | Priority input (active Low) | 1.0/2.0 | 20μA/0.6mA |
| $\overline{EI}$ | Enable input (active Low) | 1.0/2.0 | 20μA/1.2mA |
| $\overline{EO}$ | Enable output (active Low) | 50/33 | 1.0mA/20mA |
| $\overline{GS}$ | Group select output (active Low) | 50/33 | 1.0mA/20mA |
| $\overline{A}_0$ - $\overline{A}_2$ | Address outputs (active Low) | 50/33 | 1.0mA/20mA |

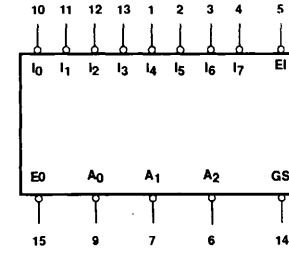
**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

### PIN CONFIGURATION




For LLCC Pin Assignments see JEDEC Standard No. 2

### LOGIC SYMBOL




For LLCC Pin Assignments see JEDEC Standard No. 2

# Encoder

# 54F148

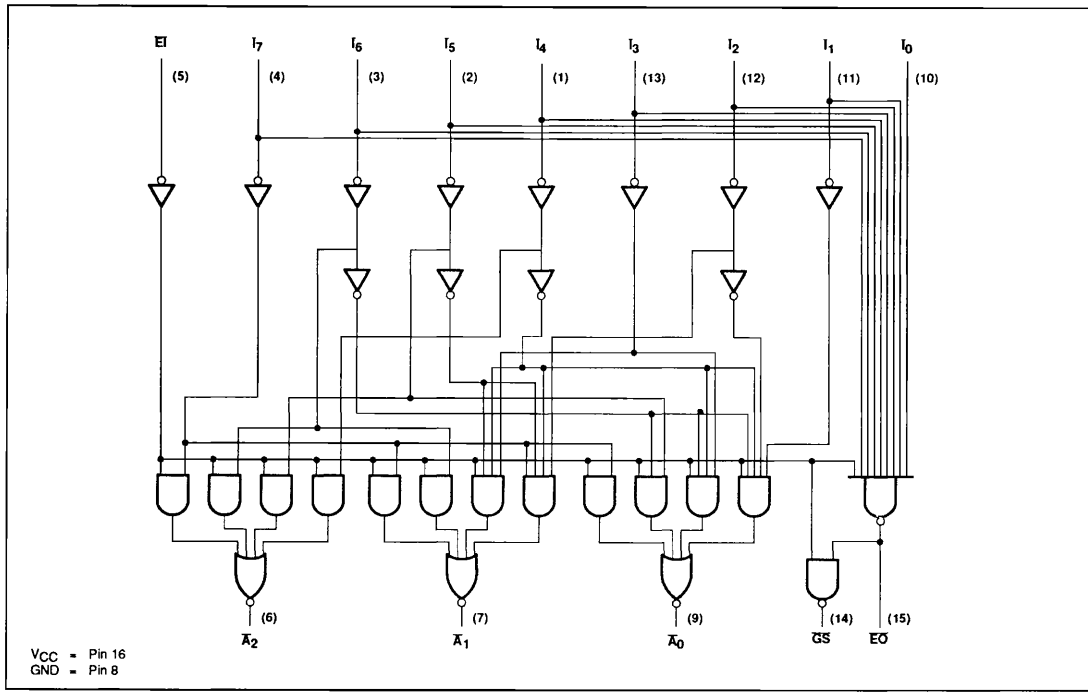
A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low; this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{EI}$ | $\overline{I}_0$ | $\overline{I}_1$ | $\overline{I}_2$ | $\overline{I}_3$ | $\overline{I}_4$ | $\overline{I}_5$ | $\overline{I}_6$ | $\overline{I}_7$ | $\overline{GS}$ | $\overline{A}_0$ | $\overline{A}_1$ | $\overline{A}_2$ | $\overline{EO}$ |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | H | L | L | H |
| L | X | X | X | X | X | L | H | H | L | L | H | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | L | L | L | H | H |
| L | X | X | L | H | H | H | H | H | L | H | L | H | H |
| L | X | L | H | H | H | H | H | H | L | L | H | H | H |
| L | L | H | H | H | H | H | H | H | L | H | H | H | H |

H = High voltage level
L = Low voltage level
X = Don't care

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range | -0.5 to +7.0 | V |
| $V_I$ | Input voltage range | -0.5 to +7.0 | V |
| $I_I$ | Input current range | -30 to +5 | mA |
| $V_O$ | Voltage applied to output in High output state range | -0.5 to +$V_{CC}$ | V |
| $I_O$ | Current applied to output in Low output state | 40 | mA |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | -18 | mA |
| $I_{OH}$ | High-level output current | | | -1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature range | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS[1] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = Min, $V_{IL}$ = Max, $I_{OH}$ = Max, $V_{IH}$ = Min | 2.5 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = Min, $V_{IL}$ = Max, $I_{OL}$ = Max, $V_{IH}$ = Min | | 0.35 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = Min, $I_I$ = $I_{IK}$ | | -0.73 | -1.2 | V |
| $I_{IH2}$ | Input current at maximum input voltage | | $V_{CC}$ = Max, $V_I$ = 7.0V | | 5 | 100 | µA |
| $I_{IH1}$ | High-level input current | | $V_{CC}$ = Max, $V_I$ = 2.7V | | 1 | 20 | µA |
| $I_{IL}$ | Low-level input current | $\overline{I_0}$, $\overline{EI}$ | $V_{CC}$ = Max, $V_I$ = 0.5V | | -0.4 | -0.6 | mA |
| | | $\overline{I_1}$ - $\overline{I_7}$ | | | -0.8 | -1.2 | mA |
| $I_{OS}$ | Short-circuit output current[3] | | $V_{CC}$ = Max | -60 | -80 | -150 | mA |
| $I_{CC}$ | Supply current (total) | | $V_{CC}$ = Max | | 23 | 35 | mA |

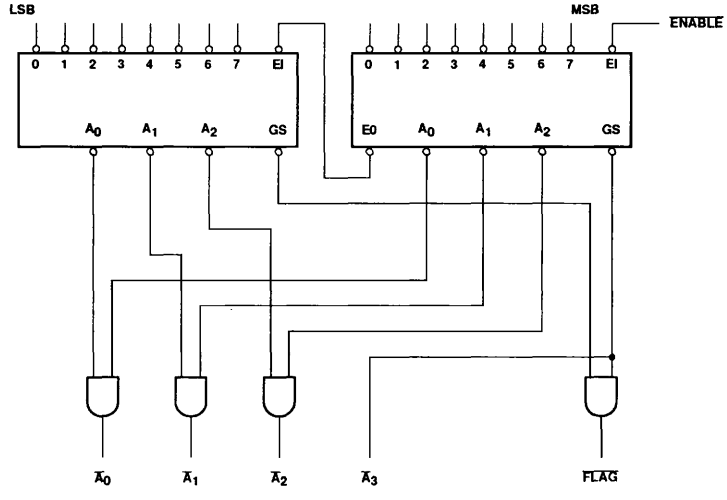
## AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_A$ = -55°C to +125°C, $V_{CC}$ = +5.0V ± 10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Type | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{I_n}$ input to $\overline{A_n}$ | Waveform 2 | 3.5<br>4.0 | 6.0<br>6.0 | 9.0<br>10.5 | 3.5<br>4.0 | 11.0<br>13.0 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{I_n}$ input to $\overline{EO}$ | Waveform 1 | 2.0<br>2.5 | 3.5<br>4.5 | 6.5<br>7.5 | 2.0<br>2.5 | 8.5<br>9.5 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{I_n}$ input to $\overline{GS}$ | Waveform 2 | 2.0<br>2.0 | 4.0<br>6.0 | 9.0<br>8.0 | 2.0<br>2.0 | 11.0<br>10.0 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{EI}$ input to $\overline{A_n}$ | Waveform 2 | 3.5<br>3.0 | 6.0<br>6.5 | 8.5<br>8.0 | 3.5<br>3.0 | 10.5<br>10.0 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{EI}$ input to $\overline{GS}$ | Waveform 2 | 2.5<br>3.0 | 4.5<br>6.5 | 7.0<br>7.5 | 2.5<br>3.0 | 9.0<br>9.5 | ns<br>ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{EI}$ input to $\overline{EO}$ | Waveform 2 | 3.0<br>4.5 | 5.0<br>7.0 | 7.0<br>10.5 | 3.0<br>4.5 | 9.0<br>13.0 | ns<br>ns |

**NOTES:**

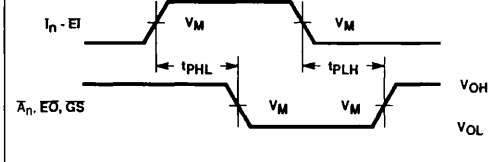
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## APPLICATION

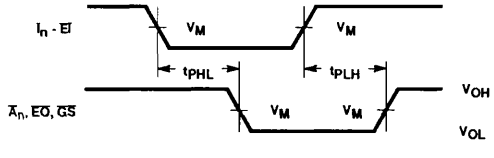



16-Input Priority Encoder

## AC WAVEFORMS



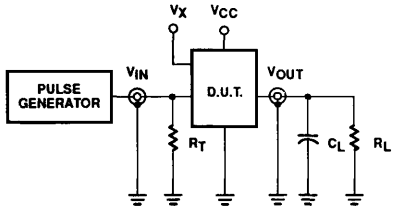

Waveform 1. For Inverting Outputs



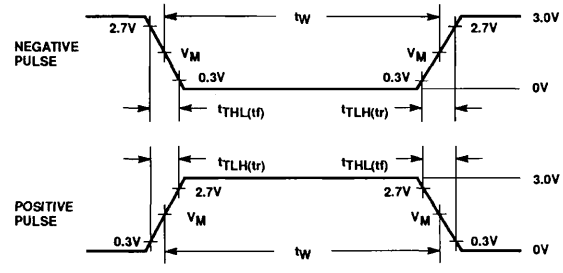

Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, $V_M$ = 1.5V

## TEST CIRCUIT AND WAVEFORM




**Test Circuit for Totem-Pole Outputs**




$V_M$ = 1.5V

**Input Pulse Definition**

**DEFINITIONS:**

$R_L$ = Load Resistor; see AC Characteristics for value.
$C_L$ = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.
$V_X$ = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| **Family** | **Rep. Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 54F | 1MHz | 500ns | ≤2.5ns | ≤2.5ns |