

Variable-Length Shift Register

8-Bit, 18MHz

The TRW TDC1011 is a high-speed, byte-wide shift register which can be programmed to any length between 3 and 18 stages. It operates at a 56ns cycle time (18MHz shift rate). A special split-word mode is provided for use with the TRW TDC1028.

The TDC1011 is fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge-triggered D-type flip-flops. The length control inputs are also registered.

Built with TRW's OMICRON-B[™] 1-micron bipolar process, the TDC1011 provides the system designer with a unique variable-delay capability at video speeds.

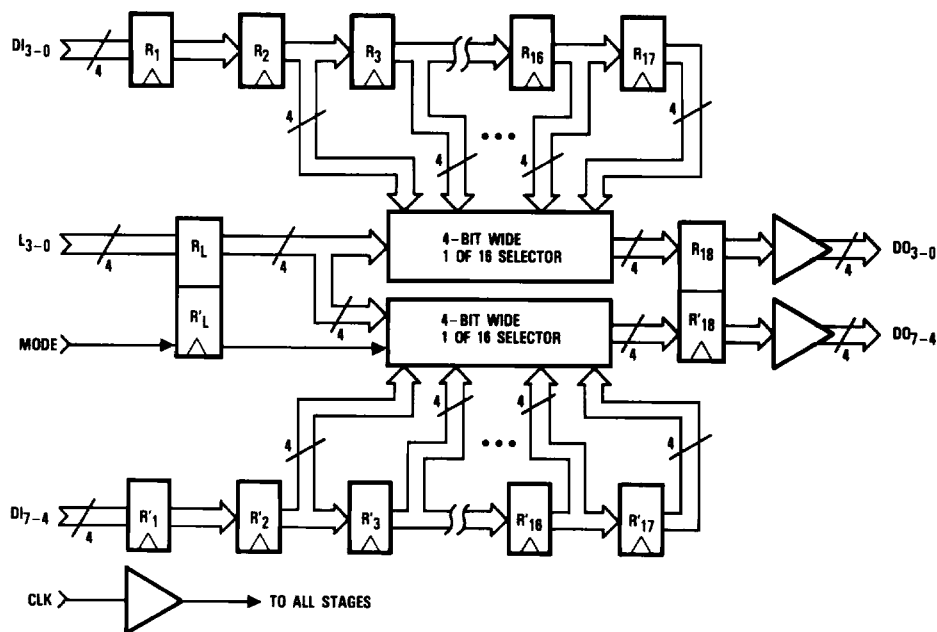
Features

- 56ns Cycle Time (Worst Case)
- Single +5V Power Supply
- TTL Compatible
- Selectable Length From 3 To 18 Stages
- Special 4-Bit Wide Mixed-Delay Mode
- Available In 24 Pin DIP, CERDIP And 28 Contact Chip Carrier

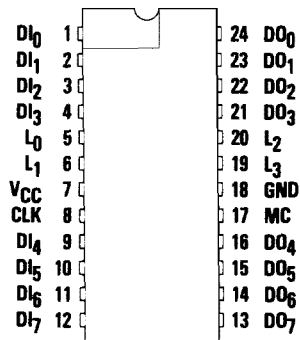
Applications

- Word Size Expansion Of TDC1028
- Video Filtering
- High-Speed Data Acquisition
- Local Storage Registers
- Digital Delay Lines
- Television Special Effects

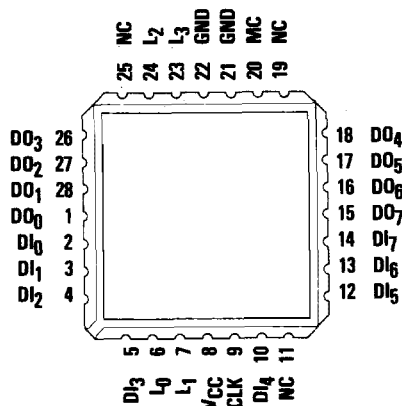
Functional Block Diagram



Pin Assignments



24 Pin DIP — J7 Package
 24 Pin Cerdip — B2 Package
 24 Pin Cerdip — B7 Package



28 Contact Chip Carrier — C3 Package

Functional Description

General Information

The TDC1011 consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock.

Power

The TDC1011 operates from a single +5 Volt supply.

Inputs

The eight inputs to the TDC1011 are divided into two groups of four, and are intended to support the TDC1028, which has inputs in groups of four bits. The lengths of these two groups are different when the Mode Control (MC) is HIGH (refer to the **Controls** section). The incoming data is unchanged by the TDC1011. All inputs are fully TTL compatible and all internal circuitry is static.

Outputs

The outputs of the TDC1011 are delayed relative to the input signals. The amount of the delay is programmable (refer to the **Controls** section). The outputs remain valid

for a minimum of t_{H0} nanoseconds after the leading edge of CLK. This allows the data to be latched into circuits with non-zero hold time requirements.

Clock

The TDC1011 operates synchronously from a single master clock line, which can be clocked up to 18MHz. All operations occur at the rising edge of the master clock. Since the internal circuitry is static, the clock can be gated if desired.

Controls

The TDC1011 has four length selection controls and one mode selection control. The operation of these controls is shown in **Table 1**.

No Connect

There are several pins labeled no connect (NC) on the TDC1011 C3 Package, which have no connections to the chip. These pins should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7, B2, B7 Package Pins	C3 Package Pins
Power	V _{CC}	Positive Supply Voltage	5.0V	7	8
	GND	Ground	0.0V	18	21, 22
Inputs	DI ₀₋₇	Data Input	TTL	1, 2, 3, 4, 9, 10, 11, 12	2, 3, 4, 5, 10, 12, 13, 14
Outputs	DO ₀₋₇	Data Output	TTL	24, 23, 22, 21, 16, 15, 14, 13	1, 28, 27, 26, 18, 17, 16, 15
Clock	CLK	Clock	TTL	8	9
Controls	L ₀	Length Select LSB	TTL	5	6
	L ₁	Length Select	TTL	6	7
	L ₂	Length Select	TTL	20	24
	L ₃	Length Select MSB	TTL	19	23
	MC (Mode)	Mode Control	TTL	17	20
No Connect	NC	No Connect	Open	None	11, 19, 25

Table 1. Length Programming

Input Code				Mode (MC) = 0		Mode (MC) = 1	
L ₃	L ₂	L ₁	L ₀	DO ₃₋₀ Length	DO ₇₋₄ Length	DO ₃₋₀ Length	DO ₇₋₄ Length
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18



Figure 1. Timing Diagram (Preset Length Controls)

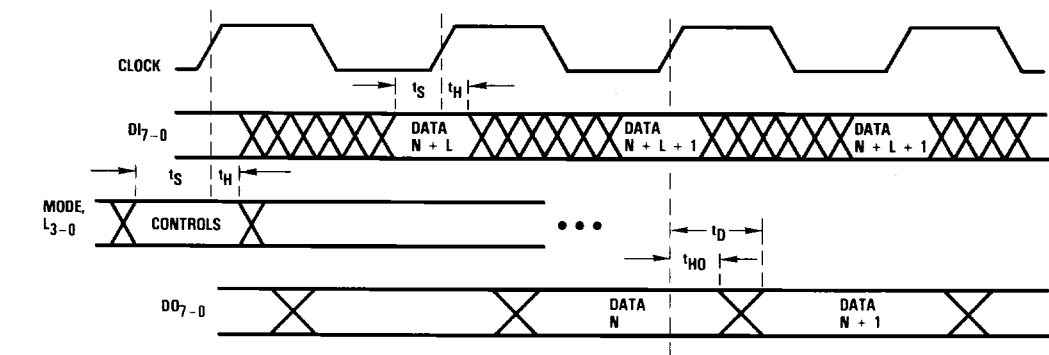


Figure 2. Length Control Operation

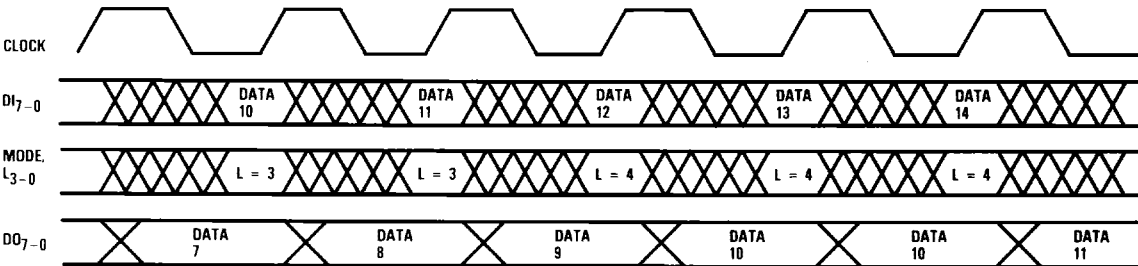


Figure 3. Equivalent Input Circuit

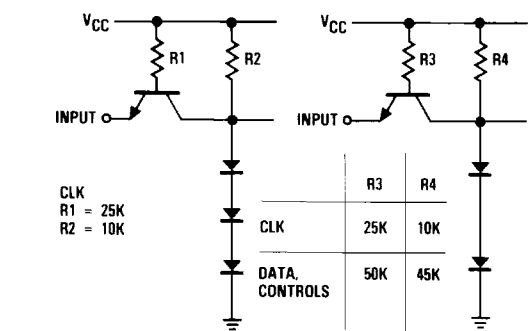


Figure 4. Equivalent Output Circuit

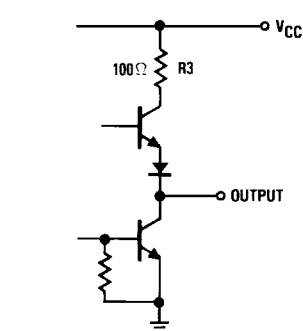
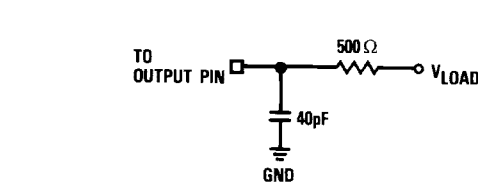


Figure 5. Test Load



Absolute maximum ratings (beyond which the device may be damaged) ¹

Supply Voltage	–0.5 to +7.0V
Input	
Applied voltage	–0.5 to +5.5V ²
Forced current	–6.0 to +6.0mA ^{3,4}
Output	
Applied voltage	–0.5 to +5.5V ²
Forced current	–1.0 to 6.0mA ^{3,4}
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	–55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	–65 to +150°C

- Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
 2. Applied voltage must be current limited to specified range, and measured with respect to GND.
 3. Forcing voltage must be limited to specified range.
 4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t _{PWL}	Clock Pulse Width, LOW	15			15			ns
t _{PWH}	Clock Pulse Width, HIGH	15			15			ns
t _S	Input Setup Time	20			25			ns
t _H	Input Hold Time	0			2			ns
V _{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V _{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V _{IHC}	Input Voltage, Logic HIGH, Clock	2.4			2.4			V
I _{OL}	Output Current, Logic LOW			4.0			4.0	mA
I _{OH}	Output Current, Logic HIGH			− 400			− 400	μA
T _A	Ambient Temperature, Still Air	0		70				°C
T _C	Case Temperature				− 55		125	°C



Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I _{CC}	Supply Current	V _{CC} = Max, Static		150		200	mA
I _{IL}	Input Current, Logic LOW	V _{CC} = Max, V _I = 0.4V					
		Data Inputs		− 0.4		− 0.4	mA
		Clock		− 1.0		− 1.0	mA
I _{IH}	Input Current, Logic HIGH	V _{CC} = Max, V _I = 2.4V		75		75	μA
I _I	Input Current, Max Input Voltage	V _{CC} = Max, V _I = 5.5V		1.0		1.0	mA
V _{OL}	Output Voltage, Logic LOW	V _{CC} = Min, I _{OL} = Max		0.5		0.5	V
V _{OH}	Output Voltage, Logic HIGH	V _{CC} = Min, I _{OH} = Max	2.4		2.4		V
I _{OS}	Short-Circuit Output Current	V _{CC} = Max, Output HIGH, one pin to ground, one second duration max.		− 40		− 40	mA
C _I	Input Capacitance	T _A = 25°C, F = 1MHz		15		15	pF
C _O	Output Capacitance	T _A = 25°C, F = 1MHz		15		15	pF

Switching characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
t _{CLK} Clock Rate	V _{CC} = Min					
	Static Length Controls	18		15		MHz
	Dynamic Length Controls	15		10		MHz
t _D Output Delay	V _{CC} = Min, Test Load: V _{LOAD} = 2.2V		25		30	ns
t _{HO} Output Hold Time ²	V _{CC} = Max, Test Load: V _{LOAD} = 2.2V	5		5		ns

Notes: 1. All transitions are measured at a 1.5V level.

2. Guaranteed, not tested.

Application Notes

The TDC1011 has two types of applications: as a support device for the TDC1028, and as a general variable-length shift register.

To support the TDC1028, the lengths will be set to one of the following:

1. Both sections 9 stages long.
2. One section 9 stages long, the other section 18 stages long.
3. Both sections 18 stages long.

The sections are interchangeable only if the lengths are identical.

Further description of the use of the TDC1011 to support the TDC1028 is given in TRW LSI Products Inc. *Application Note TP-22*.

For general use, it is important to note that the length control inputs are registered. There are no constraints on the use of the control leads other than the operational requirements shown in the *Operating Conditions Table*. Specifically, the length can be increased from one clock period to another and proper operation will occur; no data is lost, except the eighteenth stage.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1011B2C TDC1011B2A	STD- $T_A = 0^{\circ}\text{C}$ to 70°C EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	Commercial High Reliability	24 Pin Cerdip ¹ 24 Pin Cerdip ¹	1011B2C 1011B2A
TDC1011B7C TDC1011B7A	STD- $T_A = 0^{\circ}\text{C}$ to 70°C EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	Commercial High Reliability	24 Pin Cerdip ² 24 Pin Cerdip ²	1011B7C 1011B7A
TDC1011C3C TDC1011C3A	STD- $T_A = 0^{\circ}\text{C}$ to 70°C EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	Commercial High Reliability	28 Contact Hermetic Ceramic Chip Carrier 28 Contact Hermetic Ceramic Chip Carrier	1011C3C 1011C3A
TDC1011J7C TDC1011J7A	STD- $T_A = 0^{\circ}\text{C}$ to 70°C EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	Commercial High Reliability	24 Pin Hermetic Ceramic DIP 24 Pin Hermetic Ceramic DIP	1011J7C 1011J7A

Notes: 1. 0.3 inches wide.
2. 0.6 inches wide.

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