Am79C83

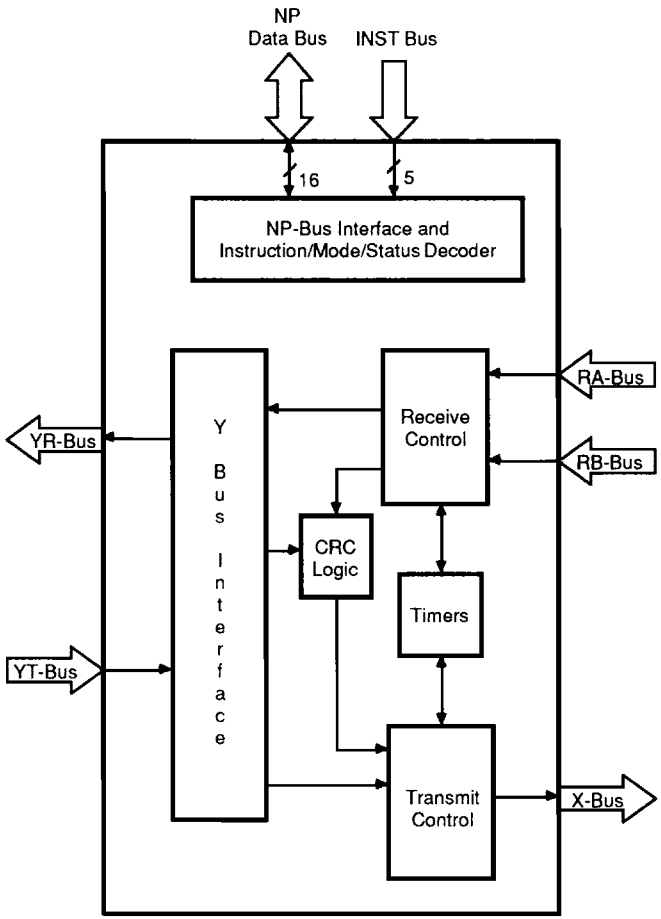
Fiber Optic Ring Media Access Controller (FORMAC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements Media Access Control (MAC) layer protocol for the ANSI X3T9.5 standard (Fiber Distributed Data Interface, FDDI)**
- **Error detection capability**
  - Cyclic redundancy checking and generation
  - Token claiming and beacon modes
- **Diagnostics Features**
  - Four loopback modes
  - Status bit collection
- **Supports data rates up to 100 Mbps**
- **Supports group, individual, and broadcast addressing**
- **Allows external address detection circuits**
  - Useful in bridge applications
- **Supports prioritized transmission of asynchronous messages**
- **Promiscuous mode for network monitoring**

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am79C83A Fiber Optic Ring Media Access Controller (FORMAC) is a CMOS device which implements the timed token passing protocol specified by the FDDI standard. It performs frame formation functions such as generating preamble, CRC, and status information. It facilitates error recovery with token claiming and beaconing capability. Information needed by station-management software for ring diagnostics and statistical network characterization is also provided by the FORMAC.

Notes:

The word "frame" is used in the SUPERNET data sheets to describe three different groups of information.

1. One group is passed over the network media and has the following structure:

Frame Preamble	Start Delimiter	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	End Delimiter	Frame Status

2. The others are stored in buffer memory and are structured as follows:
   A) Transmit frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	Pointer

   B) Receive frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence

TABLE OF CONTENTS

CONNECTION DIAGRAM
PGA Bottom View (Pins facing up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	VCC	R/W	INST2	INST1	DS	NP15	NP13	NP11	NP8	NP4	NP2	NP1	NMINTR	READY	RAP	1
2	NC	RESET	INST3	CST	NP14	NP12	NP10	NC	NP6	NP5	NP3	NP0	HOLD1	HOLD2	RACU	2
3	NC	YR7	BCLK	INST0	GND	BMODE	GND	NP9	VCC	NP7	GND	MINTR	LPBEN	RA6	RACL	3
4	YR5	YR4	YR6	●									GND	RA7	NC	4
5	YR2	YR0	YRP										RA2	RA4	RA5	5
6	YT7	YR3	GND										RA3	RA1	RA0	6
7	VCC	YTP	YR1										VCC	RBP	RBCU	7
8	YT6	GND	GND				**Bottom View**						RBCL	RB7	NC	8
9	YT4	YT5	YT1										GND	RB5	RB6	9
10	YT2	YT0	RDYTBYT										RB4	RB3	RB2	10
11	XMTABTI	YT3	XMEDAVA										GND	RB1	RB0	11
12	XMTABTO	XMEDAVS	GND										XP	XCU	XCL	12
13	RECEIVE	XFRBYTE	FULL	MEDREQA	GND	LNGADR	XSAMAT	GND	S1	LSTINC	X2	TOKISD	X7	X5	X6	13
14	DAVALID	RCVABTI	MISFRM	MEDREOS	INICLBN	XDAMAT	COUT	GND	AOUT	FRINC	ERRINC	GND	X0	VCC	X4	14
15	FSHRCVF	RCVABTO	SI	TEST	CLM/BEC	FSVLD	SDRCVD	VCC	EOUT	S0	S2	S3	S0	X1	X3	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

NC = No Connection

09731-002A

PIN DESIGNATIONS

(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A–1	V_{CC}	C–7	YR_1	H–13	GND	N–10	RB_4
A–2	NC	C–8	GND	H–14	GND	N–11	GND
A–3	NC	C–9	YT_1	H–15	V_{CC}	N–12	XP
A–4	YR_5	C–10	RDYTBYT	J–1	NP_8	N–13	X_7
A–5	YR_2	C–11	XMEDAVA	J–2	NP_6	N–14	X_0
A–6	YT_7	C–12	GND	J–3	VCC	N–15	S_0
A–7	V_{CC}	C–13	FULL	J–13	S_1	P–1	$\overline{READY}$
A–8	YT_6	C–14	MISFRM	J–14	AOUT	P–2	$HOLD_2$
A–9	YT_4	C–15	SI	J–15	EOUT	P–3	RA_6
A–10	YT_2	D–1	$INST_1$	K–1	NP_4	P–4	RA_7
A–11	XMTABTI	D–2	$\overline{CSI}$	K–2	NP_5	P–5	RA_4
A–12	XMTABTO	D–3	$INST_0$	K–3	NP_7	P–6	RA_1
A–13	RECEIVE	D–4	GUIDE PIN	K–13	LSTINC	P–7	RBP
A–14	DAVALID	D–13	MEDREQA	K–14	FRINC	P–8	RB_7
A–15	FSHRCVF	D–14	MEDREQS	K–15	S_0	P–9	RB_5
B–1	R/$\overline{W}$	D–15	TEST	L–1	NP_2	P–10	RB_3
B–2	$\overline{RESET}$	E–1	$\overline{DS}$	L–2	NP_3	P–11	RB_1
B–3	YR_7	E–2	NP_{14}	L–3	GND	P–12	XCU
B–4	YR_4	E–3	GND	L–13	X_2	P–13	X_5
B–5	YR_0	E–13	GND	L–14	ERRINC	P–14	VCC
B–6	YR_3	E–14	INICLBN	L–15	S_2	P–15	X_1
B–7	YTP	E–15	CLM/$\overline{BEC}$	M–1	NP_1	R–1	RAP
B–8	GND	F–1	NP_{15}	M–2	NP_0	R–2	RACU
B–9	YT_5	F–2	NP_{12}	M–3	$\overline{MINTR}$	R–3	RACL
B–10	YT_0	F–3	BMODE	M–13	TOKISD	R–4	NC
B–11	YT_3	F–13	LNGADR	M–14	GND	R–5	RA_5
B–12	XMEDAVS	F–14	$\overline{XDAMAT}$	M–15	S_3	R–6	RA0
B–13	XFRBYTE	F–15	$\overline{FSVLD}$	N–1	$\overline{NMINTR}$	R–7	RBCU
B–14	RCVABTI	G–1	NP_{13}	N–2	$HOLD_1$	R–8	NC
B–15	RCVABTO	G–2	NP_{10}	N–3	LPBEN	R–9	RB_6
C–1	$INST_2$	G–3	GND	N–4	GND	R–10	RB_2
C–2	$INST_3$	G–13	$\overline{XSAMAT}$	N–5	RA_2	R–11	RB_0
C–3	BCLK	G–14	COUT	N–6	RA_3	R–12	XCL
C–4	YR_6	G–15	SDRCVD	N–7	VCC	R–13	X_6
C–5	YRP	H–1	NP_{11}	N–8	RBCL	R–14	X_4
C–6	GND	H–2	NC	N–9	GND	R–15	X_3
		H–3	NP_9				

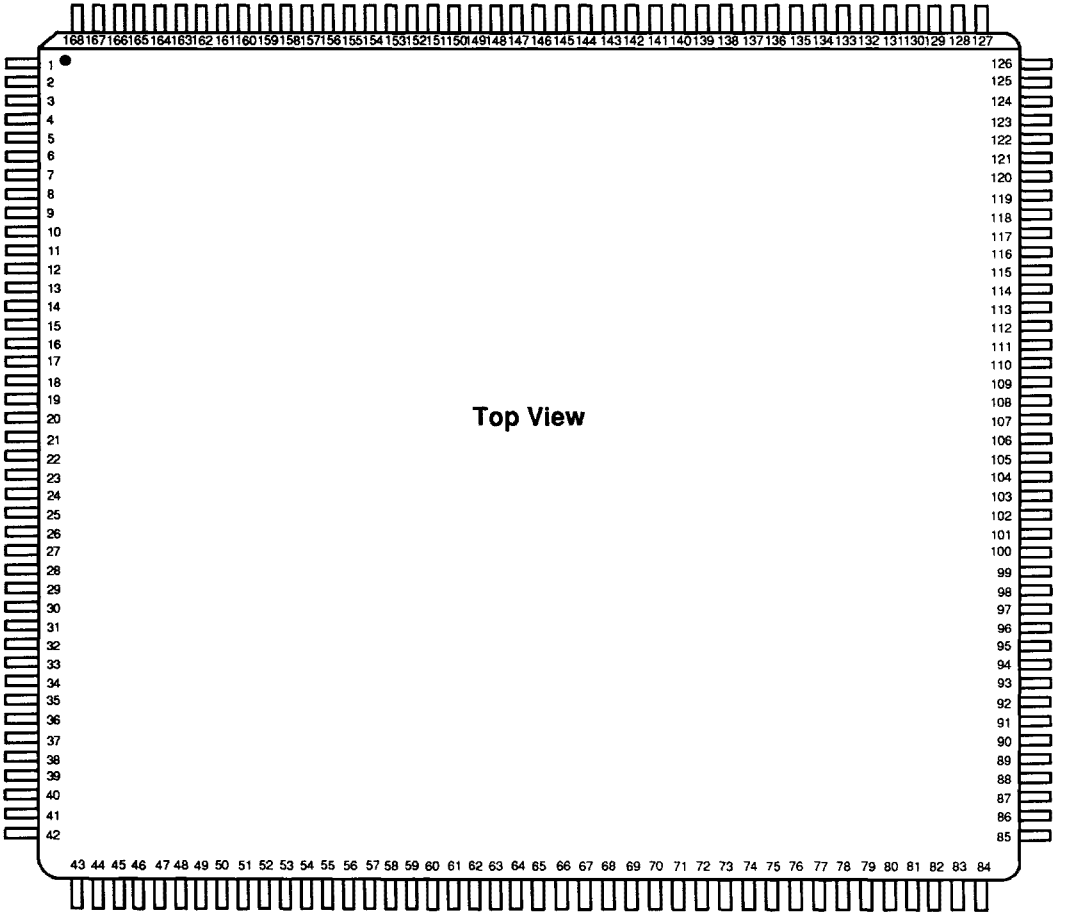
PIN DESIGNATIONS

(Sorted by Pin Name)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
J–14	AOUT	F–13	LNGADR	P–11	RB_1	P–13	X_5
C–3	BCLK	N–3	LPBEN	R–10	RB2	R–13	X_6
F–3	BMODE	K–13	LSTINC	P–10	RB_3	N–13	X_7
E–15	CLM/$\overline{BEC}$	D–13	MEDREQA	N–10	RB_4	R–12	XCL
G–14	COUT	D–14	MEDREQS	P–9	RB_5	P–12	XCU
D–2	$\overline{CSI}$	M–3	$\overline{MINTR}$	R–9	RB_6	F–14	$\overline{XDAMAT}$
A–14	DAVALID	C–14	MISFRM	P–8	RB_7	B–13	XFRBYTE
E–1	$\overline{DS}$	N–1	$\overline{NMINTR}$	N–8	RBCL	C–11	XMEDAVA
J–15	EOUT	M–2	NP_0	R–7	RBCU	B–12	XMEDAVS
L–14	ERRINC	M–1	NP_1	P–7	RBP	A–11	XMTABTI
K–14	FRINC	L–1	NP_2	B–14	RCVABTI	A–12	XMTABTO
A–15	FSHRCVF	L–2	NP_3	B–15	RCVABTO	N–12	XP
F–15	$\overline{FSVLD}$	K–1	NP_4	C–10	RDYTBYT	G–13	$\overline{XSAMAT}$
C–13	FULL	K–2	NP_5	P–1	$\overline{READY}$	B–5	YR0
H–14	GND	J–2	NP_6	A–13	RECEIVE	C–7	YR_1
E–13	GND	K–3	NP_7	B–2	$\overline{RESET}$	A–5	YR_2
B–8	GND	J–1	NP_8	K–15	S_0	B–6	YR_3
G–3	GND	H–3	NP_9	J–13	S_1	B–4	YR_4
N–9	GND	G–2	NP_{10}	L–15	S_2	A–4	YR_5
E–3	GND	H–1	NP_{11}	M–15	S_3	C–4	YR_6
C–6	GND	F–2	NP_{12}	G–15	SDRCVD	B–3	YR_7
M–14	GND	G–1	NP_{13}	C–15	SI	C–5	YRP
N–11	GND	E–2	NP_{14}	N–15	SO	B–10	YT_0
C–8	GND	F–1	NP_{15}	D–15	TEST	C–9	YT_1
N–4	GND	B–1	R/$\overline{W}$	M–13	TOKISD	A–10	YT_2
C–12	GND	R–6	RA0	A–1	VCC	B–11	YT_3
H–13	GND	P–6	RA_1	N–7	V_{CC}	A–9	YT_4
L–3	GND	N–5	RA_2	J–3	V_{CC}	B–9	YT_5
D–4	GUIDE PIN	N–6	RA_3	A–7	V_{CC}	A8	YT_6
N–2	$HOLD_1$	P–5	RA_4	P–14	V_{CC}	A–6	YT_7
P–2	$HOLD_2$	R–5	RA_5	H–15	V_{CC}	B–7	YTP
E–14	INICLBN	P–3	RA_6	N–14	X_0	R–4	NC
D–3	$INST_0$	P–4	RA_7	P–15	X_1	A–3	NC
D–1	$INST_1$	R–3	RACL	L–13	X_2	A–2	NC
C–1	$INST_2$	R–2	RACU	R–15	X3	R–8	NC
C–2	$INST_3$	R–1	RAP	R–14	X_4	H–2	NC
		R–11	RB0				

CONNECTION DIAGRAM

168-Pin PQFP



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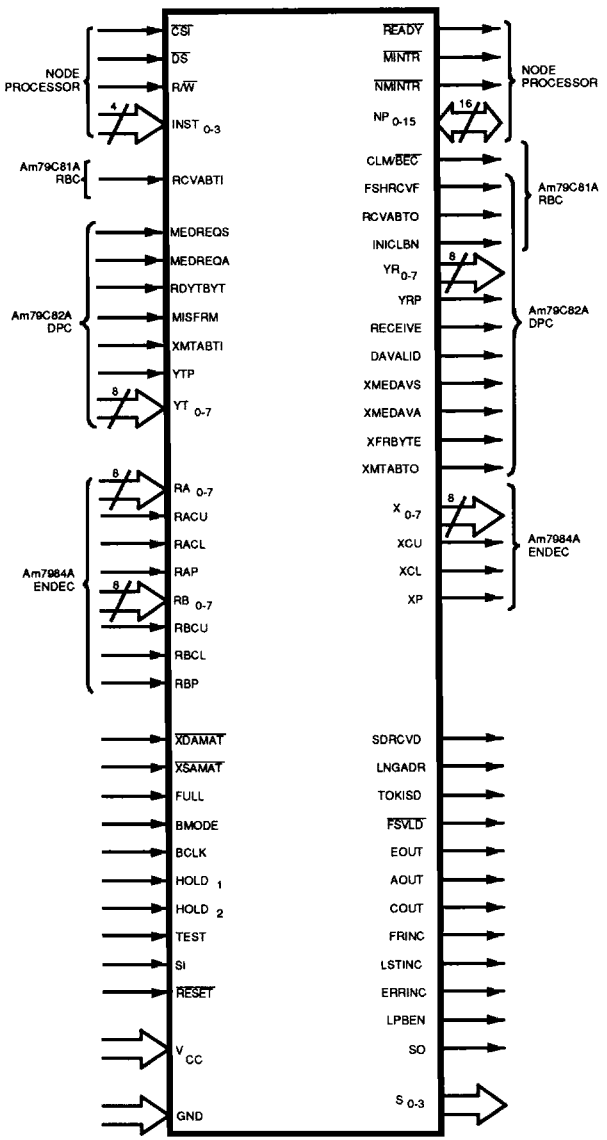
PIN DESIGNATIONS
Plastic Quad Flat Package

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	43	NC	85	NC	127	NC
2	NC	44	NC	86	NC	128	NC
3	NC	45	NC	87	NC	129	NC
4	$\overline{\text{RESET}}$	46	RCVABTI	88	VCC	130	HOLD1
5	BCLK	47	RCVABTO	89	X4	131	HOLD2
6	YRP	48	MISFRM	90	X5	132	LPBEN
7	YR7	49	FULL	91	X6	133	$\overline{\text{READY}}$
8	YR6	50	GND	92	X7	134	$\overline{\text{MINTR}}$
9	YR5	51	SI	93	XCL	135	$\overline{\text{NMINTR}}$
10	GND	52	TEST	94	GND	136	GND
11	YR4	53	MEDREQS	95	XCU	137	NP0
12	YR3	54	MEDREQA	96	XP	138	NP1
13	YR2	55	INICLBN	97	RB0	139	NP2
14	YR1	56	CLM/$\overline{\text{BEC}}$	98	RB1	140	NP3
15	YR0	57	$\overline{\text{FSVLD}}$	99	RB2	141	NP4
16	YTP	58	$\overline{\text{XSAMAT}}$	100	RB3	142	NP5
17	YT7	59	$\overline{\text{XDAMAT}}$	101	RB4	143	NP6
18	YT6	60	LNGADR	102	RB5	144	NP7
19	VCC	61	SDRCVD	103	RB6	145	NP8
20	NC	62	COUT	104	GND	146	VCC
21	GND	63	GND	105	GND	147	NC
22	GND	64	GND	106	GND	148	GND
23	GND	65	GND	107	NC	149	GND
24	YT5	66	NC	108	VCC	150	GND
25	YT4	67	VCC	109	NC	151	NP9
26	YT3	68	AOUT	110	RB7	152	NP10
27	YT2	69	EOUT	111	RBCL	153	NP11
28	YT1	70	FRINC	112	RBCU	154	NP12
29	YT0	71	LSTINC	113	RBP	155	NP13
30	RDYTBYT	72	ERRINC	114	RA0	156	NP14
31	XMTABTI	73	S0	115	RA1	157	NP15
32	NC	74	S1	116	RA2	158	BMODE
33	XMTABTO	75	S2	117	RA3	159	$\overline{\text{DS}}$
34	XMEDAVS	76	S3	118	RA4	160	GND
35	XMEDAVA	77	GND	119	RA5	161	$\overline{\text{CS}}$
36	XFRBYTE	78	TOKISD	120	RA6	162	INST0
37	GND	79	SO	121	RA7	163	INST1
38	RECEIVE	80	X0	122	GND	164	INST2
39	DAVALID	81	X1	123	RACL	165	INST3
40	FSHRCVF	82	X2	124	RACU	166	R/$\overline{\text{W}}$
41	NC	83	X3	125	RAP	167	VCC
42	NC	84	NC	126	NC	168	NC

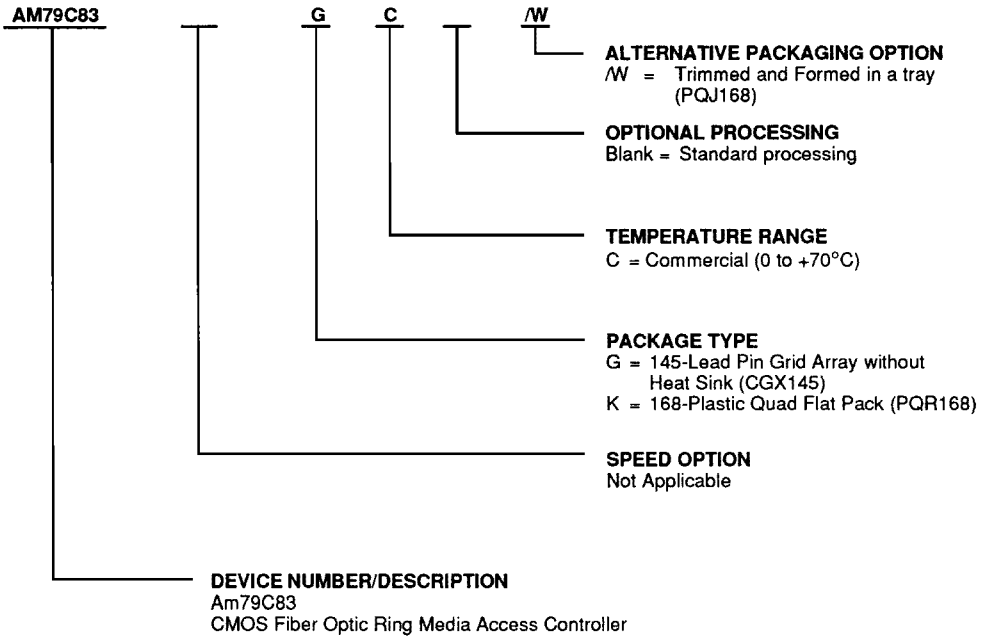
LOGIC SYMBOL



09731-003A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
AM79C83	GC, KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

RBC Interface

RCVABTI
Receive Abort In (Input; Active HIGH)

This input indicates that an external event has caused a received frame to be aborted. One such event may be when Buffer Memory is full. The FORMAC will set the C_indicator on address-recognized frames unless RCVABTI or MISFRM goes HIGH or the FORMAC is forced out of the receive state, as evidenced by RCVABTO being driven HIGH. RCVABTI will cause the FORMAC to drive the RECEIVE, DAVALID, and FSHRCVF outputs LOW and three state the YR-bus until the next frame is received.

DPC Interface

All output pins which go to the DPC change state synchronously with BCLK. All input pins which are driven by the DPC must be asserted synchronously with BCLK.

CLM/$\overline{\text{BEC}}$
Claim/$\overline{\text{Beacon}}$ (Output)

The CLM/$\overline{\text{BEC}}$ pin is used in conjunction with INICLBN. CLM/$\overline{\text{BEC}}$ is a level signal that is HIGH when a claim is required for transmission.

DAVALID
Data Valid (Output; Active HIGH)

The DAVALID signal indicates that the FORMAC has placed valid data on the YR-bus. If DAVALID is HIGH when RECEIVE is HIGH, the data output to the YR-bus is part of the frame received from the media. If DAVALID is HIGH and RECEIVE is LOW, the data output to the YR-bus represents status information. This occurs on the clock cycle when RECEIVE is brought LOW. DAVALID remains HIGH for an integral number of clock cycles. DAVALID will also go LOW during frame reception when the FORMAC is put on "hold" by a HIGH $HOLD_1$ input.

FSHRCVF
Flush Received Frame (Output; Active HIGH)

The FSHRCVF pin is used to inform the RBC and DPC that the frame currently being received should not be copied. FSHRCVF is asserted on two conditions. One condition is when the frame being received is a fragment. This occurs when the FORMAC encounters a non-data symbol in the frame stream before the End Delimiter is encountered. (FSHRCVF will be asserted the cycle prior to RECEIVE going LOW). Alternatively, the FSHRCVF output may indicate the result of the FORMAC address detect comparison. The pin is activated for one BCLK cycle while RECEIVE is HIGH when the destination address (DA) of the received frame does not match the node's own address. This condition is indicated when neither the internal address detect logic nor the $\overline{\text{XDAMAT}}$ input result in a match condition.

INICLBN
Initialize Claim/Beacon (Output; Active HIGH)

The INICLBN pin is set HIGH for one cycle, indicating a need to issue claim or beacon frames. The type of frame required is determined by the CLM/$\overline{\text{BEC}}$ output. After activating INICLBN, the FORMAC expects the proper frame to be queued for transmission via an S-frame media request (MEDREQS). The claim or beacon should be continuously queued until the FORMAC indicates otherwise. This indication can come in two forms. First, if the FORMAC wishes to switch from issuing claims to issuing beacons (or vise versa), INICLBN will be asserted again. Secondly, if the FORMAC transmit state machine returns to idle, then the FORMAC will assert XMTABTO.

MEDREQA
Media Request Asynchronous (Input; Active HIGH)

The MEDREQA input indicates a DPC request for access to the medium so that A-frames may be transmitted. If MEDREQA is HIGH, MEDREQS is LOW, and the medium is available; then the FORMAC will assert the XMEDAVA line.

MEDREQS
Media Request Synchronous (Input; Active HIGH)

The MEDREQS input indicates a DPC request for access to the medium so that S-frames may be transmitted. If MEDREQS is HIGH and the medium is available then the FORMAC will assert the XMEDAVS line.

MISFRM
Missed Frame (Input; Active HIGH)

Missed Frame is generated by the DPC when frames cannot be copied due to inter-frame gap error. The DPC handles this condition differently from the case of a receive abort. The FORMAC, however, treats these cases identically. The FORMAC will inhibit setting the C_indicator of the second frame when the MISFRM is received. RECEIVE, DAVALID, and FSHRCVF are dropped and the YR-bus is set to the high-impedance state.

RCVABTO
Receive Abort Out (Output; Active HIGH)

The RCVABTO pin is asserted for one BCLK cycle when the FORMAC receiver is interrupted while the RECEIVE output is HIGH. Such an interruption occurs when the FORMAC transmitter leaves the idle or repeat states due to a network event or an instruction to enter a new state.

RDYTBYT

Ready to Transmit Byte (Input; Active HIGH)

The RDYTBYT is an indication from the DPC that it has filled its internal FIFO and can guarantee transmission of a continuous frame. Normally, RDYTBYT will remain HIGH until the FORMAC receives the entire frame. In case of an abort, it can go LOW before the frame transmission is complete. RDYTBYT must never be HIGH if XMEDAVS and XMEDAVA are both LOW.

RECEIVE

Receive Frame (Output; Active HIGH)

The RECEIVE signal indicates that a received frame is being sent from the FORMAC to the DPC. Each frame is bound by an active RECEIVE signal. It is set HIGH when the frame control (FC) field is clocked onto the YR-bus. RECEIVE goes LOW one byte after the final byte of the frame's Frame Check sequence (or information field) is sent onto the YR-bus.

XFRBYTE

Transfer Byte (Output; Active HIGH)

The XFRBYTE output is asserted by the FORMAC in response to the RDYTBYT input. It indicates that the FORMAC is ready to read a byte from the YT-bus. XFRBYTE may stay HIGH for one or more cycles. XFRBYTE can go HIGH only if RDYTBYT is asserted.

XMEDAVA

Transmit Media Available for Asynchronous (Output; Active HIGH)

The XMEDAVA is a handshake signal between the DPC and FORMAC that is generated when MEDREQA is HIGH and a usable token is captured or held. XMEDAVA is analogous to the XMEDAVS signal. XMEDAVA will not be asserted when XMEDAVS is active (i.e., S-frames take precedent).

XMEDAVS

Transmit Media Available for Synchronous (Output; Active HIGH)

The XMEDAVS is a handshake signal between the DPC and FORMAC that is generated in response to both of the following conditions: 1) MEDREQS is HIGH and a usable token is captured or held, or 2) MEDREQS is HIGH and the FORMAC has received an ILDSNDM instruction. XMEDAVS goes LOW after the frame is transmitted (end of frame is signified by the RDYTBYT input going LOW). If the MEDREQS remains HIGH and the FORMAC determines that another transmission opportunity exists, the XMEDAVS will go HIGH again in the next clock cycle.

XMTABTI

Transmit Abort In (Input; Active HIGH)

If an abort is initiated through the DPC, then MEDREQS, MEDREQA, and RDYTBYT are set LOW. One cycle later, the XMTABTI pin is asserted. Upon detecting XMTABTI HIGH, the FORMAC aborts the outgoing frame by ensuring that the FCS and FS fields are not appended to the frame.

XMTABTO

Transmit Abort Out (Output; Active HIGH)

XMTABTO is generated when the FORMAC exits the claim/beacon mode.

YR_{0-7}

Y Receive Bus (Output; Three State)

The YR-bus is used to transfer data received from the media to the DPC. The YR-bus is also used to send status information to the DPC at the end of a frame transfer. The YR-bus is active when either the RECEIVE or DAVALID outputs are HIGH.

When the FORMAC receives a frame from the media and the transmitter is in the idle or repeat state (in half-duplex mode), the YR-bus is enabled and the RECEIVE line is set HIGH. DAVALID is asserted as the data is sent to the Y-bus. In full-duplex mode, YR is always configured for output. Frames received from the media are presented on the YR-bus regardless of the transmitter state.

Status information is also passed over the YR-bus. The received frame's status is stored as a byte in the FORMAC, appended to the end of the frame and output to the Y-bus. The FORMAC indicates this status byte with a special handshake. When the status is placed on the bus, DAVALID is set HIGH while RECEIVE remains LOW.

YRP

Y Receive Bus Parity (Output; Three State, Active HIGH)

YRP indicates odd parity on the YR-bus. This signal changes state at the same time as the YR-bus.

YT_{0-7}
Y Transmit Bus (Inputs)

The YT-bus carries data to be transmitted on the media from the DPC to the FORMAC. The YT-bus interfaces to Y-bus of the DPC. In a half-duplex system, the YT input and YR output bus share the Y-bus of a common DPC. Data for transmission is passed to the FORMAC over the YT-bus synchronous to the BCLK. Data flow is controlled using a two-wire handshake. When the DPC is ready to transmit data, it sets the RDYTBYT line HIGH. When the FORMAC is ready to receive the frame, the XFRBYTE line is set HIGH.

YTP
Y Transmit Bus Parity (Input; Active HIGH)

The YTP signal indicates odd parity on the YT-bus.

ENDEC Interface

The following sections describe the pins used to interface the FORMAC with the Am7984A ENDEC. All outputs to the ENDEC are driven synchronously with BCLK. All inputs must change state synchronously with BCLK.

RA_{0-7}
Receive Bus A (Inputs)

The RA-bus is used to receive information from an ENDEC. Bytes are clocked into the FORMAC RA-bus synchronously with BCLK.

RACL
Receive A Control Lower (Input; Active HIGH)

The RACL is driven HIGH to indicate that the lower nibble of the RA-bus (RA_{0-3}) is a network control character.

RACU
Receive A Control Upper (Input; Active HIGH)

RACU is driven HIGH to indicate that the upper nibble of the RA-bus (RA_{4-7}) is a network control character. When RACU is LOW, this nibble contains data.

RAP
Receive A Parity (Input; Active HIGH)

The RAP input reflects odd parity on the RA_{0-7}, RACU, RACL, and RAP lines. If the number of "1s" on RA_{0-7}, RACU, and RACL is odd, then RAP will be logic "0".

RB_{0-7}
Receive Bus B (Inputs)

The RB-bus is used to receive information from an ENDEC. Bytes are clocked into the FORMAC RB-bus synchronously with BCLK.

RBCL
Receive A Control Lower (Input; Active HIGH)

The RBCL is asserted to indicate that the lower nibble of the RB-bus (RB_{0-3}) is a network control character. RBCL is synchronous with the BCLK.

RBCU
Receive B Control Upper (Input; Active HIGH)

RBCU is asserted to indicate that the upper nibble of the RB-bus (RB_{4-7}) is a network control character. When RBCU is LOW, this nibble contains data. RBCU is synchronous with the BCLK.

RBP
Receive B Parity (Input; Active HIGH)

The RBP input reflects odd parity on the RB_{0-7}, RBCU, RBCL, and RBP lines. If the number of "1s" on RB_{0-7}, RBCU, and RBCL is odd, then RBP will be logic "0".

X_{0-7}
Transmit Bus (Outputs)

This output bus is used as a path for control and data information which will be transmitted over the medium through the ENDEC.

XCL
Transmit Control Lower (Output; Active HIGH)

The XCL output signal is used to identify control symbols on the lower nibble of the transmit bus. If XCL is HIGH, the lower nibble of the X-bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

XCU
Transmit Control Upper (Output; Active HIGH)

The XCU output signal is used to flag control symbols on the upper nibble of the transmit bus. If XCU is HIGH, the upper nibble of the X-bus is interpreted as a network control character. Otherwise, it is interpreted as data nibble.

XP
Transmit Parity (Output; Active HIGH)

This signal reflects odd parity on the X_{0-7}, XCU, XCL, and XP lines. If the number of "1s" on X_{0-7}, XCU, and XCL is odd, then XP will be logic "0".

Node Processor Interface

All inputs from the Node Processor (NP) must be asserted synchronously with BCLK unless the FORMAC is in asynchronous mode (BMODE pin is LOW). All outputs to the NP change state synchronously with BCLK.

$\overline{CSI}$
Chip Select Input (Input; Active LOW)

$\overline{CSI}$ enables read and write operations to the FORMAC. It is logically "ANDed" with the $\overline{DS}$ line to enable transmit logic of the FORMAC. In synchronous mode $\overline{CSI}$ must stay LOW one BCLK cycle longer than $\overline{DS}$.

$\overline{DS}$
Data Strobe (Input; Active LOW)

This signal is logically "ANDed" with the $\overline{CSI}$ line. The $\overline{DS}$ input is part of the handshake between the NP and FORMAC when the FORMAC acts as bus slave. This input signal is set by the Node Processor to frame the data transfers between the NP and the FORMAC. The direction of the data transfer is dictated by the status of the R/$\overline{W}$ line. The NP sets $\overline{DS}$ LOW, initiating a data transfer. The FORMAC reacts asynchronously to this signal when BMode is LOW.

$INST_{0-3}$
Instruction 0–3 (Inputs)

The instruction input lines allow direct access to the FORMAC internal registers. These lines are used to place the FORMAC into different operating states. The instruction timing has been designed so that $INST_{0-3}$ can be tied to the address bus of a conventional microprocessor.

$\overline{MINTR}$
Maskable Interrupt (Output; Open Drain, Active LOW)

The $\overline{MINTR}$ output of the FORMAC is an attention line that indicates, when LOW, the status of one or more unmasked flags in the status registers.

$\overline{NMINTR}$
Non-Maskable Interrupts (Output; Open Drain, Active LOW)

The $\overline{NMINTR}$ output of the FORMAC is an attention line that indicates, when LOW, that one or more non-maskable interrupt conditions have occurred.

NP_{0-15}
Node Processor Data Bus (Input/Output; Three State)

The NP-bus is a 16-bit wide bidirectional data bus used to interface the FORMAC to the NP. Data transfer on the NP-bus can be synchronous or asynchronous depending upon the setting of the BMODE pin. For asynchronous operation, a two-wire handshake is provided through the $\overline{READY}$ and $\overline{DS}$ lines.

R/$\overline{W}$
Read/$\overline{Write}$ (Input)

This pin allows the NP to read from or write into internal registers of the FORMAC.

$\overline{READY}$
Ready (Output; Open Drain, Active LOW)

The $\overline{READY}$ output is used in the handshake between the NP and FORMAC. The FORMAC $\overline{READY}$ output provides an asynchronous acknowledgment to the NP that a data transfer is complete. The FORMAC asserts $\overline{READY}$ when it has put data onto the NP-bus during a read cycle or is about to take data off the NP-bus during a write cycle. $\overline{READY}$ is a response to the $\overline{DS}$ and will return HIGH after the $\overline{DS}$ signal goes HIGH.

Clocks, Control, and Special-Function Interfaces

AOUT
Address Indicator (Output; Active HIGH)

AOUT identifies the state of the A_indicator which is received from frames whose source address match the local address. AOUT is HIGH for set indicators and LOW for indicators received as reset or not received. The state of EOUT is only meaningful when the $\overline{FSVLD}$ output is asserted. EOUT, AOUT, and COUT will retain their values until the next Start Delimiter is received. This allows simple latching of these status bits on the falling edge of $\overline{FSVLD}$.

BCLK
Byte Clock (Input)

The BCLK is the clock that runs the media access logic in the FORMAC. Data transmitted to and received from the ENDEC interface is synchronous to BCLK.

BMODE
Bus Mode (Input)

The BMODE input is strapped HIGH for synchronous operation of the NP-bus. A LOW level allows asynchronous operation of the NP-bus.

COUT
Copy Indicator (Output; Active HIGH)

COUT identifies the state of the C_indicator received from frames whose source address match the node's address. COUT is HIGH for set indicators and LOW for indicators received as reset or not received. The state of COUT is only meaningful when the $\overline{FSVLD}$ output is asserted. EOUT, AOUT, and COUT will retain their values until the next Start Delimiter is received. This allows simple latching of these status bits on the falling edge of $\overline{FSVLD}$.

EOUT
Error Indicator (Output; Active HIGH)

EOUT identifies the state of the E_indicator received from frames whose source address match the node's address. EOUT is HIGH for set indicators and LOW for indicators received as reset or not received. The state of EOUT is only meaningful when the $\overline{FSVLD}$ output is asserted. EOUT, AOUT, and COUT will retain their values until the next Start Delimiter is received. This permits simple latching of these status bits on the falling edge of $\overline{FSVLD}$.

ERRINC
Error Counter Increment (Output; Active HIGH)

ERRINC is synchronous with BCLK and remains HIGH for one BCLK cycle. ERRINC indicates reception of an

invalid FDDI frame (invalid data length or CRC) where the error indicator was not set by a previous station. This output can be used to increment a counter for the collection of ring statistics.

FRINC
Frame Counter Increment (Output; Active HIGH)

FRINC is synchronous with BCLK and remains HIGH for one BCLK cycle. FRINC indicates reception of a symbol stream which conforms to the FDDI frame format. FRINC can be used to increment an external counter for collection of ring statistics.

$\overline{\text{FSVLD}}$
$\overline{\text{Frame Status Valid}}$ (Output; Active LOW)

This pin is used to indicate that valid status information is presented on the EOUT, AOUT, and COUT pins. $\overline{\text{FSVLD}}$ is asserted when a frame whose source address equals the local address is received. This match is determined by either the internal address detection logic or the $\overline{\text{XSAMAT}}$ input. $\overline{\text{FSVLD}}$ as well as the EOUT, AOUT, and COUT indicators are asserted on the second cycle after the End Delimiter is received on the R-bus. The rising edge of $\overline{\text{FSVLD}}$ can be used to clock EOUT, AOUT, and COUT into a register.

FULL
Full Duplex (Input; Active HIGH)

During normal operation, RECEIVE cannot go HIGH while the transmit state machine is in the transmit data, claim, or beacon states. The FULL pin overrides this requirement and is useful for implementing a full-duplex system.

HOLD_1
Hold One (Input; Active HIGH)

HOLD_1 acts as a suspend/resume feature. When HOLD_1 is asserted, the FORMAC receive state machines and the internal pipelines will hold their present values. Bytes received during the cycle following HOLD_1 assertion are ignored. If the chip is transmitting or receiving on the Y-bus, HOLD_1 will also cause XFRBYT and/or DAVALID to go LOW. The TVX timer will be held and frame transmission suspended as a result of HOLD_1. No other timers are affected by HOLD_1.

HOLD_2
Hold Two (Input; Active HIGH)

HOLD_2 holds the current state of the THT and TRT timers.

LNGADR
Long Address (Output; Active HIGH)

The LNGADR output becomes valid during the BCLK cycle after the SDRCVD pin is asserted. The LNGADR output value will hold until the next Start Delimiter is received. LNGADR is asserted if the frame's frame-control field indicates a 48-bit address. The LNGADR output is used in conjunction with the SDRCVD signal to support external address detection and token discrimination. Upon reception of a token, the LNGADR output will be HIGH if the frame-control field identifies the token as a restricted token.

LPBEN
Loopback Enable (Output; Active HIGH)

LPBEN is asserted when the FORMAC enters loopback mode. This pin is provided to support configurations using external hardware to store loopback frames.

LSTINC
Lost Counter Increment (Output; Active HIGH)

LSTINC is synchronous with BCLK and remains HIGH for one BCLK cycle. LSTINC indicates reception of a non-data, non-End Delimiter symbol pair in the midst of frame. LSTINC can be used to increment an external counter for collection of ring statistics.

$\overline{\text{RESET}}$
$\overline{\text{Reset}}$ (Input; Active LOW)

$\overline{\text{RESET}}$ is an asynchronous input which initializes the internal FORMAC state machines and registers. It must be held LOW for at least four BCLK cycles.

S_{0-3}
Status Receive (Outputs)

The S pins indicate the type of frame received by the FORMAC (regardless of destination or source address match). The bit assignment is as follows:

S_3	S_2	S_1	S_0	Description
0	0	0	0	Quiescent
0	0	0	1	Claim frame
0	0	1	0	Beacon frame
0	0	1	1	Other MAC frame
0	1	0	0	NSA frame
0	1	0	1	Other SMT frame
0	1	1	0	Implementor frame
0	1	1	1	Reserved
1	0	0	0	Pass Token—Unrestricted
1	0	0	1	Pass Token-Restricted
1	0	1	0	Capture Token—Unrestricted
1	0	1	1	Capture Token—Restricted
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	PH_Invalid Received

The S pins are set to logic "0" upon reset. They remain in this state until a frame is received from the ring. After the frame status field is received, the code corresponding to the frame type is driven onto the S pins for one BCLK cycle. PH_Invalid is output upon receipt of the PH_Invalid symbol from an ENDEC. PH_Invalid is indicated by all "1s" on the upper nibble of the selected R-bus with the upper and lower control input held HIGH. These pins can be used by the NP in conjunction with external RS flip-flops.

SDRCVD

Start Delimiter Received (Output; Active HIGH)

The SDRCVD output is asserted after a Start Delimiter (JK) is received at the FORMAC input. The signal remains HIGH for one clock cycle. The SDRCVD pin is used to support external address detection.

SI

Shift In (Input)

The SI pin provides an input path for serial shift scan diagnostics. This pin must be left unconnected for normal operation.

SO

Shift Out (Output)

SO is the output for shift scan diagnostic data while in TEST mode. This pin must be left unconnected for normal operation.

TEST

Test Mode (Input; Active HIGH)

The TEST pin is used for factory and incoming testing of FORMAC. This pin must be strapped to ground for normal operation.

TOKISD

Token Issued (Output; Active HIGH)

The TOKISD pin indicates that the FORMAC issued a restricted or non-restricted token. The pin goes HIGH for one BCLK cycle when the token End Delimiter is placed on the X-bus.

$\overline{\text{XDAMAT}}$

External Destination Address Match (Input; Active LOW)

This input provides a means for additional destination address detection outside of the FORMAC. In order to ensure proper setting of the A_indicator and correct FSHRCVF operation, $\overline{\text{XDAMAT}}$ assertion must occur during a specific window of the frame arrival on the R-bus. This window begins on the third byte following the frame start delimiter and ends on the fifth byte of the information field.

$\overline{\text{XSAMAT}}$

External Source Address Match (Input; Active LOW)

This input provides a means for additional source address detection outside of the FORMAC. $\overline{\text{XSAMAT}}$ causes the received frame to be stripped from the ring. When $\overline{\text{XSAMAT}}$ is asserted, the byte present on the R-bus at the time of assertion and all following bytes of the frame will be stripped from the ring. This pin should be tied HIGH when external address detection is not used.

Power Supply

GND

Ground (Inputs)

There are fourteen GND pins. They must all be connected to the power return.

VCC

Power (Inputs)

There are six Vcc pins. They must all be connected to a +5–V±5% supply.

FUNCTIONAL DESCRIPTION

Overview of User-Accessible Resources

Programmable Resources

Several registers in the FORMAC can be accessed through the NP-bus. Through initialization of these registers, the user can tailor the device to fit a particular application. The instruction bus (R/$\overline{W}$, $INST_{0-3}$) is used as a pointer to select the various internal registers.

Mode Register (MODE)
The FORMAC contains a 16-bit mode register. When reset, the mode register is initialized so that all bits (except MSELRA) are inactive (LOW). The NP can access the mode register using the ILDMODE and IRDMODE instructions.

Address Registers ($ADRS_{0-7}$)
The FORMAC address registers store the node's 48-bit address, 16-bit individual and 16-bit group address, and the station T_Request time value. These registers are organized in a 8-by-16-bit structure that is loaded and read sequentially through the ILDADRS and IRDADRS instructions.

MAC Information Register 1–0 (MIR_{1-0})
The MIR is a read-only register. MIR is used to store the first four bytes of the information field of received MAC frames. MIR is also used to store the first four information bytes of a frame in loopback mode. It can be read with the $IRDMIR_1$ and $IRDMIR_0$ instructions.

Token Rotation Timer (TRT)
The TRT is used to implement the timed token access protocol specified by FDDI and determine certain error conditions on the ring. It can be read from or written to under processor control. The upper 16 bits of the TRT timer can be read directly with the IRDTRT instruction. The lower 5 bits are read with the IRDTLSB instruction. A single instruction, ILDTRT, loads the entire 21-bit TRT register, filling the upper 16 bits with the value stored in TMAX and writing "0s" into the lower 5 bits.

Timer Default Maximum (TMAX)
TMAX specifies the default token rotation time to be used during ring initialization and recovery. It is also used to hold a default TRT (TMAX) during the claim token process. This 16-bit register is loaded using the ILDTMAX instruction and read using IRDTMAX.

Valid Transmission Timer (TVX)
The 8-bit TVX counts the time between valid frame transmissions on the ring. If the time exceeds the value loaded into TVX at initialization, then ring recovery will occur. Loading TVX (using the ILDTVXD instruction) writes the default number into a latch. Reading TVX (using the IRDTVXT instruction) places the TVX timer value on the most-significant byte of the NP-bus, and the previously written latch value on the least-significant byte of the NP-bus.

Negotiated Token Rotation Time (TNEG)
This 21-bit register stores the lowest 21 bits of the bid field of a received Higher Claim or My Claim frame. When the ring becomes operational, this register represents the winning value of the claim process. The upper 16 bits of TNEG can be read with the IRDTNEG instruction. The lower 5 bits are read with the IRDTLSB instruction.

Status Register (STAT)
STAT is used to report error and operational conditions to the NP. Individual bits in the status register can be used to generate interrupts to the NP. Status is a read-only register which can be read using the IRDSTAT instruction.

Interrupt Mask Register (IMSK)
The FORMAC contains a 13-bit register used to control maskable interrupts. This register can be written and read via the NP-bus using the ILDIMSK and IRDIMSK instructions.

Frame Status Register (FRSTAT)
Frame status is generated and appended to the end of all frames when they are transferred to the YR-bus. Frame status is recognized by the DPC through a special handshake sequence. The DPC stores this byte (as external status) in the received frame header in the Buffer Memory.

State Machine Register
The state machine register is a read-only register that contains the states of the machines as described in the FDDI MAC protocol specifications. It can be read using the IRDSTMC instruction and the NP-bus.

Asynchronous Priority Register (TPRI)
The TPRI register is used to control the priority of asynchronous messages. The value of TPRI is compared with TRT or THT. This register can be loaded from the NP-bus with an ILDTPRI instruction or read with an IRDTPRI instruction.

Instruction Set

The NP can issue software instructions to the FORMAC using the $INST_{0-3}$, $R/\overline{W}$ and NP_{0-15} lines. $INST_{0-3}$ are normally connected to the address bus of the NP.

Hardwired Resources

The FORMAC provides two strap options that configure the FORMAC for special functionality. The FULL pin is used to select full-duplex operation at the FORMAC Y interface. The BMODE input can be strapped to V_{CC} for synchronous operation of the NP-bus.

Block Diagram

External Buses

Seven buses are provided to interface the FORMAC with external hardware. The NP-bus provides a path for initialization and control of the chip. Associated handshake logic permits asynchronous communication over the NP-bus. The NP-bus can also be programmed for synchronous operation.

The two Y-buses are used to interface to the DPC. The YR-bus is the output for frames received from the media. The YT-bus is the input for data to be transmitted on the medium. Y-bus handshake logic provides control signals for data flow between devices. In addition, data on both YR- and YT-buses is protected with a parity signal.

The RA-, RB-, and X-buses comprise the FORMAC interface with the physical layer. Data received from the media is input via the selected R-bus. A MUX at the input of the FORMAC permits selection of the active R input bus. Data is sent to the media over the X-bus. Again, parity is provided on both buses.

Finally, an instruction bus input ($R/\overline{W}$, $INST_{0-3}$) is used to select between read and write operations on the different registers within the chip.

MUX1

A MUX is provided at the input to the FORMAC to select the input to the receiver logic of the chip. Under normal operation, the MUX is used to select one of the R-buses as an input to the FORMAC. A HIGH MSELRA bit in the mode register selects the RA-bus as the chip input. MSELRA LOW selects RB. This control is provided to facilitate ring re-configuration.

There is a case when neither R-bus is used as the FORMAC input from the media. This occurs when the FORMAC is programmed for internal loopback; the FORMAC X-bus is used as the input to the chips internal receive path. This is useful for "in-circuit" testing of the FORMAC and associated hardware before a station is placed on the ring. When internal loopback is selected, data input on the RB- and RA-buses is ignored.

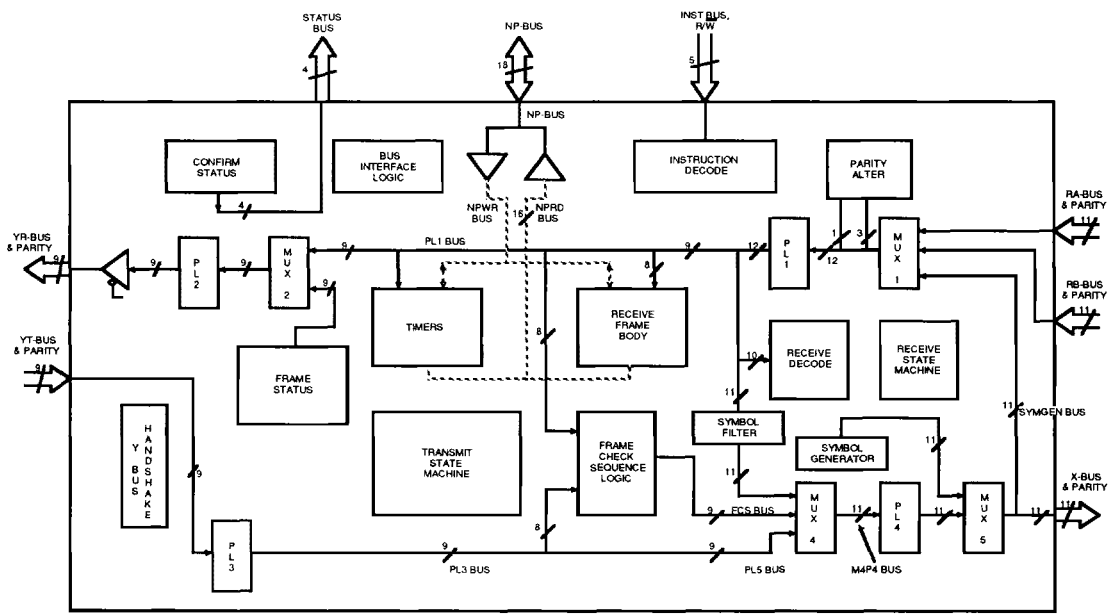


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Figure 1. FORMAC Detailed Block Diagram

Pipeline1

Pipeline1 captures received data and brings it onto the internal PL1– bus. This latching allows appropriate setup time for decoding the frame control and address field of incoming frames.

Parity Alter

The parity alter logic changes the parity system used by the FORMAC. Odd parity is normally used on the selected R-bus, RCU, and RCL input signals. This parity system is altered to reflect odd parity on only the R-bus information, by setting input parity based on the state of the RCU and RCL signals. Thus, bad parity received on the RP input will yield bad parity output from this logic.

Receive Frame Logic

This block of logic consists of three basic elements. First a decoder is provided to interpret the frame control and other special symbols in the incoming frames. Frame validity logic within this block checks each frame against the FDDI criteria. Finally, the receive state machine is included in this block. The receive frame block provides many of the global signals used throughout the chip.

Receive Frame Body Logic

This logic sets the flags required for address detection and token claiming. The addresses and requested token time associated with the FORMAC are stored in registers within this block. An ALU compares these stored values with the address and T_Bid_Rc fields of received frames. A state machine within the block selects the proper address for comparison. The receive frame body logic uses the inputs from the receive frame logic block to determine the type of address being received (i.e., long/short, individual/group). The flags that are set by this block are used by the transmit state machine and the symbol generator. The flags are also input to the Y-bus handshake block where they are used to generate some of the FORMAC–DPC interface signals.

Timers

The timer block contains the timers and registers required for the timed token protocol of FDDI. Three timers are contained within this block. The TVX timer is used to check the time between End Delimiters on the ring. Should TVX exceed the value programmed by the user, ring recovery is initiated through the claim process. The TVX timer is an 8-bit timer clocked once per 255 clock cycles. The TVX timer is loaded with the 8-bit TVX default value every time a valid frame of unrestricted token is received by the FORMAC. An instruction is provided to force the default value into the timer. The timer is also loaded each time the mode register is programmed to exit initialization mode.

The TRT timer counts the time between receipt of tokens. If the TRT exceeds 2 times the operative token rotation time (2 x TOPR) for the network, recovery action is required. When the ring is operational, TOPR will be the time negotiated through the claim process and is stored in TNEG. During ring initialization and recovery, TOPR is equal to the default value called TMAX. TMAX can be loaded directly via the NP-bus. Loading of TRT with TMAX can also be forced by an instruction. In addition, TRT is loaded with TMAX everytime the FORMAC is programmed to exit the initialization mode.

The third timer, the THT or token holding timer, controls the length of time that the node can hold a token for the purpose of transmitting A-frames. Functionally, THT can be thought of as a down counter. THT is loaded when the FORMAC captures a token. The value loaded is the difference between the time the FORMAC expected to capture a token (TOPR) and the actual time it took for the token to circulate the ring. If this is greater than the value loaded into TPRI (i.e., the token was received sooner than expected), the FORMAC can transmit asynchronously. The FORMAC can continue to transmit A-frames until the THT falls below the TPRI value. Both TRT and THT are implemented as 21-bit counters providing one BCLK resolution.

Bus Interface Logic

This block of logic controls the handshake pins required to interface the FORMAC with the NP.

Instruction Decode

The instruction decode logic decodes the instruction bus. The decoded outputs are used internally as pointers and control signals.

Status/Mode/Interrupts

This block is comprised of the status, mode, and interrupt logic. The status logic allows for error reporting to the NP. This status information can be read directly or reported using maskable and non-maskable interrupts. The mode register allows the NP to control the operation of the FORMAC.

Frame Status

This block is used to map the frame status (FS) of a received frame and other pertinent information into an 8-bit register. The R and S symbols received after the End Delimiter of the frame are decoded as a zero and one, respectively. The contents of the frame status register are appended to the receive frame and passed to the DPC.

MUX2

MUX2 is used to append the frame status byte to the frame being sent out to the Y-bus. The MUX will output data from the PL1-bus, while received FC and INFO data is contained internally. After the last byte of information has passed through the MUX, it will switch to select the receive frame status register.

Pipeline2

Pipeline2 latches the received frame information being sent out on the Y-bus. This ensures sufficient setup time at the FORMAC-DPC interface.

Confirmation Status

This block is used to confirm the received status of frames originating at the station associated with the FORMAC.

Transmit State Machine

This block implements the transmit state machine outlined in the FDDI MAC specification.

Y-bus Handshake

The Y-bus handshake logic controls all signals required to interface the FORMAC to the DPC.

Pipeline3

This pipeline latches frames before they are transmitted onto the FORMAC internal transmit path. This allows adequate setup time for the frame check sequence logic.

Frame Check Sequence (FCS)

This logic checks the FCS of received frames and generates FCS for transmitted frames. A MUX steers either the PL1 (internal receive) or the PL3– (internal transmit) bus into the CRC logic. The MUX normally selects the PL1-bus when the FORMAC is in the repeat or idle modes. When the FORMAC enters one of the transmit states, PL3 is selected. The CRC is calculated using a 32-bit Autodin II polynomial as specified by the FDDI MAC specification.

MUX4

MUX4 selects one of three different sources to be output on the X-bus. These sources are the output of the symbol filter, the FCS logic, and the PL3-bus.

Symbol Filter

The symbol filter logic alters the E_, A_, and C_indicators on repeated frames as specified by the FDDI standard.

Symbol Generator State Machine

This logic generates the command symbols required for transmission on the media. These include idle symbols for preamble, as well as the set/reset and End Delimiter symbols appended to transmitted and repeated frames. This logic is also used to generate the tokens when they are issued.

MUX5

MUX5 selects between the internal transmit and repeat paths and the symbol generator output for transmission onto the X-bus.

Pipeline4

Pipeline4 guarantees ENDEC setup time.

Operational Modes

This section describes the various control tasks performed by the FORMAC. The operation is broken down to three basic modes. Initialization mode is entered upon reset. On-line enables the receive and transmit state machines for operation on the ring. The four modes of loopback permit node self-test before entering the on-line state. Selection of these modes is performed through the mode register.

Initialization

The initialization mode is indicated by three zeros in the MMODE bits in the mode register. This mode is automatically entered on a pin or software reset. In this mode, the receive and transmit state machines are locked in the reset condition. The network data path is locked in a "blind repeat" configuration. In this fashion, data input to the selected R-bus is repeated on the X-bus with no protocol processing.

The FORMAC address registers can only be written and read properly with the chip in initialization mode. Although the timer default values can be written in any mode, changing these ring parameters while on-line may lead to undeterministic behavior. Network events can occur asynchronous to the loading of the registers. The timers can be loaded with the default at any time. The user cannot determine if the timer is operating with the new or old default time.

During initialization mode, no receiver protocol is executed. When the chip is placed in this mode, certain ring events such as claim or beacon frames may be missed. Thus, a FORMAC leaving the initialization mode may not be operating with current parameters such as the negotiated token rotation time for the ring. Also, the Claim/Listen and Beacon/Listen instructions do not operate in the initialization mode.

Even though the transmit state machine will not process the information, the internal timers (TRT and THT) continue to operate. This permits rough timer checkout before going on-line. On reset, TVX is loaded with its terminal count value. This timer, during non-initialization operations, will expire in 255 clock cycles. Status is set accordingly. TVX will stop once expired until it is reloaded.

TRT and THT are cleared on reset. They expire in 2_{21} BCLK cycles. THT will stop when the terminal count is reached. TRT will reload with the current TMAX value and resume counting.

All counters resume sequencing when reloaded. Reloading can be forced with the instruction commands provided. These instructions can be used with the timer expiration bits in the status register to verify timer operation against "soft" timers during power on confidence testing of the node hardware. It should also be noted that the timers are loaded with their default values when the Mode register MMODE bits are programmed to exit the initialization mode.

On-Line

The on-line mode is entered by writing the appropriate bit pattern to the MMODE bits. When this mode is entered, the FORMAC performs the operational sequences required for the FDDI. The chip exits the on-line mode if the MMODE bits are altered or a chip reset occurs. The on-line sequences can be examined further by investigating the functions of the chips receiver and transmitter.

Receiver

When "on-line" the FORMAC continually processes the incoming symbol stream as per the FDDI receiver state machines. The actions of the receiver can be further categorized. The fundamental actions are frame reception and frame repetition control. The receiver also controls some special function outputs that are used to log ring statistics, support external addressing and provide general status information.

Frame Reception. Frame reception refers to the action of placing network data on the YR-bus and setting the control signals on the bus accordingly. There are four basic actions that can occur when the head of a frame is received from the selected R-bus. First, normal frame reception can occur. This case is illustrated in Figure 2. Here the RECEIVE and DAVALID outputs from the FORMAC go HIGH as the YR-bus is activated. DAVALID goes LOW after the last byte of the frame is output. RECEIVE stays HIGH. In the next cycle, DAVALID goes HIGH while RECEIVE drops, indicating that the contents of the frame status register have been placed on the YR-bus.

The second case of frame reception is the flushed frame. There are two criteria for flushing a frame. First, flush occurs at the end of a properly formed frame when the address matching criteria are not met. The address match criteria includes the internal and external address match decisions and the state of the MDELADET and MADET bits in the mode register. The frame will also be flushed if the frame ends on an uneven byte boundary. Figure 3 illustrates a case of a flush due to an address mismatch. If no valid address match occurs (either internal or external) by the fifth byte of the frame following the SA (when MDELADET = 0), FSHRCVF is asserted.

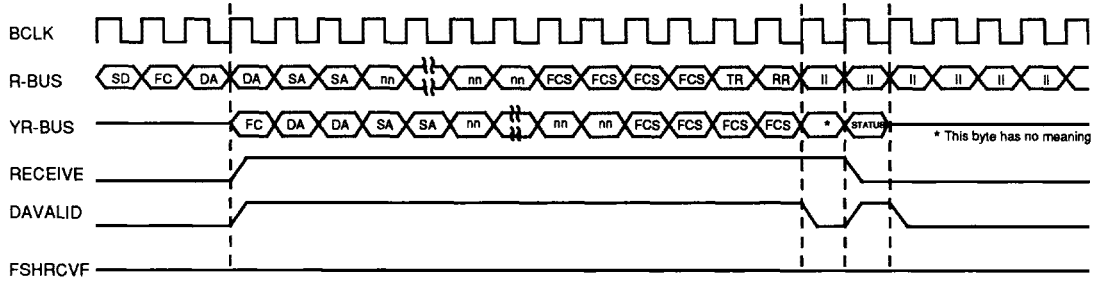

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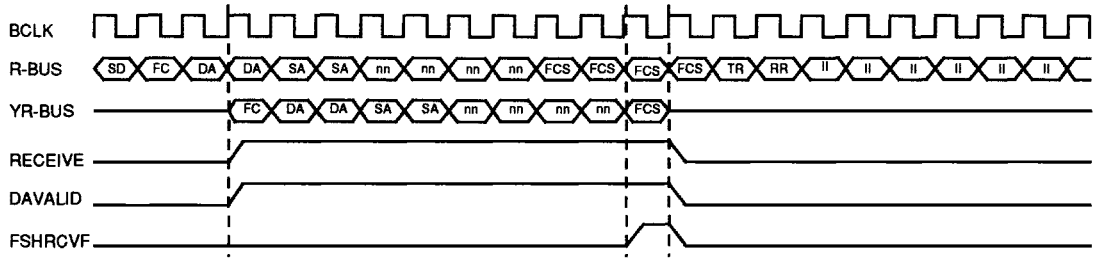
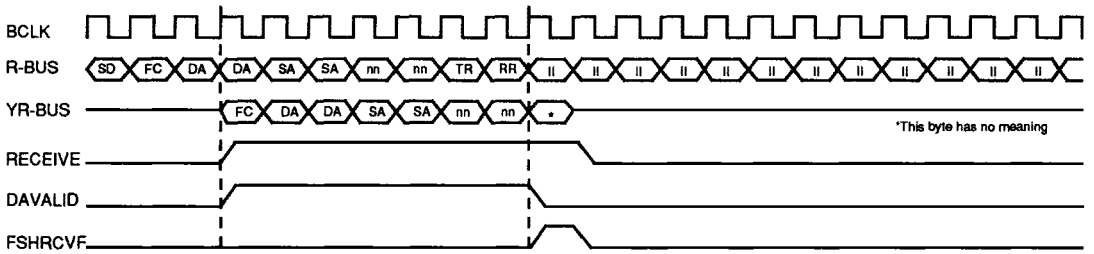
Figure 2. Normal Frame Reception



(Case A) Flush on Address Mismatch: frame with 5 or more data bytes following SA field boundary and MDELADET = 0



(Case B) Flush on Address Mismatch: less than 5 data bytes following SA field boundary or when 5 or more data bytes follow SA field and MDELADET = 1

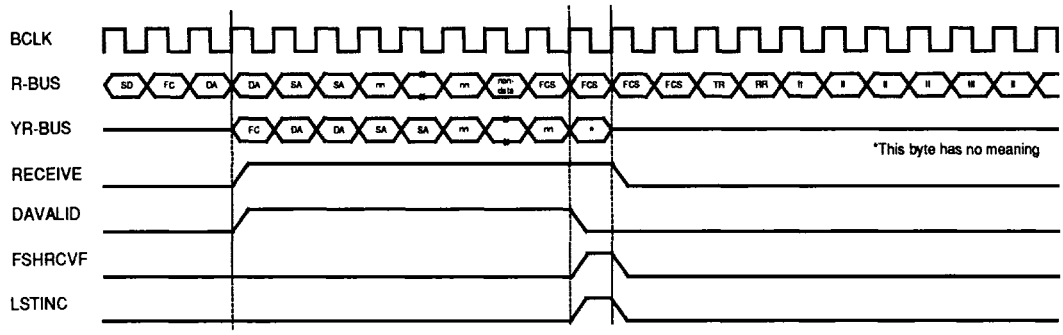
09731-007B

Figure 3. Flush Cases A and B

FSHRCVF is also asserted during reception of a stripped or lost frame. Stripped frames are frames that were partially repeated by a node. Before the End Delimiter is repeated, the node began to transmit idle. The resultant symbol stream is referred to as a stripped frame. A lost frame is one whose symbol stream is corrupted so that a symbol encountered after the Start Delimiter results in a non-data, non-End Delimiter symbol. These frames are flushed in a similar fashion to the stripped frame case. This is illustrated in Figure 4.

The next case that needs to be examined are those of non-reception. In these cases, the RECEIVE, DAVALID and YR-bus outputs never go active. In order to activate these signals, the receive state machine must be in the awaiting SD state. A valid Start Delimiter followed by two data symbols must be received. The two data symbols are interpreted as the frame control (FC) field. If FC indicates a claim frame or token, frame reception will not occur. If all criteria have been met, the state of the transmitter must be considered. The transmitter must be in the idle or repeat states for frame reception. The only exception is when the FULL strap option is tied HIGH. Finally, reception will not occur if the mode register is programmed to disable receive.

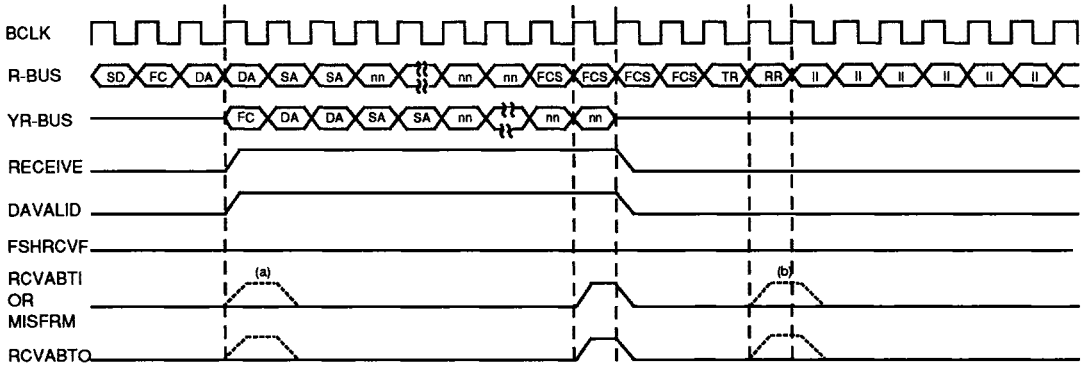
The final case of frame reception deals with the frame abort action. This action is indicated in Figure 5. The abort action occurs when the RCVABTI or MISFRM inputs are activated within the proper time periods shown. The abort action also occurs if the FORMAC enters a non-repeat, non-idle transmit state during frame reception or the disable receive mode register setting is programmed while frame reception is taking place.



Flush on stripped or corrupted frame

09731-008B

Figure 4. Flush Case C



Note:

MISFRM/RCVABTI will be processed correctly at cycle times from (a) and (b).

09731-009B

Figure 5. RCVABTI/MISFRM Reception

Frame Repetition. Frames received on the selected R-bus are repeated on the X-bus. In a normal case the entire frame is repeated with the frame status (FS) indicators modified according to the FDDI specification. The FORMAC transmitter can leave the repeat mode for several reasons. When this occurs, the frame received at that time is said to have been stripped.

One primary cause for stripping is the recognition of a frame whose source address (SA) equals the nodes corresponding address (my address or MA)(when comparing the receive source address against MA, the most-significant bit of the address is ignored). This is the mechanism for removing frames once they've circulated the ring. An example is illustrated in Figure 6–a. Stripping also occurs when a lost frame is encountered. The byte containing the offensive symbol as well as all subsequent bytes are removed from the ring. This case is illustrated in Figure 6–b. Tokens are also stripped when the FORMAC decides to capture. In this case, only the Start Delimiter of the token is repeated on the X-bus.

Frame status indicators are repeated, stripped, or modified according to the FDDI protocol. The FORMAC will repeat an infinite number of symbols following the frame provided they are properly formed. The first control symbol encountered must be a "T" in the most-significant nibble of the R-bus. This signifies termination of the frame. If the first control character encountered is a "T" in the least-significant nibble, the frame has an uneven number of symbol pairs. The octet containing the "T" is repeated and all subsequent indicators are stripped. In a properly formed frame, the "T" is present in the most-significant nibble of the byte. The symbol after the "T" in the least- significant nibble is the error indicator. The error indicator received should be an "S" or "R" symbol. If the error indicator is not an "S" or "R", an "S" is assumed and the FORMAC will assume that frame status (FS) reception is complete. The FORMAC will recover the missing error indicator by transmitting an "S". Aside from the error indicator, no other indicator will be recovered. If a byte of FS is received with a non-"S" or "R" symbol in the most-significant nibble or non-"S", "R", or "T" symbol in the least-significant nibble, FS processing is completed. That byte and subsequent bytes of status are stripped.

Frames are not repeated when the FORMAC transmitter is in the transmit data, issue token, claim, or beacon states.

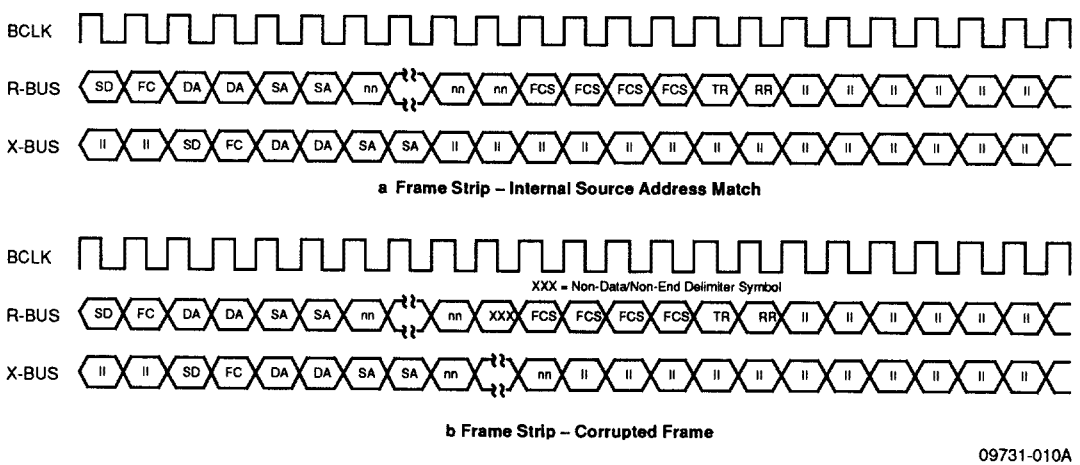


Figure 6. Frame Stripping

Special Function Operation. The FORMAC receiver processes additional status information that is output via some special function pins. Special inputs are available to allow the user to supplement the FORMAC's internal address detect logic with additional hardware. This section covers the operation of these pins.

Figure 7 illustrates the relative timing of the SDRCVD, LNGADR, $\overline{\text{FSVLD}}$, EOUT, AOUT, COUT, ERRINC, FRINC, and S_{0-3} outputs to the received symbol stream. SDRCVD goes HIGH indicating a valid Start Delimiter is received. The LNGADR output retains the state of the last frame until the new SD is received. $\overline{\text{FSVLD}}$, along with the E/A/COUT pins, goes HIGH at the end of frames whose SA = MA. $\overline{\text{FSVLD}}$, EOUT, AOUT, and COUT go HIGH after the byte containing the A_ and C_indicators is received. The FRINC and ERRINC go HIGH when the ED is received. The S_{0-3} pins go HIGH when the first byte of non-status information is received.

Figure 8 shows the operation of SDRCVD, LNGADR, and S_{0-3} with relation to a token. In this case, the LNGADR output changes to reflect the type of token rather than the address length.

External address detection is illustrated in Figure 9. This figure shows the standard case for address detection with the solid lines. Either the $\overline{\text{XDAMAT}}$ or $\overline{\text{XSAMAT}}$ inputs can be set as early as indicated by note 1. This is the third byte following the SD on the R-bus. Although the FORMAC can handle this case, it may be difficult to achieve since the DA is still being received in the 48-bit case and the SA has not yet begun.

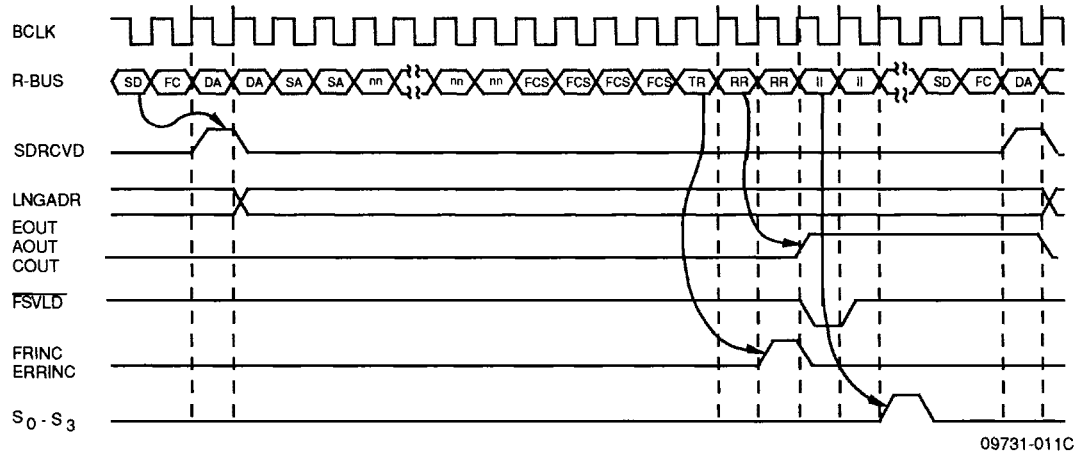


Figure 7. Special Function Outputs for Frame Reception

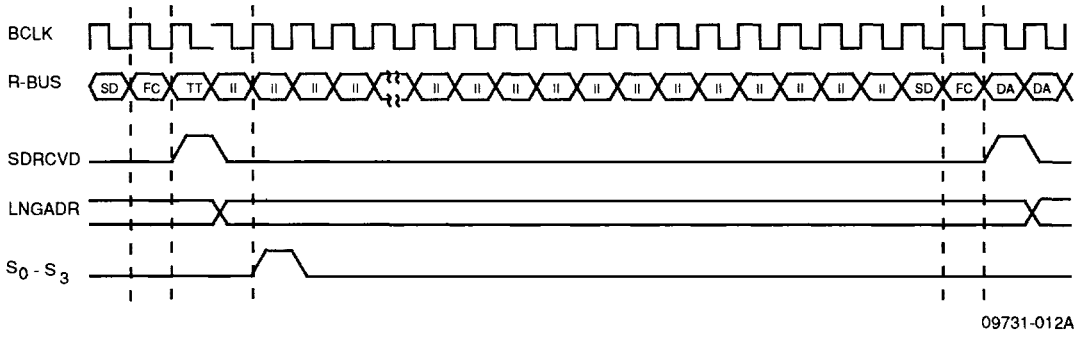


Figure 8. Special Function Outputs for Token Reception

The XSAMAT input can come as late as the appearance of the End Delimiter on the R-bus (shown as 2 on Figure 9). There is an important issue to consider regarding the timing of the XSAMAT pin. The XSAMAT will result in a stripping action beginning with the byte being received on the R-bus at the time assertion. According to the FDDI state machines, stripping for SA = MA frames should begin with the byte following the last SA byte (the solid line timing). Later assertion of XSAMAT, though in violation of the spec, will not cause inoperability problems so long as the End Delimiter is stripped. For stripping of the frame after the SA field, XSAMAT should be asserted in the cycle shown as 4 in Figure 9.

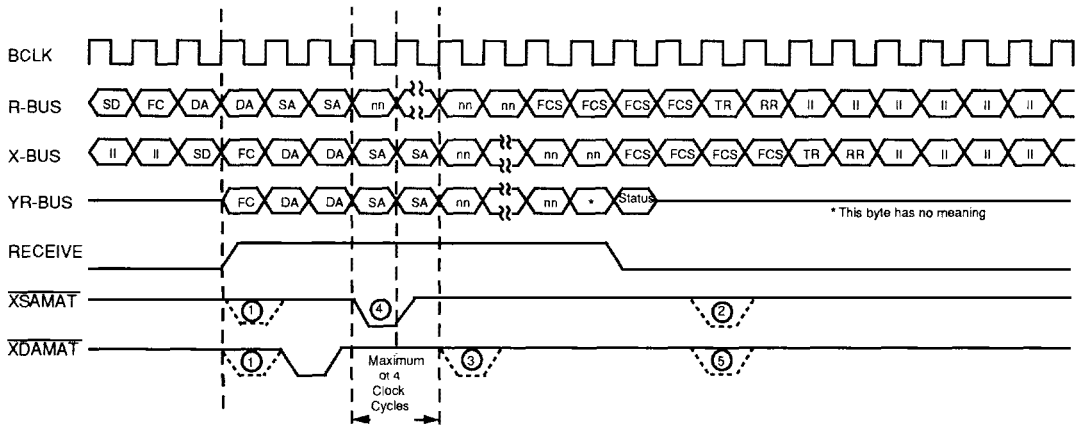
For proper setting of the FSHRCVF pin, based on external address detection, XDAMAT must be asserted in the cycle shown as cycle 3 when MDELADET = 0 or in cycle 2 when MDELADET = 1. If source address matching is being used as a criteria for frame reception (programmed in the mode register), the XSAMAT pin should also be asserted at cycle 3 to prevent the frame from being flushed, when MDELADET = 0, or at cycle 2 when MDELADET = 1.

Transmitter

The FORMAC transmitter controls the timing of node transmission as a result of network activity. The transmitter reacts to timer expiration and received MAC frames to queue the claim and beacon frames. The transmitter controls the node's flow of data by indicating XMEDAVS or XMEDAVA as a result of token capture. The transmitter makes capture and pass decisions based upon the state of the MEDREQ inputs and token control register when the token is received.

The FORMAC asserts XMEDAVA and XMEDAVS based upon the corresponding request and the timer values. Only one XMEDAV output will be HIGH at a given time. XMEDAVS is given priority when conditions indicate that both S- and A-frames can be transmitted. When XMEDAVS is asserted, the THT timer is held. This keeps the S-frame transmission from eating into the A-frame bandwidth. The FORMAC re-evaluates the decision to transmit each time the RDYTBYT input goes LOW. If a MEDREQ input remains HIGH, the FORMAC will check the token holding criteria to determine whether another frame can be sent (see FDDI spec).

The FORMAC transmitter enters the transmit idle state when reset.



1 Earliest allowed assertion
2 Latest allowed assertion still stripping 'ED'
3 Latest allowed assertion suppressing FSRCVF and setting A_ indicator (if MDELADET = 0)
4 Latest allowed assertion still stripping after SA
5 Latest allowed assertion suppressing FSRCVF and A_ indicator (if MDELADET = 1)

09731-013B

Figure 9. External Address Detection

Frame Transmission. Figure 10 gives an example of a transmitted frame. The XMEDAVS or XMEDAVA is asserted based on a corresponding MEDREQS or MEDREQA. The delay from the request to the acknowledgement is based on the time required to capture a token. Once XMEDAV is given, the FORMAC waits for RDYTBYT input. RDYTBYT guarantees a continuous frame is available at the YT-bus for transmission. The FORMAC will wait to assert XFRBYT, if required, to ensure that at least 8 bytes (16 symbols) of preamble have been transmitted.

The FORMAC will encapsulate all bytes input on the YT-bus when XFRBYTE and RDYTBYT signals are active. An SD is output on the X-bus immediately prior to transmission of the first YT byte. The frame check sequence (FCS) is appended after the last byte given on YT. FCS will not be appended if the MNFCS bit is set in the FORMAC mode register. After the FCS field, a "T" and "R" symbol are output on the most- and least-significant nibble of the X-bus, respectively. This is the frame's End Delimiter and error status indicator. This is followed by two more "Rs" for the address and copy indication.

In Figure 10, the frame transmitted is the final frame in the queue. This is determined by the MEDREQ going LOW with RDYTBYT. Figure 11 gives the case where another frame should be transmitted from the queue. Here MEDREQ remains HIGH. The FORMAC will lower XMEDAV as a result of RDYTBYT going LOW. If the network conditions for sending another frame can be met, XMEDAV is asserted in the next cycle.

A transmit abort is indicated by the XMTABTI input pin going HIGH. In this case, the next byte to be placed on the X-bus is replaced by idle. The FORMAC transmit state machine will be reset to the idle state. XMTABTI is asserted in the cycle after MEDREQ (S or A) and RDYTBYT are lowered. This case is given in Figure 12.

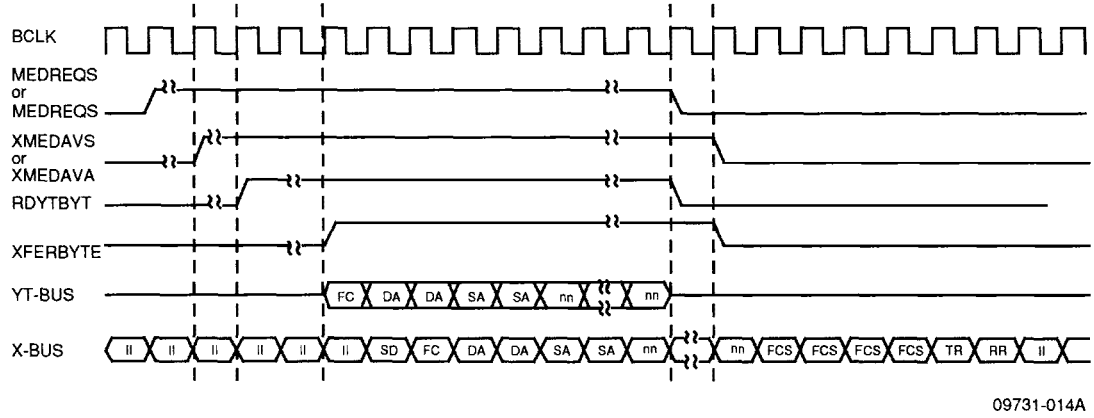


Figure 10. Frame Transmission: Last Frame on the Queue

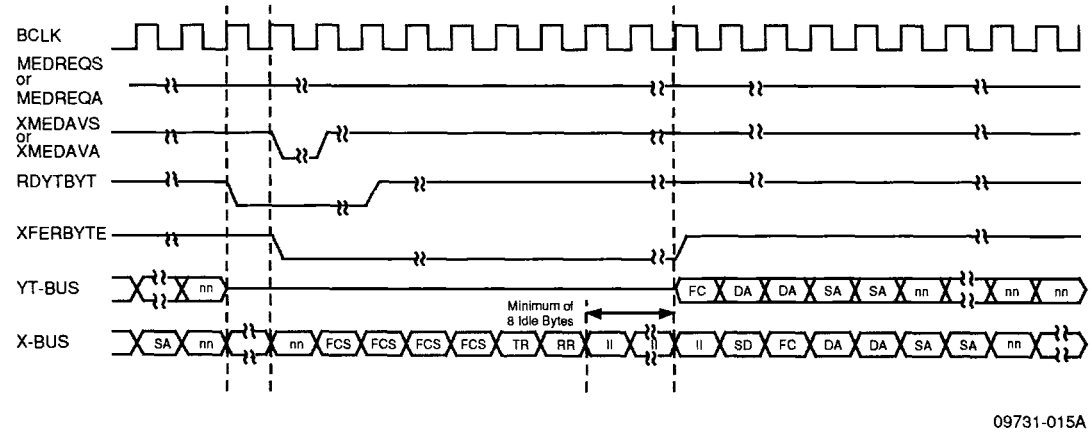
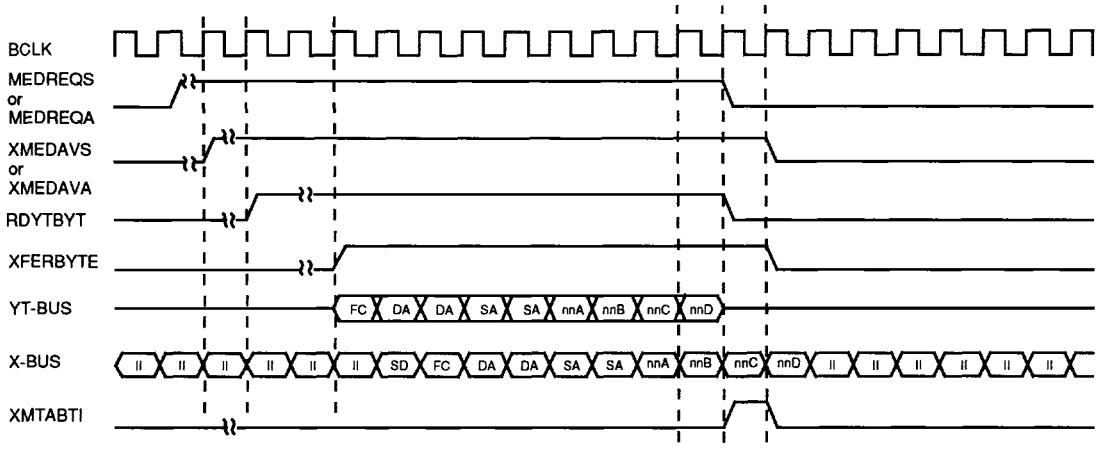
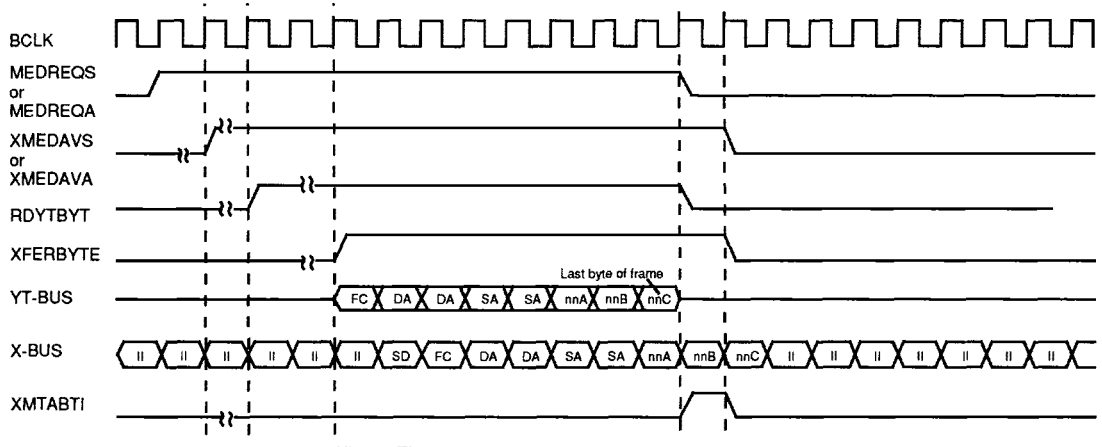


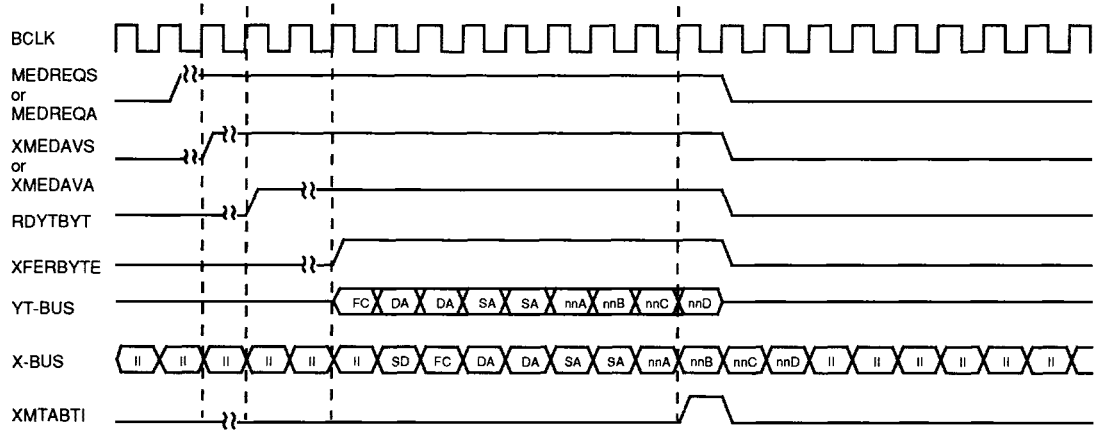
Figure 11. Frame Transmission: Another Frame



a) XMTABTI due to NP instruction to the Am79C82A



b) XMTABTI due to parity error during data read



c) XMTABTI due to parity errors during pointer read, descriptor read, or transmit FIFO underflow, or coding errors in pointers or descriptors

09731-016B

Figure 12. Frame Transmission: Transmit Abort

Recovery Operation. The FORMAC transmitter can go into recovery based upon frames received, instructions from the NP, and timer expiration. There are two recovery states specified in the FDDI. These are the claim and beacon states. Claim is used to negotiate the operative time for token rotation and determine which node will issue the token. Beacon is used to guarantee ring integrity by verifying the path of the ring.

Claim and beacon state can be entered at any given time. Once claim or beacon is entered, the FORMAC must respond by placing the corresponding claim or beacon frames on the X-bus. The FORMAC signals the claim or beacon state so that the proper frame can be queued for transmission. This is shown in Figure 13.

The INICLBN will go HIGH for one cycle indicating the *claim or beacon state has been selected. The exact* state is determined by the CLM/$\overline{\text{BEC}}$ output. This pin is HIGH the entire time the FORMAC is in the claim state. If INICLBN is asserted and CLM/$\overline{\text{BEC}}$ is LOW, the FORMAC has entered the beacon state. INICLBN can be asserted in the middle of a transmission. This is shown in the figure with the dotted lines. In this case, INICLBN acts like an abort of frame.

The FORMAC can go from claim to beacon or beacon to claim. Each of these transitions result in assertion of INICLBN. When the FORMAC exits claim or beacon to return to the idle state, XMTABTO is asserted.

Loopback

Loopback mode is useful for "in-circuit" testing of the FORMAC and associated node hardware before insertion on the ring. loopback operation can be performed four ways. First, loopback can be categorized as internal or external. If internal loopback is selected, the FORMAC's X-bus is connected internally to R-bus input. Data on the RA– and RB-buses is ignored. If external loopback is selected, the loopback connection is assumed to be outside of the chip boundary.

Both internal and external loopback testing can be performed in two different manners, making four possible loopback modes. With loopback 1 selected, the data received will not be output on the YR-bus. In this fashion, the shared YT–/YR-bus can be used for transmit only. When the FORMAC is programmed for loopback, the first four bytes following the frames source address field are stored in the two MAC information registers (MIR). These two registers can be read from the NP-bus. This operation permits limited loopback testing without additional hardware.

With loopback 2 selected, the FORMAC writes the entire received frame to the YR-bus. This data can be received by a dedicated receive DPC (in a two DPC/RBC full-duplex system). If a full-duplex system is not used, an external bus transceiver on the YR-bus and a high-speed FIFO can be added to support loopback. The LPBEN output pin is provided to facilitate this feature.

The internal timers are held during loopback mode. This prevents the FORMAC from entering a recovery state due to a time-out. While in loopback mode, the transmit immediate instruction should be used to allow the FORMAC transmitter to enter the transmit data without capturing a token. This instruction is normally used by station management (SMT) when ring operation is off.

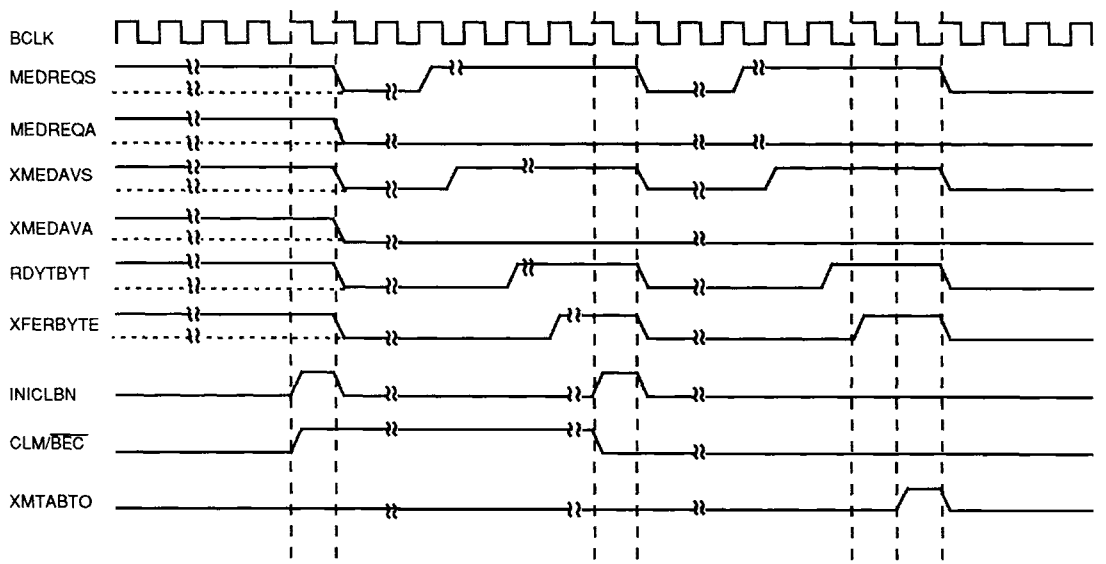


Figure 13. Recovery Operation

HOLD$_1$ Operation

HOLD1 acts as a suspended/resume feature. Bytes received in the cycle following HOLD$_1$ assertion are ignored. Transmission is temporarily suspended by assertion of HOLD$_1$. See Figures 14 and 15.

HOLD$_1$'s use is outside the scope of FDDI. It is useful for the development of hybrid FDDI rings using a time-division multiplex approach to incorporate circuit and packet switch operation.

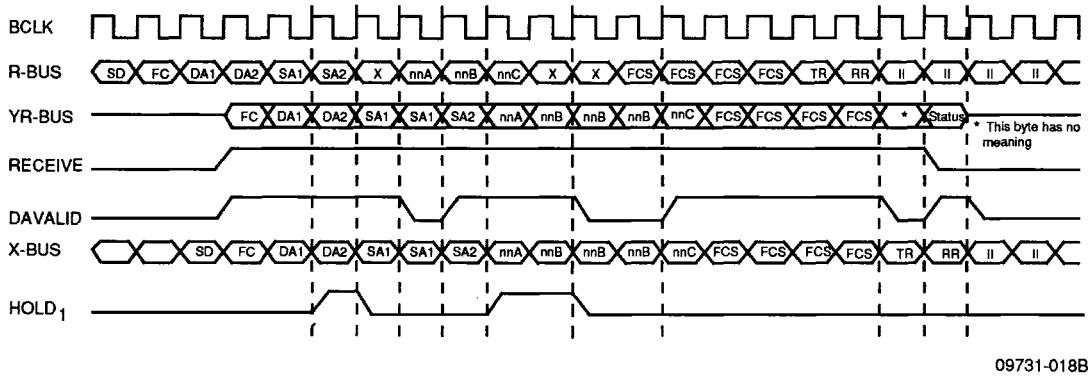


Figure 14. HOLD$_1$ Operation: Frame Reception

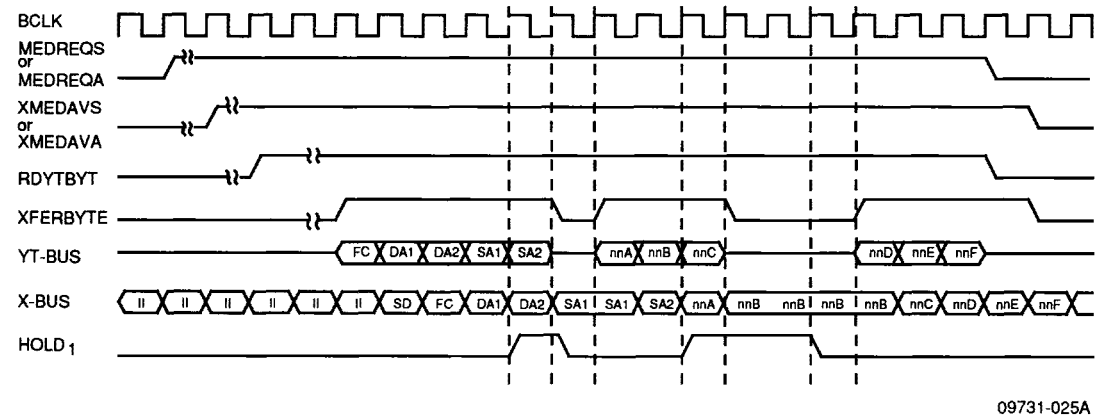


Figure 15. HOLD$_1$ Operation: Frame Transmission

FORMAC Programming

There are two basic methods for controlling operation of the FORMAC. First, programming the FORMAC mode register sets a variety of operational parameters. Secondly, the instruction bus input is used directly in certain instances to control dynamic operation of the chip.

Mode Register (MODE)

The mode register is used to program FORMAC operational parameters and is shown in Figure 16. All bits with the exception of MSELRA are reset to zero on $\overline{\text{RESET}}$ assertion or an instruction to reset. All unused bits are reserved and should be programmed to logic "0". The bits within MODE are as follows:

$MMODE_{0-2}$ ($Mode_{0-2}$)
The three mode bits control the operational mode of the FORMAC. The bit assignment is as follows:

$MMODE_2$	$MMODE_1$	$MMODE_0$	Description
0	0	0	Initialize
0	0	1	Reserved
0	1	0	Reserved
0	1	1	On-Line
1	0	0	Internal Loopback 1
1	0	1	Internal Loopback 2
1	1	0	External Loopback 1
1	1	1	External Loopback 2

Initialize. Initialize is the reset mode of the FORMAC. Initialize mode is used to read and write many of the internal registers in the FORMAC.

On-Line. On-line mode places the FORMAC in the FDDI operational mode.

Internal Loopback 1. Internal loopback 1 places the FORMAC in internal loopback mode. The internal transmit bus is connected to the chip's internal receive path. R-bus inputs are ignored. In this mode, the LPBEN pin is asserted.

Internal Loopback 2. Internal loopback 2 operates exactly like 1 with the exception of the receiver operation. With the 2 setting, data received in loopback mode will be output on the YR-bus. Again, LPBEN is asserted when this mode is entered.

External Loopback 1. This setting places the FORMAC in external loopback mode. LPBEN is arrested in this mode.

External Loopback 2. External loopback 2 is analogous to the internal loopback 2.

MUSESA (Mode to Use Short Address)
This mode bit is used by FORMAC in the token claiming procedure. This bit should be set to one if the addresses transmitted in the node's claim frames are 16 bits long. Otherwise, MUSESA is reset. It is important that the MUSESA bit, the address length bit in the FC fields of the claim and beacon frames stored in Buffer Memory, and the actual address lengths used in the claim and beacon frames all be consistent. Otherwise the claim process may never finish.

MDELADET (Mode Delayed Address Detection)
MDELADET selects the delayed address detection. If MDELADET = 1, external DA detection is accepted until the End-Delimiter is received. If MDELADET = 0, and if DA does not match within four BCLKs after SA is received on the R-bus, the frame is flushed from the Buffer Memory.

MDISRCV (Mode to Disable Receive)
With disable receive set, the FORMAC will not send frames on the YR-bus.

$MADET_{0-1}$ (Mode Address Detect)
The MADET bits select the conditions which inhibit the FSHRCVF signal during frame reception on the YR-bus. These bits are decoded as follows:

$MADET_1$	$MADET_0$	Description
0	0	DA = MA
0	1	DA = MA or SA = MA
1	0	Promiscuous
1	1	Reserved

DA = MA. In this setting, the FORMAC will assert FSHRCVF when the destination address of the received frame does not match the corresponding source address in the FORMAC and the XDAMAT input is not asserted during frame reception.

DA = MA and SA = MA. In addition to inhibiting FSHRCVF for frames whose DA = MA, the FORMAC will also inhibit the signal for frames it transmitted.

Promiscuous. In promiscuous operation, FSHRCVF is not asserted as a result of destination address mismatch.

Promiscuous. In promiscuous operation, FSHRCVF is not asserted as a result of destination address mismatch.

Reserved. Reserved for future use; should not be used.

MNFCS (Mode No Frame Check Sequence)
This bit allows the user to suppress generation of CRC on transmitted frames. The MNFCS feature is particularly useful for loopback testing.

MSELRA (Mode to Select RA)
MSELRA controls the MUX input to the FORMAC at its interface with the ENDECs. A one in this bit position selects the RA-bus as the active FORMAC media input. A zero indicates RB as the active input. MSELRA retains its state on a chip reset.

MDSCRY (Disable Carry)
MDSCRY is used to test the operation of the internal FORMAC timer. MDSCRY must be cleared for proper FDDI operation.

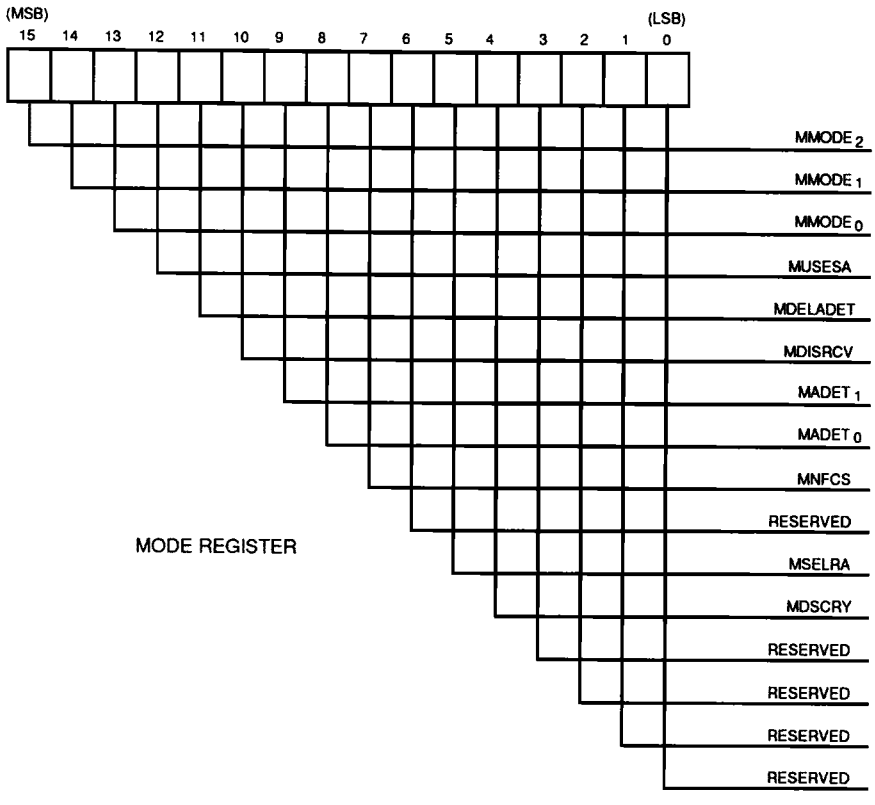


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Figure 16. Mode Register

Instruction Set

The instruction bus of the FORMAC performs two control functions. First, the inputs on R/$\overline{W}$ and $INST_{0-3}$ act as a pointer, selecting the proper internal register for a subsequent read or write operation.

Secondly, the instructions are sometimes used to force the FORMAC into a given state. Table 1 outlines the FORMAC instruction set. The description following Table 1 details the meaning of each instruction. The 5-bit code is given along with a 7-letter mnemonic.

Table 1. FORMAC Instruction Set

Instruction Mnemonic	R/$\overline{W}$	$INST_3$	$INST_2$	$INST_1$	(LSB) $INST_0$	NP_{0-15}	Function
Software Reset:							
ILDSRST	0	0	0	0	0	X X X X	Software Reset
Instructions to Force the FORMAC into a Specific State:							
ILDIDLS	0	0	0	0	1	X X X X	Idle/Listen
ILDCLLS	0	0	0	1	0	X X X X	Claim/Listen
ILDBCLS	0	0	0	1	1	X X X X	Beacon/Listen
ILDRCTL	0	0	1	1	1	W W W W	Restricted Control
ILDSNDM	0	1	0	0	1	W W W W	Send Immediate
Instructions to Load and Read FORMAC Registers:							
IRDTLB	1	0	0	0	0	R R R R	Read LSBs
IRDTNEG	1	0	0	0	1	R R R R	Read TNeg
IRDMIR1	1	0	0	1	0	R R R R	Read MIR_1
IRDMIR0	1	0	0	1	1	R R R R	Read MIR_0
ILDTHTT	0	0	1	0	0	X X X X	Load THT
IRDTHTH	1	0	1	0	0	R R R R	Read THT
ILDTRTH	0	0	1	0	1	X X X X	Load TRT
IRDTRTH	1	0	1	0	1	R R R R	Read TRT
ILDTMAX	0	0	1	1	0	W W W W	Load TMAX
IRDTMAX	1	0	1	1	0	R R R R	Read TMAX
ILDTVXD	0	1	0	0	0	W W W W	Load TVX
IRDTVXT	1	1	0	0	0	R R R R	Read TVX
IRDSTMC	1	1	0	0	1	R R R R	Read States
ILDMODE	0	1	0	1	0	W W W W	Load Mode Register
IRDMODE	1	1	0	1	0	R R R R	Read Mode Register
ILDIMSK	0	1	0	1	1	W W W W	Load Interrupt Mask Register
IRDIMSK	1	1	0	1	1	R R R R	Read Interrupt Mask Register
ICLAPTR	0	1	1	0	0	X X X X	Reset Address Pointer
IRDSTAT	1	1	1	0	0	R R R R	Read Status Register
ILDADRS	0	1	1	0	1	W W W W	Load Address Register
IRDADRS	1	1	1	0	1	R R R R	Read Address Register
ILDTVXT	0	1	1	1	0	W W W W	Load TVX Timer
IRDTPRI	1	1	1	1	1	R R R R	Read TPRI Register
ILDTPRI	0	1	1	1	1	W W W W	Load TPRI Register
Reserved Instructions:							
IRSV1	1	0	1	1	1	—	Reserved
IRSV2	1	1	1	1	0	—	Reserved

Key: W W W W = Write data to FORMAC register
R R R R = Read data from FORMAC register
X X X X = Don't Care

Software Reset

Software reset performs the same function as the $\overline{\text{RESET}}$ pin. Software reset places the FORMAC internal registers and state machines into a known state.

Idle/Listen

This instruction places the FORMAC transmit state machine in the idle state while the receiver enters the listen state. This function is referred to as a MAC_reset in the FDDI specification. It should be noted that timer and register values are unaffected by this operation.

Claim/Listen

This instruction forces the claim state. The TRT is loaded with TMAX when this instruction is given.

Beacon/Listen

This instruction forces the beacon state. The TRT is loaded with TMAX when this instruction is given.

Load THT

This instruction loads the 21-bit THT timer with the value of the TRT timer. This instruction is provided for test purposes and should not be used during normal operation.

Load TRT

This instruction loads the 21-bit TRT timer with the value of the TMAX register. The lower 5 bits are loaded with "0s". This instruction is provided for test purposes and should not be used during normal operation.

Load TMAX

This instruction loads the 16-bit TMAX register with the value of the NP-bus. The TMAX register is used to load the TRT timer when the ring is not operational. The TMAX register represents bits 20–5 of the TMAX time. Bits 4–0 are fixed as zero. When loaded with TMAX, TRT will expire at a time equal to The TMAX value multiplied by the BCLK cycle time. The FDDI default value for TMAX is 165 ms.

Restricted Control

This instruction is used to control use of the restricted token. There are four options that can be selected by the value of the lower two bits on the NP-bus when the instruction is given. The options are as follows:

NP_1	NP_0	Description
0	0	Off
0	1	Exit Restricted Token Mode
1	0	Enter Restricted Token Mode
1	1	Restricted Token Mode

Load TVX Default Value

This instruction loads the 8-bit TVX default value with the lower byte of the NP-bus. The TVX register allows the user to specify the value of the TVX counter. TVX is a single 8-bit register. The value of TVX is the two's complement of the desired number of clocks between 1 and 255 (1 to FF). The TVX timer is clocked at 1/255 the BCLK rate. The FDDI standard specifies a default value of at least 2.5 ms.

Send Immediate

This instruction can be used to start immediate transmission on the media without waiting for a token. Three options are available to select the immediate transmission of data, a restricted token or an unrestricted token. The options are selected by placing following bit combinations on the NP-bus when the instruction is given:

NP_1	NP_0	Description
0	0	Reserved
0	1	Send Unrestricted Token
1	0	Send Restricted Token
1	1	Send the Synchronous Queue

Use of this instruction could violate the FDDI specification. This service is intended for diagnostic purposes.

Load Mode Register

This instruction loads the 16-bit mode register with the value of the NP-bus.

Load IMSK Register

This instruction loads the interrupt mask register.

Reset Address Pointer

The address registers consist of eight 16-bit registers used to store the node's individual and group addresses as well as the 32-bit T_Req value. Access to these registers is sequential, with each read or load instruction (1DHEX and 0DHEX) incrementing the pointer. The pointer is reset to zero with this instruction. It should be noted that the address pointer will "wrap-around" after the eighth access, so reset is not mandatory.

Load Address Registers

This instruction loads the address register selected by the pointer.

Load TVX Timer

This instruction loads the TVX timer with the TVX default value. This instruction is provided for test purposes and not intended for normal operation.

Read The Least-Significant Bits

The lower 5 bits of TNEG, TRT, and THT can be read via this instruction. Bit 15 of the NP-bus will reflect the state of the FORMAC's late flag. Bits 14–10 are the lower 5 bits of TNEG. Bits 9–5 indicate the lower TRT bits while 4–0 indicate the low-order THT bits.

Read TNEG

This instruction reads the upper 16 bits of the TNEG register.

Read MIR_1

This instruction reads the upper 16 bits of the 32-bit MIR value. Since MIR is loaded sequentially from the 8-bit network interface, the 16-bit value read could indicate a byte of the previous information and a byte of new information.

Read MIR_0

This instruction reads the lower 16 bits of the 32-bit MIR value.

Read THT

This instruction reads the upper 16 bits of THT.

Read TRT

This instruction reads the upper 16 bits of TRT.

Read TMAX

This instruction reads the TMAX register.

Read TVX

This instruction reads the 8-bit TVX default value and 8-bit TVX timer value. The default is read on the lower byte of the NP-bus while the timer value is placed on the most-significant byte.

Read States

This instruction reads the state machine register.

Read Mode Register

This instruction reads the mode register.

Read Interrupt Mask Register

This instruction reads the interrupt mask register.

Read Status

This instruction reads the status register. After this read instruction, all the status bits except for SRNGOP will be cleared.

Read Address Register

This instruction reads the address register selected by the pointer. After the read instruction, the pointer is incremented. If the last register was read, the pointer is reset.

Load TPRI

This instruction loads the TPRI 16-bit register with the value placed on the NP-bus. A binary value of "1" represents a time of 32 x the BCLK period.

Read TPRI

This instruction reads the TPRI 16-bit register.

Address Registers ($ADRS_{0-7}$)

The FORMAC has an address space organized as eight 16-bit words. The assignment of the eight words are shown in Figure 17.

The FORMAC address registers are used to implement individual and group as well as long and short addresses. These combinations are referred to as the long address individual (LAID), the short address group (SAGP) and short address individual (SAID). Two words are used to store the station's T_Request value. This value is equal to the number transmitted in the information field of the station claim frame. The most-significant 16-bits are stored in $TREQ_1$, with the least-significant word stored in $TREQ_0$. This value is used to compare against incoming claim values. One of the eight address words is reserved.

The eight address words can be read or written via the NP-bus. The user is cautioned not to access these registers unless the FORMAC is placed in Initialization mode. The registers will not be properly read or loaded unless this mode is selected.

MAC Information Register (MIR_{0-1})

In normal operation, the MIR is used to store the first four bytes following the source address of a MAC frame. In the case of claim frames, this field represents the T_Bid_RC value.

When the FORMAC is configured for loopback mode, the MIR will store the four bytes following the source address of any frame received. This provides a means for "in-circuit" testing without external hardware.

The MIR is composed of two separate 16-bit "read-only" registers. Each register is selected by executing a separate instruction. MIR_1 contains the most significant word or the first two bytes received from the media.

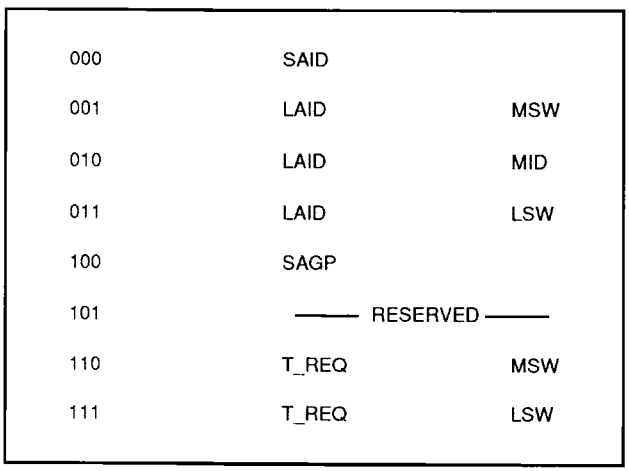
MIR is loaded sequentially with the bytes as they arrive on the FORMAC's internal receive bus. When reading MIR_1 and MIR_0 it is important to realize that the registers will only hold the correct value from the time the first four information bytes are received until the next frame arrives. Thus the MIR registers may only be useful for loopback testing where the frame reception is under user-control or at times when the protocol ensures successive reception of frames with identical information fields.

TMAX Register (TMAX)

In the FDDI scheme, the expected token rotation time (TRT) is negotiated through the token claiming procedure. During the claim procedure, TMAX is used as the node's expected TRT.

The TMAX register is used to load the TRT timer when the ring is not operational. The TMAX register represents bits 20–5 of the TMAX time. Bits 4–0 are fixed as zero. When loaded with TMAX, TRT will expire at a time equal to the TMAX value multiplied by the BCLK cycle time. The FDDI default for TMAX is 165 mS. If the BCLK cycle time was 80 ns, a TMAX value of 1F8720 would correspond to a TRT expiration of 165.3 mS. The upper 16 bits of this value (FC39HEX) would be loaded into TMAX to yield a 165 mS time value.

ARAM ASSIGNMENT



09731-020A

Figure 17. Address Register Assignment

Negotiated Token Rotation Time (TNEG)

This 21-bit register stores the lowest 21 bits of the bid field of a received Higher Claim or My Claim frame. When the ring becomes operational, this register represents the winning value of the claim process. The upper 16 bits of TNEG can be read with the IRDTNEG instruction. The lower 5 bits are read with the IRDTLSB instruction.

TVX Register (TVX)

The TVX value, as defined in the FDDI, is the expected time between valid transmissions. Each node maintains a TVX timer that checks the time between valid transmission. Should this timer expire, the node will attempt to recover the ring.

State Machine Register (STAT)

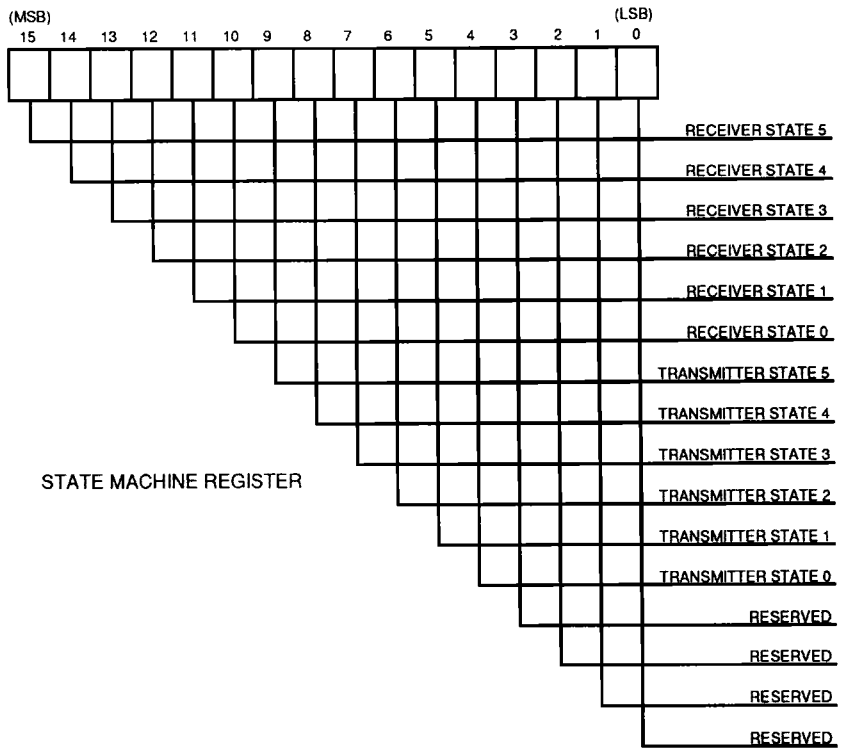
The state machine register is a 16-bit read only value that gives the states of the machines according to the FDDI MAC protocol specification. The bit assignment is given in Figure 18.

Status Register and Interrupts

One 16-bit register in the FORMAC is dedicated to status handling and interrupt reporting. The STAT register stores status information in the FORMAC. Any bit set in the status registers can be used to generate an interrupt. Bit 15, 14, and 13 generate non-maskable interrupts. Interrupt reporting on the lower 13 bits can be masked by clearing the appropriate bits of the IMSK register. All status bits are autocleared on reading with the exception of SRNGOP.

SRNGOP: Status Ring Operational

This bit is cleared when ring recovery actions are complete and set after the first token is received. A change in SRNGOP sets a shadow SOPCHNG flag. If SOPCHNG is HIGH, a non-maskable interrupt will be generated to the node processor. Reading the status word clears the SOPCHNG (but does not affect SRNGOP) thereby bringing $\overline{\text{NMINTR}}$ LOW.



09731-021B

Figure 18. State Machine Register

SMULTDA: Status Multiple Destination Address
This bit is used to identify nodes on the ring which use the same individual address. The bit is set when a frame is received which has an individual DA that matches the FORMAC individual address and which has the A_indicator set. SMULTDA forces a non- maskable interrupt.

SMISFRM: Status Missed Frame
The SMISFRM is set when the MAC logic sets the A_indicator (i.e. DA match) but repeats the C_indicator as received. This tells the NP that a frame which was sent to the node was not received. In general, any incoming frame whose destination address (DA) (and not the source address (SA)) matches the node's address and is not received causes the SMISFRM status bit to get set. This bit is set when the end delimiter of the frame is received. When bits $MADET_0$ and $MADET_0$ in the FORMAC mode register are programmed to anything other than 0,0, the SA is not checked as a qualifier for setting SMISFRM. The SMISFRM bit is set when an incoming frame, whose DA matches the node's address, is repeated but not received by the node for one of the following reasons:

1) The MISFRM signal is asserted to the FORMAC
2) The RCVABTI input to the FORMAC is asserted
3) The NP disables the FORMAC receiver or forces the FORMAC into the claim/beacon state

SMISFRM causes $\overline{\text{NMINTR}}$ to go LOW. SMISFRM stays LOW if the received frame was in error.

SXMTABT: Status Transmit Abort
Status Transmit Abort is set when the FORMAC generates a transmit abort. This status bit is used by the NP during ring recovery. Transmit abort occurs when the FORMAC leaves the Claim or Beacon mode.

STKERR: Status Token Error
The Status Token Error bit is set if a valid token is received while the FORMAC transmitter is in states T2 or T3.

SCLM: Status Claim
This bit is set when the FORMAC enters state T4: Claim state described in the FDDI transmit state machine.

SBEC: Status Beacon
This bit is set when the FORMAC enters state T5: Beacon state described in the FDDI transmit state machine.

STVXEXP: Status TVX Expired
STVXEXP is set when the valid transmission timer expires.

STRTEXP: Status TRT Expired
STRTEXP is set when the Token Rotation Timer expires and the Late count is not equal to zero.

STKISS: Status Token Issued
STKISS bit is set when the FORMAC issues a token and leaves state T3: Issue Token State.

SADET: Status Address Detect
The SADET bit is set when a received packet DA match occurs as indicated by the internal detection logic. The SADET is useful for monitoring received messages while data is being transmitted. The status bit is also used to check the address detect logic during loopback testing.

SMYCLM: Status My Claim
This bit is set when My_Claim is received.

SLOCLM: Status Lower Claim
SLOCLM is set when a lower claim (i.e., longer T_Bid_Rc) frame is received.

SHICLM: Status High Claim
This bit is set when a higher claim is received.

SMYBEC: Status My_Beacon
When My_Beacon is received, SMYBEC is asserted.

SOTRBEC: Status Other Beacon
SOTRBEC is asserted when Other Beacon is received.

Interrupt Mask Register (IMSK)

The interrupt mask register (IMSK) is used to disable interrupts caused by an event setting a status bit. Setting an IMSK bit to one enables the corresponding status bits capability of causing an interrupt. The bit assignment is given in Figure 19. All bits in IMSK are cleared when the FORMAC is reset.

Asynchronous Priority Register (TPRI)

The TPRI register is used to control the priority of all asynchronous messages within a node. The value of TPRI is compared with TRT or THT. Conceptually, TRT (or THT) act as "down counters." TRT is loaded with the token rotation time that was negotiated during claim (TNEG) and counts down until a new token is received. THT is loaded with the value of TRT when a token is captured, and then TRT is reset to the value of TNEG. If the most-significant 16 bits of the TRT value is greater than TPRI when a token is captured, then A-frames may be transmitted until THT falls below TPRI. TPRI is a 16-bit register, and is loaded with zeros when reset, giving the highest threshold priority.

Frame Status Register (FRSTAT)

The contents of the frame status register are placed on the YR-bus following the final FCS byte of a received frame. The special handshake flags this status information. The bit assignment within the register is as follows:

Bit 7: E_Indicator as received
Bit 6: A_Indicator as received
Bit 5: C_Indicator as received
Bit 4: Error detected at this node (CRC or Invalid Length)
Bit 3: Address Recognized
Bit 2: MAC Frame
Bit 1: SMT Frame
Bit 0: Implementer Frame

The first three bits are set if the status symbols received are set. Otherwise, these bits are zero. Bit 4 is set if the CRC comparison is incorrect or the frames length was invalid. Bit 3 is set if the frame's DA matched the node's address as a result of an internal or external match decision.

See also the $MSEXT_{0-7}$ bit descriptions in the 79C82A data sheet.

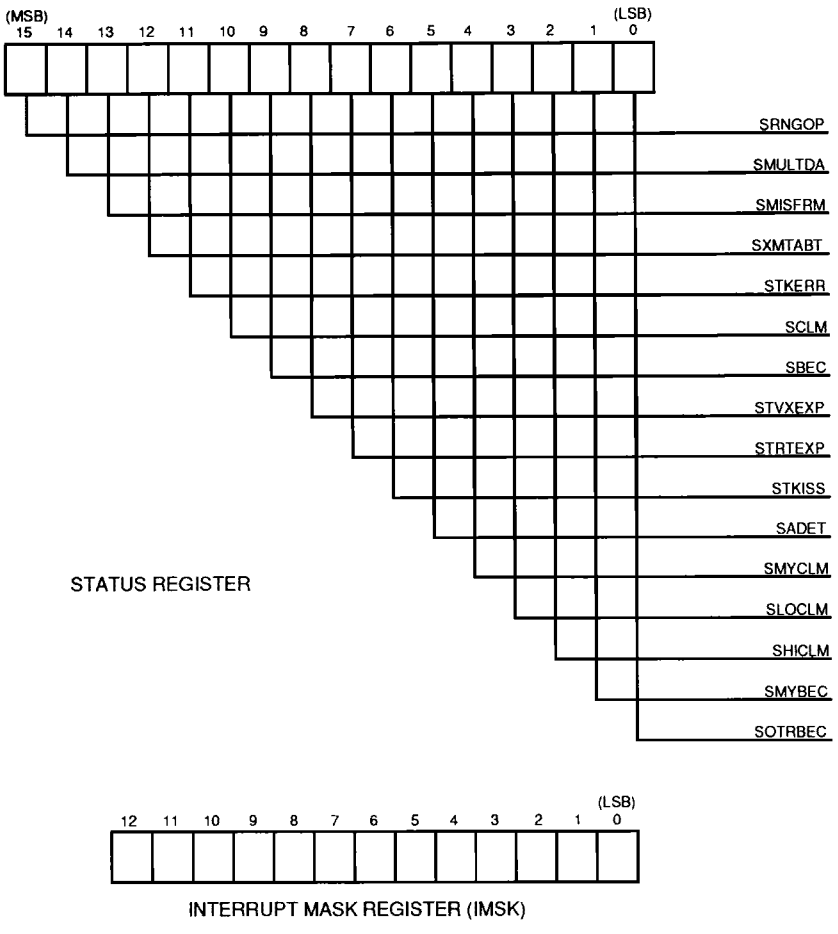


Figure 19. Status Register and Interrupt Mask Register

Data Handling and Formats

FDDI Frame Formats

The FDDI frame format is outlined in section 4 of the FDDI Token Ring MAC Layer Protocol Standard. Basically, FDDI frames are composed of the following fields in this order:

IDLE: Frame Preamble
SD: Start Delimiter
FC: Frame Control Field
DA: Destination Address
SA: Source Address
INFO: Information Field
FCS: Frame Check Sequence (CRC)
ED: End Delimiter
FS: Frame Status

For transmitted frames, the FORMAC will precede the transmission with the required IDLE and SD symbols. The FORMAC expects FC, DA, SA and INFO to be stored in the transmit buffer. If the MNFCS control bit is reset, the FORMAC will append the CRC result after the last byte stored in memory is presented to the ring. The FORMAC attaches the End Delimiter and FS indicators.

On receive, the FORMAC strips IDLE and SD before storing the frame. The 4-byte FCS field is stored at the end of the INFO field. The first three FS indicators are stored as bits in the received frame status field.

Network Data Format

Control and data information passed between the FORMAC and ENDEC is distinguished by a control signal. The upper nibble on each bus is interpreted as the first received from (or transmitted to) the media. Every 4 bits of information has a corresponding control signal. This line is LOW when the nibble represents an FDDI data symbol. For control symbols, the signal is asserted. Table 2 shows the format for symbol transfer between the two devices. Certain control characters are never generated by the FORMAC. They could be received from an ENDEC, however. These patterns are indicated with an asterisk.

User Test Mode

The loopback modes, described in the "Operational Modes" section, are provided to facilitate "on-line" testing of the FORMAC. Loopback testing can be performed internally as well as externally.

Table 2. Network Data Format

Symbol	NRZ Code	Format Control	FORMAC/ENDEC Int. Data
0	11110	0	0000
1	01001	0	0001
2	10100	0	0010
3	10101	0	0011
4	01010	0	0100
5	01011	0	0101
6	01110	0	0110
7	01111	0	0111
8	10010	0	1000
9	10011	0	1001
A	10110	0	1010
B	10111	0	1011
C	11010	0	1100
D	11011	0	1101
E	11100	0	1110
F	11101	0	1111
HALT1	00100	1	0100*
HALT2	10000	1	0100*
HALT3	01000	1	0100*
HALT4	00010	1	0100*
HALT5	00001	1	0100*
IDLE	11111	1	0111
J	11000	1	1100
K	10001	1	0011
QUIET	00000	1	0000*
R	00111	1	0001
S	11001	1	1001
T	01101	1	1101
VIOL1	00011	1	1000*
VIOL2	00101	1	1000*
VIOL3	00110	1	1000*
VIOL4	01100	1	1000*
Phy_Inv.	xxxxx	1	1111*
Phy_Inv._J	11000	1	1110*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Operating Temperature	−55 to +125°C
Maximum V_{CC} Relative to V_{SS}	−0.3 to +7.0 V
DC Voltage Applied to Any Pin Relative to V_{SS}	−0.5 to V_{CC} + 0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	InputLOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH}	Output HIGH Voltage (Note 1)	I_{OH} = −4.0 mA	2.4		V
I_{IX}	Input Leakage Current (Note 2)	0 V < V_{IN} < V_{CC}	−10	10	µA
I_{OZ}	Output Leakage Current (Note 3)	0.4 V < V_{OUT} < V_{CC}	−10	10	µA
I_{CC}	Power Supply Current	V_{CC} = Max. f(BCLK) = 12.5 MHz		140	mA

Notes:
1. V_{OH} does not apply to open-drain output pins.
2. I_{IX} applies to all input-only pins.
3. I_{OZ} applies to all three-state output pins and bidirectional pins.

CAPACITANCE*

Parameter Symbol	Parameter Descriptions	Typ.	Unit
C_{IN}	Input Pins (except $HOLD_1$)	15	pF
C_{IO}	Bidirectional Pins (except R/$\overline{W}$)	15	pF

Notes:

*Pin capacitance is characterized at a frequency of 1 MHz, but is not 100% tested.

$HOLD_1$ has Cin ≤ 30 pF, R/$\overline{W}$ has C_{IO} ≤ 25 pF.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Notes 1 & 3)

Parameter Number	Parameter Description	Parameter Symbol	Min. (Note 2)	Max. (Note 2)	Unit
1	Clock Period	BCLK	80		ns
2	HIGH Pulse Width	BCLK	35		ns
3	LOW Pulse Width	BCLK	35		ns
4	Setup Time Before BCLK ↑	$\overline{CSI}$, $\overline{DS}$, $INST_{0-3}$, R/$\overline{W}$	45		ns
5	Hold Time After BCLK ↑	$\overline{CSI}$, R/$\overline{W}$	2		ns
6	Hold Time After BCLK ↑	$\overline{DS}$	6		ns
7	Hold Time After BCLK ↑	$INST_{0-3}$	10		ns
8	Hold Time After BCLK ↑	NP_{0-15}	15		ns
9	Setup Time Before BCLK ↑	NP_{0-15}	12		ns
10	R/$\overline{W}$ ↑, $\overline{CSI}$ ↓, $\overline{DS}$ ↓ (Whichever Occurs Last) Until NP-bus is Enabled (Synchronous Mode)	NP_{0-15}	3		ns
11	Signal Valid After BCLK ↑	NP_{0-15}		51	ns
12	Signal Invalid After BCLK ↑	NP_{0-15}	3		ns
13	Signal Invalid After $\overline{CSI}$ ↑ or R/$\overline{W}$ ↓ (Whichever Occurs First at the End of a Synchronous Read Cycle)	NP_{0-15}	3		ns
14	R/$\overline{W}$ ↓ or $\overline{CSI}$ ↑ (Whichever Occurs First at the End of a Synchronous Read Cycle) to Bus Inactive	NP_{0-15}		35	ns
15	Hold Time After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Write)	NP_{0-15}	0		ns
16	Signal LOW After NP-bus Valid	$\overline{READY}$	(T1– 20)		ns
17–19	Unused				
20	Setup Time Before $\overline{CSI}$ ↓ or $\overline{DS}$ ↓ (Whichever Occurs Last in Asynchronous Read/Write)	R/$\overline{W}$ ↓ (Write) or R/$\overline{W}$ ↑ (Read), $INST_{0-3}$	0		ns
21	Unused				
22	Pulse Width HIGH (Asynchronous Read or Write)	$\overline{DS}$, $\overline{CSI}$	(1.5 x T1)		ns
23	Hold Time After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First at the End of Asynchronous Read/Write)	R/$\overline{W}$ ↑(Write) or R/$\overline{W}$ ↓ (Read), $INST_{0-3}$	0		ns
24	Signal LOW After $\overline{DS}$ or $\overline{CSI}$ ↓	$\overline{READY}$	3 x T1	(4 x T1 + 70)	ns
25	Signal Disabled After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑	$\overline{READY}$		40	ns
26	Bus Active After $\overline{DS}$ ↓ or $\overline{CSI}$ ↓(Whichever Occurs Last in Asynchronous Read)	NP_{0-15}	0		ns
27	Bus Valid After $\overline{DS}$ ↓ or $\overline{CSI}$ ↓ (Whichever Occurs Last in Asynchronous Read)	NP_{0-15}		(3 x T1 + 48)	ns

SWITCHING CHARACTERISTICS (Continued)

Parameter Number	Parameter Description	Parameter Symbol	Min. (Note 2)	Max. (Note 2)	Unit
28	Signal Invalid After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Read)	NP_{0-15}	0		ns
29	Bus Disabled After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Read)	NP_{0-15}		35	ns
30	Setup Time Before $\overline{DS}$ ↓ or $\overline{CSI}$ ↓ (Whichever Occurs Last in Asynchronous Write)	NP_{0-15}	–[(T1 x 2) –20]		ns
31	RA_bus, RB_bus Setup Before BCLK ↑	RA_{0-7}, RACU, RACL, RAP, RB_{0-7}, RBCL, RBCU, RBP	10		ns
32	Signal Enabled After BCLK ↑	YR_{0-7}, YRP	2		ns
33	Signal Valid After BCLK ↑	YR_{0-7}, YRP		50	ns
34	Signal Invalid After BCLK ↑	YR_{0-7}, YRP	9		ns
35	Signal Disabled After BCLK ↑	YR_{0-7}, YRP		55	ns
36	Hold Time After BCLK ↑	RA_{0-7}, RACU, RACL, RAP, RB_{0-7}, RBCU, RBCL, RBP	15		ns
37	Signal Valid After BCLK ↑	RECEIVE		45	ns
38	Signal Invalid After BCLK ↑	RECEIVE	8		ns
39	Signal Valid After BCLK ↑	DAVALID		45	ns
40	Signal Invalid After BCLK ↑	DAVALID	8		ns
41	Signal Valid After BCLK ↑	FSHRCVF		50	ns
42	Signal Invalid After BCLK ↑	FSHRCVF	8		ns
43	Signal Valid After BCLK ↑	RCVABTO		50	ns
44	Signal Invalid After BCLK ↑	RCVABTO	8		ns
45	Setup Time Before BCLK ↑	RCVABTI, MISFRM	10		ns
46	Hold Time After BCLK ↑	RCVABTI, MISFRM	9		ns
47	Setup Time Before BCLK ↑	$\overline{XDAMAT}$, $\overline{XSAMAT}$	10		ns
48	Hold Time After BCLK ↑	$\overline{XDAMAT}$, $\overline{XSAMAT}$	10		ns
49	Signal Valid After BCLK ↑	LPBEN		55	ns
50	Setup Time Before BCLK ↑	FULL	20		ns
51	Signal Invalid After BCLK ↑	LPBEN	3		ns
52	Hold Time BCLK ↑	FULL	10		ns
53	Unused				
54	Setup Before BCLK ↑	YT_{0-7}, YTP	10		ns
55	Hold Time After BCLK ↑	YT_{0-7}, YTP	15		ns
56	Setup Time After BCLK ↑	MEDREQS, MEDREQA	20		ns
57	Signal Valid After BCLK ↑	XMEDAVS, XMEDAVA		45	ns
58	Hold Time After BCLK ↑	MEDREQS, MEDREQA	10		ns
59	Signal Invalid After BCLK ↑	XMEDAVS, XMEDAVA	8		ns
60	Unused				
61	Setup Before BCLK ↑	RDYTBYT	20		ns
62	Hold Time After BCLK ↑	RDYTBYT	10		ns
63	Signal Valid After BCLK ↑	XFRBYTE		40	ns
64	Signal Invalid After BCLK ↑	XFRBYTE	3		ns
65	Signal Valid After BCLK ↑	X_{0-7}, XCU, XCL, XP		57	ns
66	Signal Invalid After BCLK ↑	X_{0-7}, XCU, XCL, XP	10		ns
67	Signal Valid After BCLK ↑	XMTABTO		50	ns
68	Signal Invalid After BCLK ↑	XMTABTO	10		ns
69	Signal Invalid After BCLK ↑	INICLBN	8		ns
70	Signal Valid After BCLK ↑	INICLBN		50	ns

SWITCHING CHARACTERISTICS (Continued)

Parameter Number	Parameter Description	Parameter Symbol	Min. (Note 2)	Max. (Note 2)	Unit
71	Signal Valid After BCLK ↑	CLM/$\overline{\text{BEC}}$		50	ns
72	Signal Invalid After BCLK ↑	CLM/$\overline{\text{BEC}}$	10		ns
73	Signal LOW after BCLK ↑	$\overline{\text{NMINTR}}$, $\overline{\text{MINTR}}$		45	ns
74	Signal Disabled After BCLK ↑	$\overline{\text{NMINTR}}$, $\overline{\text{MINTR}}$	0 (Note 1h)		ns
75	Setup Time Before BCLK ↑	XMTABTI	20		ns
76	Hold Time After BCLK ↑	XMTABTI	6		ns
77	Signal Valid After BCLK ↑	TOKISD		50	ns
78	Signal Invalid After BCLK ↑	TOKISD	3		ns
79	Unused				
80	Signal Valid After BCLK ↑	SDRCVD		45	ns
81	SDRCVD Invalid After BCLK ↑	SDRCVD	8		ns
82	LNGADR Valid After BCLK ↑	LNGADR		50	ns
83	LNGADR Invalid After BCLK ↑	LNGADR	10		ns
84	Signal Valid After BCLK ↑	EOUT, AOUT, COUT		50	ns
85	Signal Invalid After BCLK ↑	EOUT, AOUT, COUT	3		ns
86	Signal Valid After BCLK ↑	$\overline{\text{FSVLD}}$		45	ns
87	$\overline{\text{FSVLD}}$ Invalid After BCLK ↑	$\overline{\text{FSVLD}}$	8		ns
88	Unused				
89	Signal Valid After BCLK ↑	FRINC, LSTINC, ERRINC		50	ns
90	Signal Invalid After BCLK ↑	FRINC, LSTINC, ERRINC	3		ns
91	Pulse Width HIGH	FRINC, LSTINC, ERRINC	60		ns
92–93	Unused				
94	Signal Invalid After BCLK ↑	S_{0-3}	8		ns
95	Signal Valid After BCLK ↑	S_{0-3}		45	ns

Notes:

1. Measurement points for timing parameters are the following:

   a) Input waveforms: +1.4 V

   b) Output HIGH threshold: > 2.0 V

   c) Output LOW threshold: < 0.8 V

   d) Output valid: < 0.8 V or > 2.0 V

   e) Output invalid minimum: output is verified to be still valid at the minimum spec time.

   f) Output enabled: time when the output driver turns on.

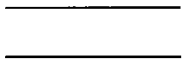
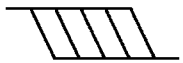
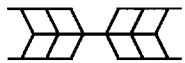
   g) Output disabled: time when the output driver turns off.

   h) T74 is guaranteed by design.

2. Numbered parameters such as T1 or T51 refer to the switching characteristic number listed in the far left–hand column.

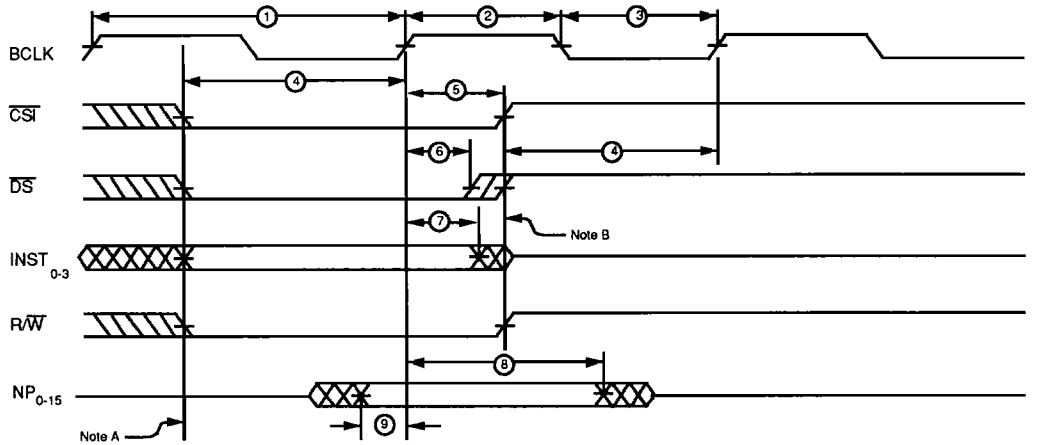
3. Maximum "BCLK to Signal Valid" delay and minimum "BCLK to Signal Invalid" delay specifications apply to both rising and falling edges of the signal listed, even though the measurement is only shown once in the Switching Waveforms section that follows. Valid and Invalid do not mean HIGH or LOW; see notes 1d and 1e and Switching Waveforms for the definition of Valid and Invalid.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



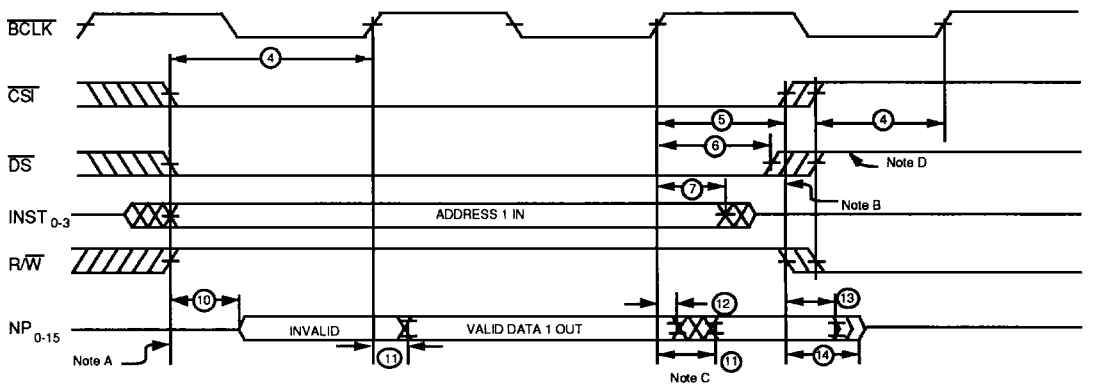
09729-018A

Notes:

A. Timing measured from falling edge of $\overline{CSI}$, $\overline{DS}$, or R/$\overline{W}$ or the assertion of $INST_{0-3}$, whichever occurs last.

B. Parameter #5 is measured from the rising edge of $\overline{CSI}$, or R/$\overline{W}$, whichever occurs first;
Parameter #4 is measured from the falling edge of $\overline{CSI}$, $\overline{DS}$, or R/$\overline{W}$, or the assertion of $INST_{0-3}$, whichever occurs last.

NP-Bus Synchronous Write Timing



09729-019A

Notes:

A. Timing measured from falling edge of $\overline{CSI}$ or $\overline{DS}$, or the rising edge of R/$\overline{W}$ (or the assertion of $INST_{0-3}$ for parameter #4 only), whichever occurs last.

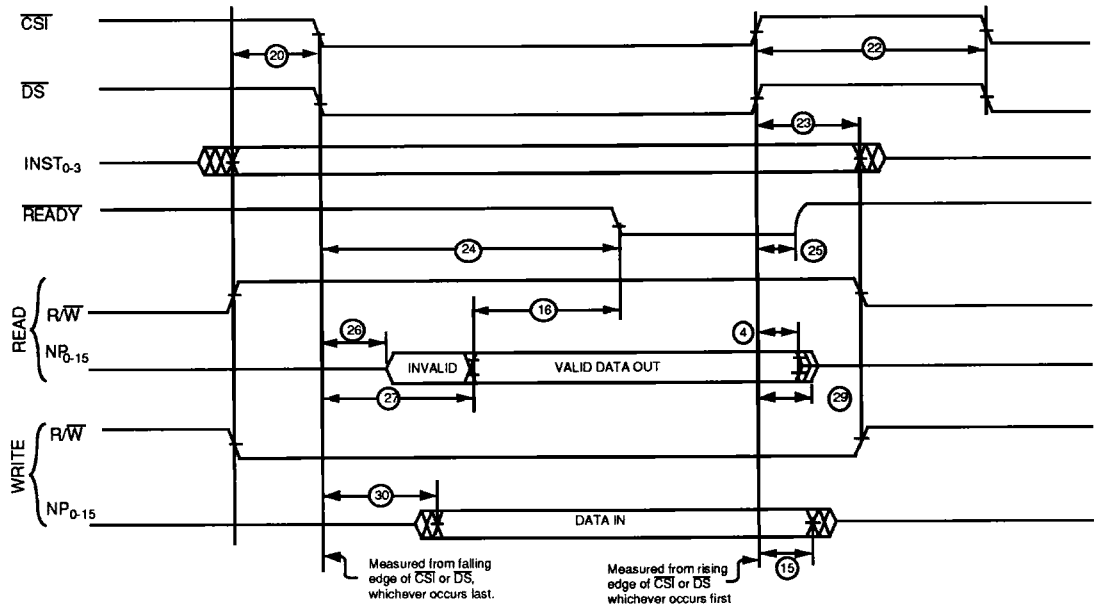
B. Timing is measured from the rising edge of $\overline{CSI}$ or the falling edge of R/$\overline{W}$, whichever occurs first.

C. If an address register in the FORMAC is being addressed, then the register being read onto the NP-bus will be incremented with each rising edge of BLCK.

D. $\overline{DS}$ must be driven HIGH at the completion of each read cycle.

NP-Bus Synchronous Read Timing

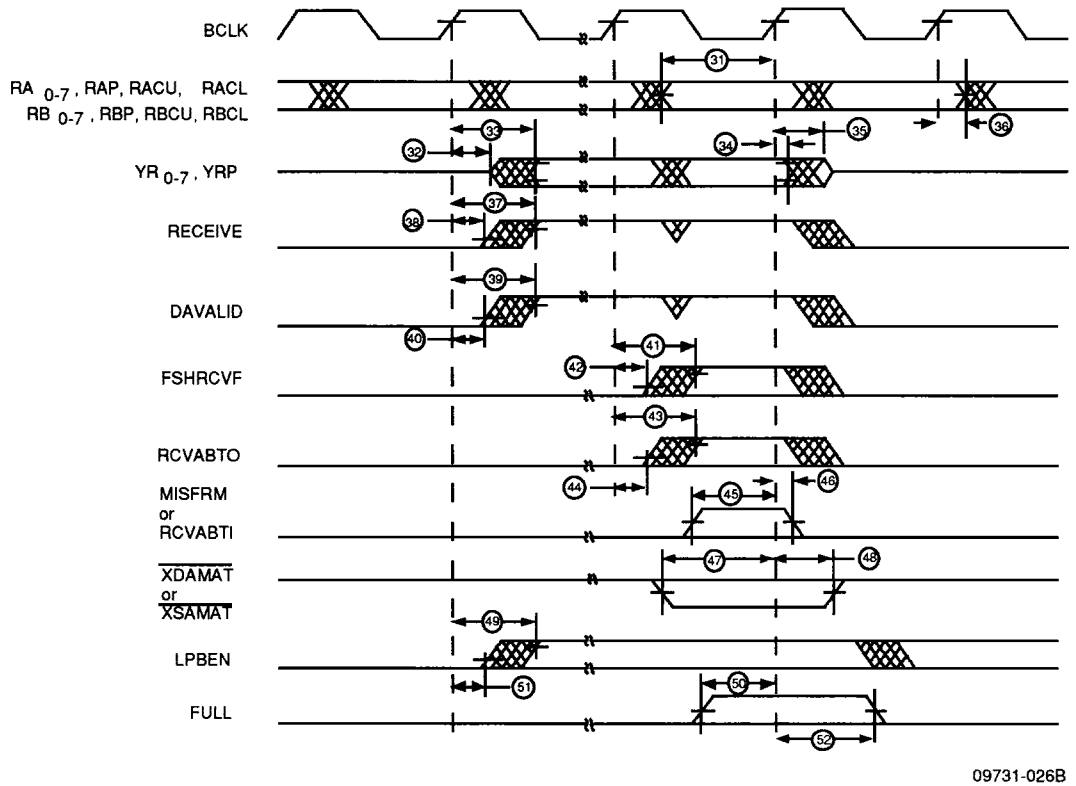
SWITCHING WAVEFORMS



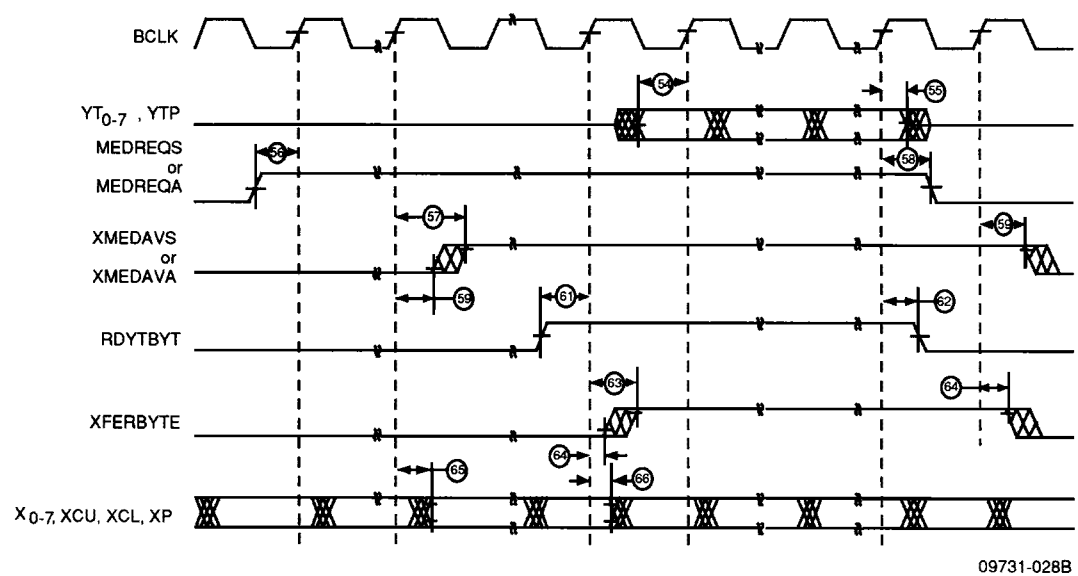
09729-020A

NP-Bus Asynchronous Read/Write Timing

SWITCHING WAVEFORMS

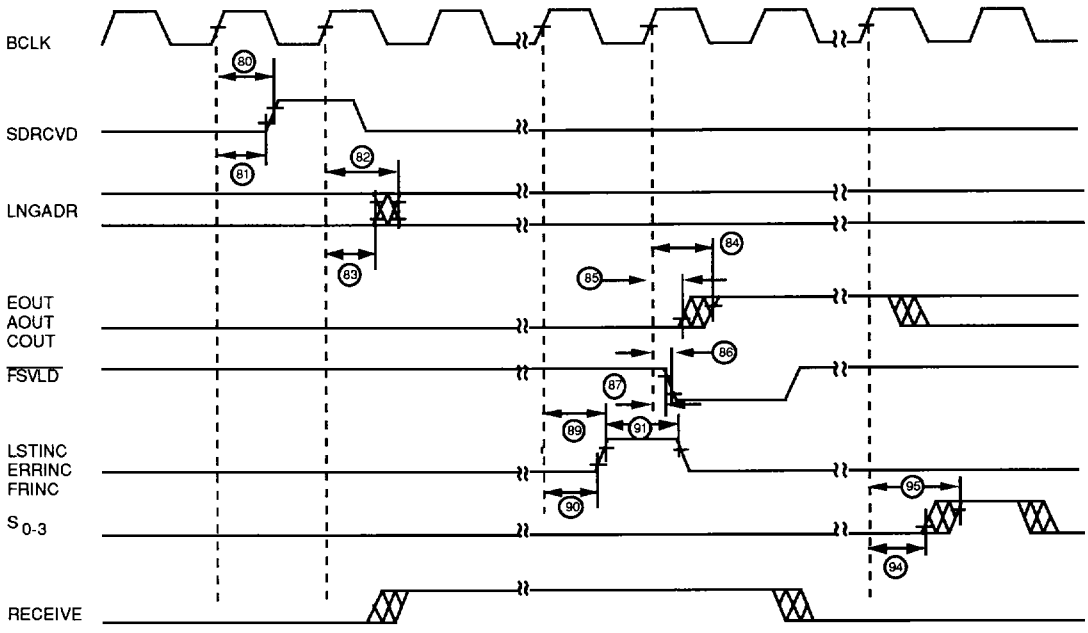


Frame Reception Timing

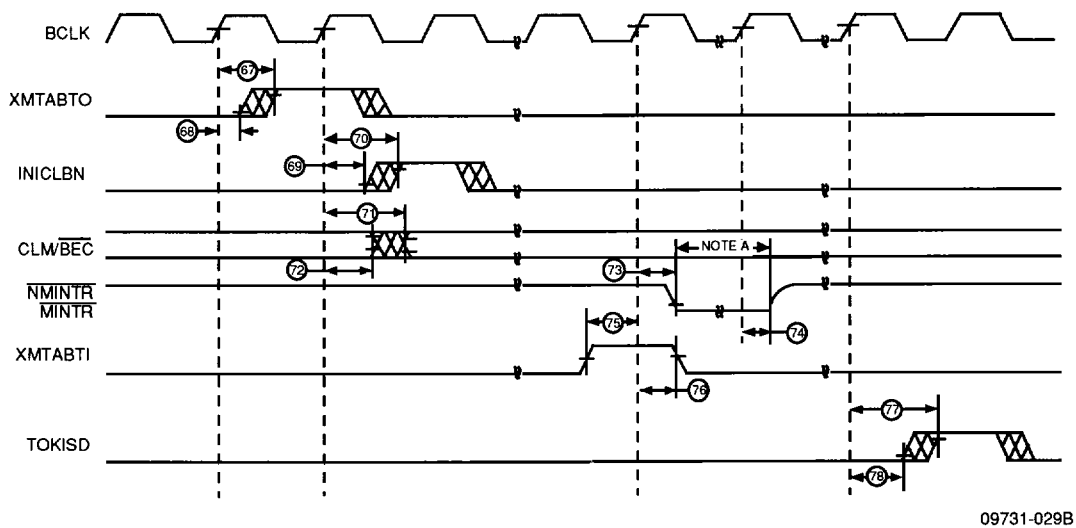


Frame Transmission Timing

SWITCHING WAVEFORMS



Frame Recovery Timing

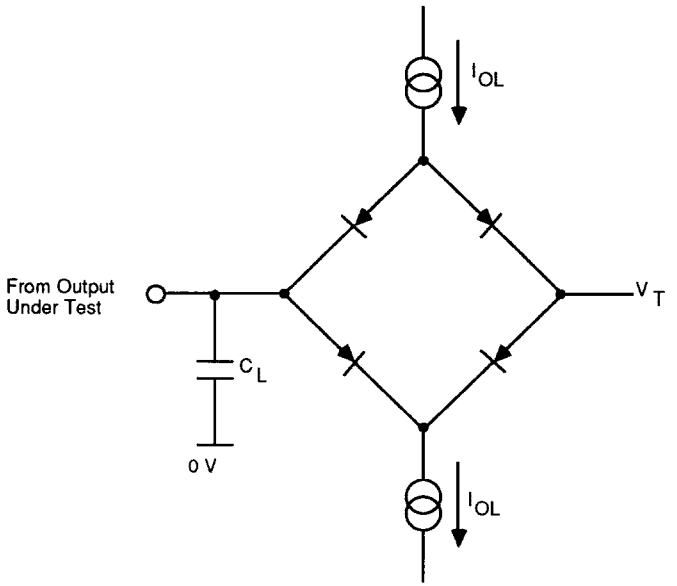


Note:

A. This signal will stay LOW# until the status register is read.

Special Frame Reception Timing

SWITCHING TEST CIRCUIT

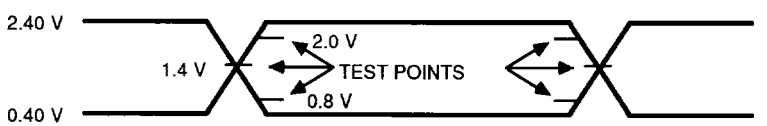


Notes:

C_L = 100 pF for pin NP_{0-15} $\overline{READY}$, $\overline{MINTR}$, $\overline{NMINTR}$.
C_L = 50 pF for all other output pins.

Standard Test Load 09731-023A

SWITCHING TEST WAVEFORM



Input/Output Waveform

09731-024A