SMART
Modular Technologies

SM5364400
September 1992
Rev 0

SM5364400
16MByte (4M x 36) CMOS DRAM Module

General Description

The SM5364400 is a high performance, 16-megabyte dynamic RAM module organized as 4M words by 36 bits, in a 72-pin, leadless, single-in-line memory module (SIMM) package.

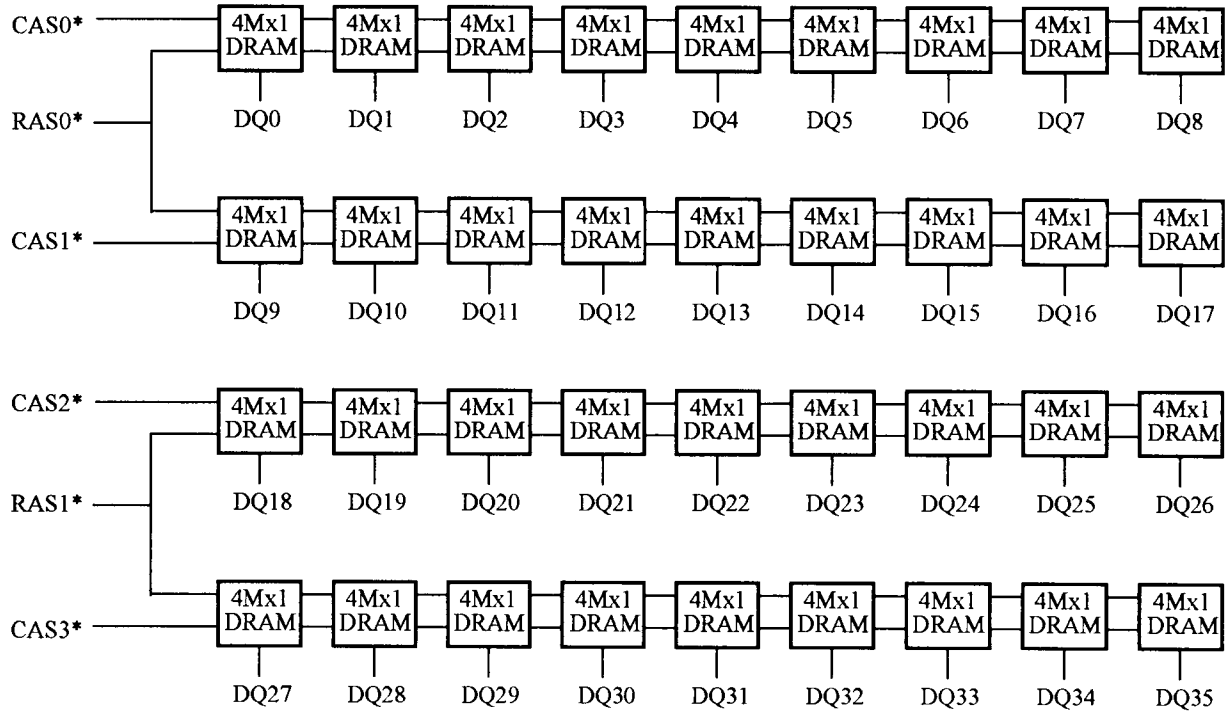
The module utilizes thirtysix CMOS 4M x 1 dynamic RAMs in surface mount package on an epoxy laminate substrate. The ninth 4M x 1 DRAM per bank is for parity. Each device is accompanied by a 0.22μf decoupling capacitor for improved noise immunity.

Control lines are so provided that byte control is possible.

Features

- JEDEC standard pinout
- High Density : 16 MByte
- Fast Access Time of 60/70/80ns (max.)
- Low Power :
  21.8/19.8/17.8W (max.) - Active (60/70/80ns)
  0.396W (max.) - Standby (TTL)
  0.198W(max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes
- Single power supply of 5V±10%
- PCB footprint of less than 1.67 sq. in.
- Low profile of 1.29 in.

Functional Diagram



Notes: 1. "*" signifies complement signal.
2. A0~A10 to all devices.
3. WE* to all devices.

V_{CC} —||— V_{SS}
0.22μF to all DRAMs

(All specifications of this device are subject to change without notice)

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Pin Name

A0~A10	Addresses
DQ0~DQ35	Data Inputs/Outputs
CAS0*~CAS3*	Column Address Strobes
RAS0*, RAS1*	Row Address Strobes
WE*	Write Enable
PD1~PD4	Presence Detects
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

Pin	-06	-07	-08
PD1	GND	GND	GND
PD2	NC	NC	NC
PD3	NC	GND	NC
PD4	NC	NC	GND

Ordering Information

Part Number	Speed
SM5364400-06	60 ns
SM5364400-07	70 ns
SM5364400-08	80 ns

Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	V_{SS}
4	DQ1	40	CAS0*
5	DQ19	41	CAS2*
6	DQ2	42	CAS3*
7	DQ20	43	CAS1*
8	DQ3	44	RAS0*
9	DQ21	45	NC
10	V_{CC}	46	NC
11	NC	47	WE*
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	V_{CC}
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	V_{CC}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS1*	70	PD4
35	DQ26	71	NC
36	DQ8	72	V_{SS}

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	- 1 to +7.0	V
Power Dissipation	P_T	36	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	Tstg	- 55 to +125	°C
Short Circuit Output Current	I_{OS}	50	mA

Recommended DC Operating Conditions
(T_A = 0 to +70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1	-	0.8	V

DC Characteristics
(V_{CC} = 5V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Max. -06	Max. -07	Max. -08	Unit	Note
Operating Current	I_{CC1}	RAS*, CAS* cycling; t_{RC} = min.	3960	3600	3240	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS*, CAS* = V_{IH} D_{out} = High-Z	72	72	72	mA	
		CMOS Interface RAS*, CAS* ≥ V_{CC} - 0.2V D_{out} = High-Z	36	36	36	mA	
RAS* only Refresh Current	I_{CC3}	t_{RC} = Min	3960	3600	3240	mA	2
Standby Current	I_{CC5}	RAS* = V_{IH}, CAS* = V_{IL}, D_{out} = Enable	180	180	180	mA	1
CAS*-Before-RAS* Refresh Current	I_{CC6}	t_{RC} = Min.	3960	3600	3240	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	3960	3600	3240	mA	1, 3

DC Characteristics (contd.)

Parameter	Symbol	Test Conditions	-06		-07		-08		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le 7V$	-360	360	-360	360	-360	360	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le 7V$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	I_{OH} = -5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS* = V_{IL}.
3. Address can be changed once or less while CAS* = V_{IH}.

Capacitance
(T_A =+25°C, V_{CC} = 5V±10%)

Parameter	Symbol	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	185	pF	1
Input Capacitance (RAS0*, RAS1*)	C_{I2}	17	pF	1
Input Capacitance (CAS0* ~ CAS3*)	C_{I3}	66	pF	1
Input Capacitance (WE*)	C_{I4}	257	pF	1
Input/Output Capacitance (DQ0~DQ35)	$C_{I/O}$	10	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* = V_{IH} to disable D_{out}.

AC Characteristics
(T_A = 0 to +70 °C, V_{CC} = 5.0V±10%, V_{SS} = 0V)

Parameter	Symbol	-06		-07		-08		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read/write cycle time	t_{RC}	110	-	130	-	150	-	ns	
Access time from RAS*	t_{RAC}	-	60	-	70	-	80	ns	3, 4
Access time from CAS*	t_{CAC}	-	15	-	20	-	20	ns	3, 4, 5
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Output buffer turn-off time	t_{OFF}	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
RAS* precharge time	t_{RP}	40	-	50	-	60	-	ns	
RAS* pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
RAS* hold time	t_{RSH}	15	-	20	-	20	-	ns	

AC Characteristics (contd.)

Parameter	Symbol	-06		-07		-08		Unit	Note
		Min	Max	Min	Max	Min	Max		
CAS* hold time	t_{CSH}	60	-	70	-	80	-	ns	
CAS* pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
RAS* to CAS* delay time	t_{RCD}	20	45	20	50	20	60	ns	4
RAS* to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
CAS* to RAS* precharge time	t_{CRP}	10	-	10	-	10	-	ns	
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	15	-	ns	
Column address to RAS* lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time to CAS*	t_{RCH}	0	-	0	-	0	-	ns	8
Read command hold time to RAS*	t_{RRH}	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	15	-	15	-	15	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	10	-	ns	
Write command to RAS* lead time	t_{RWL}	15	-	20	-	20	-	ns	
Write command to CAS* lead time	t_{CWL}	15	-	20	-	20	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	9
Data-in hold time	t_{DH}	15	-	15	-	15	-	ns	9
Refresh period (1024 cycles)	t_{REF}	-	16	-	16	-	16	ms	
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)	t_{CSR}	10	-	10	-	10	-	ns	1
CAS* hold time (CBR refresh)	t_{CHR}	10	-	10	-	10	-	ns	1
RAS* precharge to CAS* hold time	t_{RPC}	10	-	10	-	10	-	ns	
Access time from CAS* precharge	t_{ACP}	-	35	-	40	-	45	ns	3, 11
Fast page mode cycle time	t_{PC}	40	-	45	-	50	-	ns	
CAS* precharge time (Fast page)	t_{CP}	10	-	10	-	10	-	ns	
RAS* pulse width (Fast page)	t_{RASC}	-	100000	-	100000	-	100000	ns	12

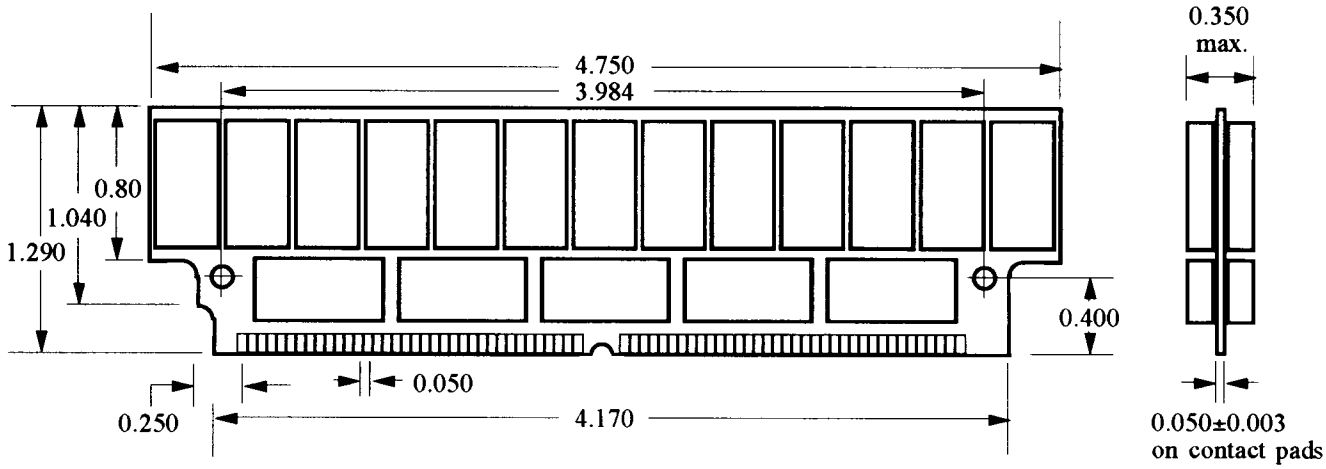
Notes:
1. An initial pause of atleast 500µs is required after power-up followed by any eight RAS* cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are refernce levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) limit can be met; t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

Notes (contd.):

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS* leading edge in early write cycles.
10. Operation within the $t_{RAD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA} , t_{CAC} or t_{ACP}.
12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

72-pin SIMM



All dimensions are in inches with ±0.005" tolerance unless specified otherwise.
Do not scale drawing.

TIMING WAVEFORMS

Read Cycle

Write Cycle (Early Write)

Fast Page Mode Read Cycle

Fast Page Mode Write Cycle (Early Write)

RAS* Only Refresh Cycle

Hidden Refresh Cycle

CAS*-Before-RAS* Refresh Cycle