Document order number: MC33883/D
Rev 6.0, 01/2004

33883

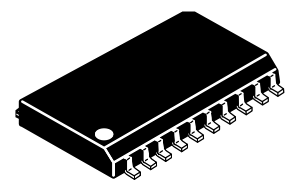
H-Bridge Gate Driver IC

The 33883 is an H-bridge gate driver (also known as a full-bridge predriver) IC with integrated charge pump and independent high- and low-side gate driver channels. The gate driver channels are independently controlled by four separate input terminals, thus allowing the device to be optionally configured as two independent high-side gate drivers and two independent low-side gate drivers. The low-side channels are referenced to ground. The high-side channels are floating.

The gate driver outputs can source and sink up to 1.0 A peak current pulses, permitting large gate-charge MOSFETs to be driven and/or high Pulse Width Modulation (PWM) frequencies to be utilized. A linear regulator is incorporated, providing a 15 V typical gate supply to the low-side gate drivers.

Features
- V_{CC} Operating Voltage Range from 5.5 V up to 55 V
- V_{CC2} Operating Voltage Range from 5.5 V up to 28 V
- CMOS/LSTTL Compatible I/O
- 1.0 A Peak Gate Driver Current
- Built-In High-Side Charge Pump
- Undervoltage Lockout (UVLO)
- Overvoltage Lockout (OVLO)
- Global Enable with <10 µA Sleep Mode
- Supports PWM up to 100 kHz

H-BRIDGE GATE DRIVER IC

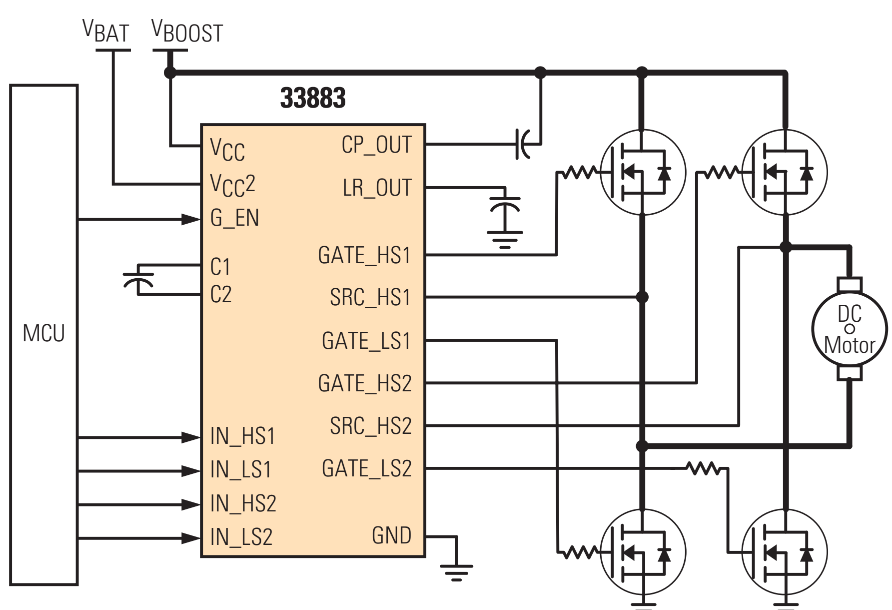


DW SUFFIX
CASE 751D-06
20-TERMINAL SOICW

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33883DW/R2	-40°C to 125°C	20 SOICW

Simplified Application Diagram



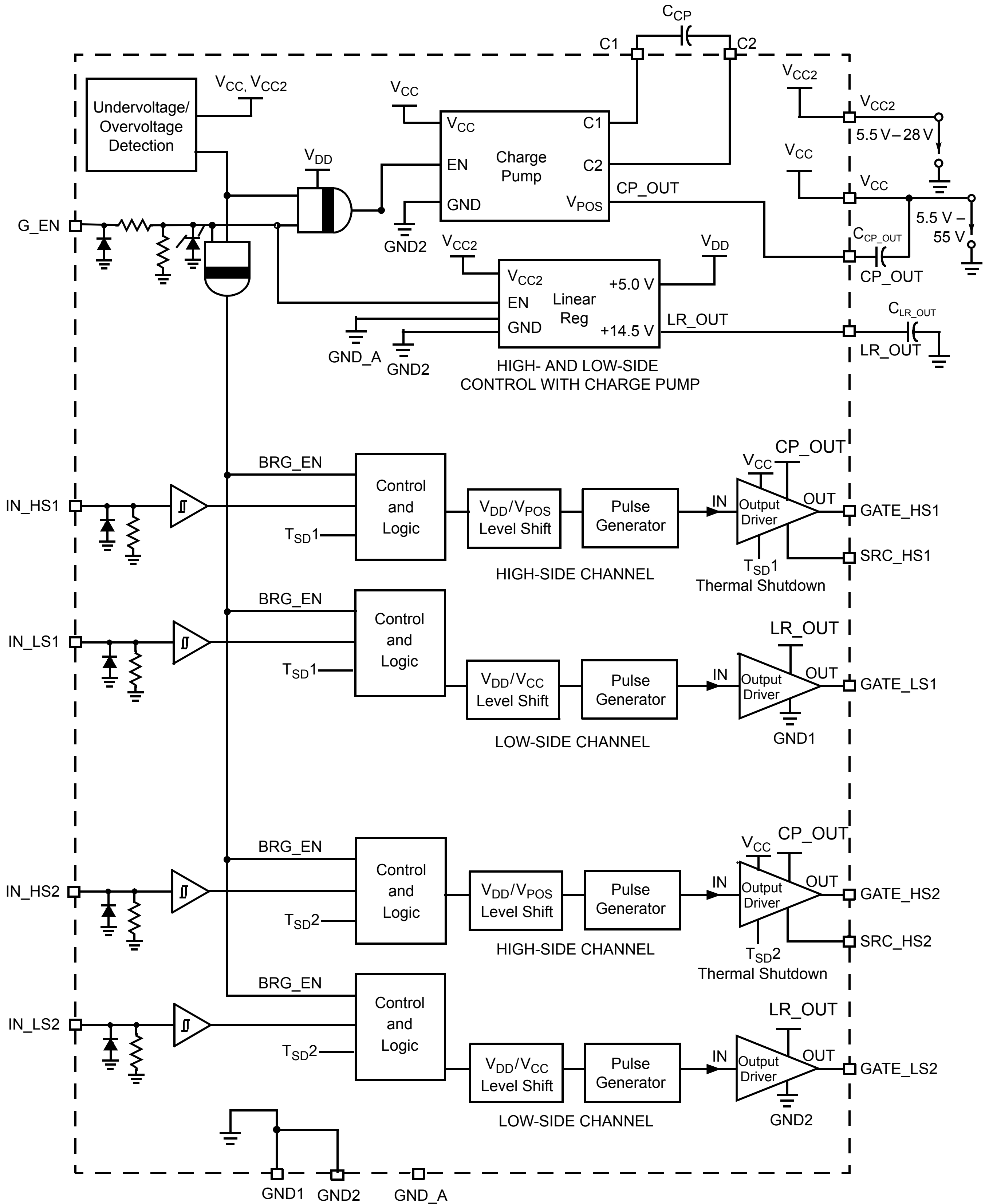
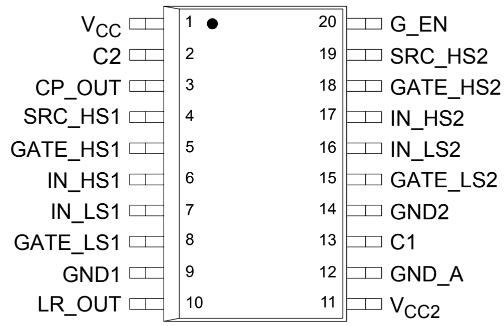


Figure 1. 33883 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	V_{CC}	Supply Voltage 1	Device power supply 1.
2	C2	Charge Pump Capacitor	External capacitor for internal charge pump.
3	CP_OUT	Charge Pump Out	External reservoir capacitor for internal charge pump.
4	SRC_HS1	Source 1 Output High Side	Source of high-side 1 MOSFET
5	GATE_HS1	Gate 1 Output High Side	Gate of high-side 1 MOSFET.
6	IN_HS1	Input High Side 1	Logic input control of high-side 1 gate (i.e., IN_HS1 logic HIGH = GATE_HS1 HIGH).
7	IN_LS1	Input Low Side 1	Logic input control of low-side 1 gate (i.e., IN_LS1 logic HIGH = GATE_LS1 HIGH).
8	GATE_LS1	Gate 1 Output Low Side	Gate of low-side 1 MOSFET.
9	GND1	Ground 1	Device ground 1.
10	LR_OUT	Linear Regulator Output	Output of internal linear regulator.
11	V_{CC2}	Supply Voltage 2	Device power supply 2.
12	GND_A	Analog Ground	Device analog ground.
13	C1	Charge Pump Capacitor	External capacitor for internal charge pump.
14	GND2	Ground 2	Device ground 2.
15	GATE_LS2	Gate 2 Output Low Side	Gate of low-side 2 MOSFET.
16	IN_LS2	Input Low Side 2	Logic input control of low-side 2 gate (i.e., IN_LS2 logic HIGH = GATE_LS2 HIGH).
17	IN_HS2	Input High Side 2	Logic input control of high-side 2 gate (i.e., IN_HS2 logic HIGH = GATE_HS2 HIGH).
18	GATE_HS2	Gate 2 Output High Side	Gate of high-side 2 MOSFET.
19	SRC_HS2	Source 2 Output High Side	Source of high-side 2 MOSFET.
20	G_EN	Global Enable	Logic input Enable control of device (i.e., G_EN logic HIGH = Full Operation, G_EN logic LOW = Sleep Mode).

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Supply Voltage 1	V_{CC}	-0.3 to 65	V
Supply Voltage 2 (Note 1)	V_{CC2}	-0.3 to 35	V
Linear Regulator Output Voltage	V_{LR_OUT}	-0.3 to 18	V
High-Side Floating Supply Absolute Voltage	V_{CP_OUT}	-0.3 to 65	V
High-Side Floating Source Voltage	V_{SRC_HS}	-1.0 to 65	V
High-Side Source Current from CP_OUT in Switch ON State	I_S	250	mA
High-Side Gate Voltage	V_{GATE_HS}	-0.3 to 65	V
High-Side Gate Source Voltage	V_{GATE_HS} - V_{SRC_HS}	-0.3 to 20	V
High-Side Floating Supply Gate Voltage	V_{CP_OUT} - V_{GATE_HS}	-0.3 to 65	V
Low-Side Gate Voltage	V_{GATE_LS}	-0.3 to 17	V
Wake-Up Voltage	V_{G_EN}	-0.3 to 35	V
Logic Input Voltage	V_{IN}	-0.3 to 10	V
Charge Pump Capacitor Voltage	V_{C1}	-0.3 to V_{LR_OUT}	V
Charge Pump Capacitor Voltage	V_{C2}	-0.3 to 65	V
ESD Voltage Human Body Model on All Pins (V_{CC} and V_{CC2} as Two Power Supplies) (Note 2) Machine Model (Note 3)	 V_{ESD1} V_{ESD2}	 ±1500 ±130	V
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ 25°C Thermal Resistance (Junction to Ambient) Operating Junction Temperature Storage Temperature	 P_D $R_{\theta JA}$ T_J T_{STG}	 1.25 100 -40 to 150 -65 to 150	 W °C/W °C °C
Terminal Soldering Temperature (Note 4)	T_{SOLDER}	240	°C

Notes

1. V_{CC2} can sustain load dump pulse of 40 V, 400 ms, 2.0 Ω.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
4. Terminal soldering temperature limit is for 10 second maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise noted. Typical values for T_A = 25°C and min/max values for T_A = -40°C to 125°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Supply Voltage 1 for Output High-Side Driver and Charge Pump	V_{CC}	5.5	–	55	V
Supply Voltage 2 for Linear Regulation	V_{CC2}	5.5	–	28	V
High-Side Floating Supply Absolute Voltage	V_{CP_OUT}	V_{CC}+4	–	V_{CC}+11 but < 65	V
LOGIC					
Logic 1 Input Voltage (IN_LS and IN_HS)	V_{IH}	2.0	–	10	V
Logic 0 Input Voltage (IN_LS and IN_HS)	V_{IL}	–	–	0.8	V
Logic 1 Input Current V_{IN} = 5.0 V	I_{IN+}	 200	 –	 1000	µA
Wake-Up Input Voltage (G_EN)	V_{G_EN}	4.5	5.0	V_{CC2}	V
Wake-Up Input Current (G_EN) V_{G_EN} = 14 V	I_{G_EN}	 –	 200	 500	µA
Wake-Up Input Current (G_EN) V_{G_EN} = 28 V	I_{G_EN2}	 –	 –	 1.5	mA
LINEAR REGULATOR					
Linear Regulator V_{LR_OUT} @ V_{CC2} from 15 V to 28 V, I_{LOAD} from 0 mA to 20 mA V_{LR_OUT} @ I_{LOAD} = 20 mA V_{LR_OUT} @ I_{LOAD} = 20 mA, V_{CC2} = 5.5 V, V_{CC} = 5.5 V	V_{LR_OUT}	 12.5 V_{CC2}-1.5 4.0	 – – –	 16.5 – –	V
CHARGE PUMP					
Charge Pump Output Voltage, Reference to V_{CC} V_{CC} = 12 V, I_{LOAD} = 0 mA, C_{CP_OUT} = 1.0 µF V_{CC} = 12 V, I_{LOAD} = 7.0 mA, C_{CP_OUT} = 1.0 µF V_{CC2} = V_{CC} = 5.5 V, I_{LOAD} = 0 mA, C_{CP_OUT} = 1.0 µF V_{CC2} = V_{CC} = 5.5 V, I_{LOAD} = 7.0 mA, C_{CP_OUT} = 1.0 µF V_{CC} = 55 V, I_{LOAD} = 0 mA, C_{CP_OUT} = 1.0 µF V_{CC} = 55 V, I_{LOAD} = 7.0 mA, C_{CP_OUT} = 1.0 µF	V_{CP_OUT}	 7.5 7.0 2.3 1.8 7.5 7.0	 – – – – – –	 – – – – – –	V
Peak Current Through Pin C1 Under Rapidly Changing V_{CC} Voltages (see Figure 11, page 14)	I_{C1}	-2.0	–	2.0	A
Minimum Peak Voltage at Pin C1 Under Rapidly Changing V_{CC} Voltages (see Figure 11, page 14)	V_{C1}min	-1.5	–	–	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise noted. Typical values for T_A = 25°C and min/max values for T_A = -40°C to 125°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Quiescent V_{CC} Supply Current V_{G_EN} = 0 V and V_{CC} = 55 V V_{G_EN} = 0 V and V_{CC} = 12 V	$IV_{CCsleep}$	 – –	 – –	 10 10	µA
Operating V_{CC} Supply Current (Note 5) V_{CC} = 55 V and V_{CC2} = 28 V V_{CC} = 12 V and V_{CC2} = 12 V	IV_{CCop}	 – –	 2.2 0.7	 – –	mA
Additional Operating V_{CC} Supply Current for Each Logic Input Terminal Active V_{CC} = 55 V and V_{CC2} = 28 V (Note 6)	IV_{CClog}	–	–	5.0	mA
Quiescent V_{CC2} Supply Current V_{G_EN} = 0 V and V_{CC} = 12 V V_{G_EN} = 0 V and V_{CC} = 28 V	$IV_{CC2sleep}$	 – –	 – –	 5.0 5.0	µA
Operating V_{CC2} Supply Current (Note 5) V_{CC} = 55 V and V_{CC2} = 28 V V_{CC} = 12 V and V_{CC2} = 12 V	IV_{CC2op}	 – –	 – –	 12 9.0	mA
Additional Operating V_{CC2} Supply Current for Each Logic Input Terminal Active V_{CC} = 55 V and V_{CC2} = 28 V (Note 6)	IV_{CC2log}	–	–	5.0	mA
Undervoltage Shutdown V_{CC}	UV	4.0	5.0	5.5	V
Undervoltage Shutdown V_{CC2} (Note 7)	UV2	4.0	5.0	5.5	V
Overvoltage Shutdown V_{CC}	OV	57	61	65	V
Overvoltage Shutdown V_{CC2}	OV2	29.5	31	35	V
OUTPUT					
Output Sink Resistance (Turned Off) $I_{discharge\ LSS}$ = 50 mA, V_{SRC_HS} = 0 V (Note 8)	R_{DS}	–	–	22	Ω
Output Source Resistance (Turned On) $I_{charge\ HSS}$ = 50 mA, V_{CP_OUT} = 20 V (Note 8)	R_{DS}	–	–	22	Ω
Charge Current of the External High-Side MOSFET Through GATE_HSn Terminal (Note 8)	$I_{charge\ HSS}$	–	100	200	mA
Maximum Voltage (V_{GATE_HS} - V_{SRC_HS}) INH = Logic 1, $I_S$max = 5.0 mA	Vmax	–	–	18	V

Notes

5. Logic input terminal inactive (high impedance).
6. High-frequency PWM-ing (» 20 kHz) of the logic inputs will result in greater power dissipation within the device. Care must be taken to remain within the package power handling rating.
7. The device may exhibit predictable behavior between 4.0 V and 5.5 V.
8. See Figure 3, page 10, for a description of charge current.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise noted. Typical values for T_A = 25°C and min/max values for T_A = -40°C to 125°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING CHARACTERISTICS					
Propagation Delay High Side and Low Side C_{LOAD} = 5.0 nF, Between 50% Input to 50% Output (Note 9) (see Figure 2)	t_{pd}	–	200	300	ns
Turn-On Rise Time C_{LOAD} = 5.0 nF, 10% to 90% (Note 9), (Note 10) (see Figure 2)	t_r	–	80	180	ns
Turn-Off Fall Time C_{LOAD} = 5.0 nF, 10% to 90% (Note 9), (Note 10) (see Figure 2)	t_f	–	80	180	ns

Notes

9. C_{LOAD} corresponds to a capacitor between GATE_HS and SRC_HS for the high side and between GATE_LS and ground for low side.
10. Rise time is given by time needed to change the gate from 1.0 V to 10 V (vice versa for fall time).

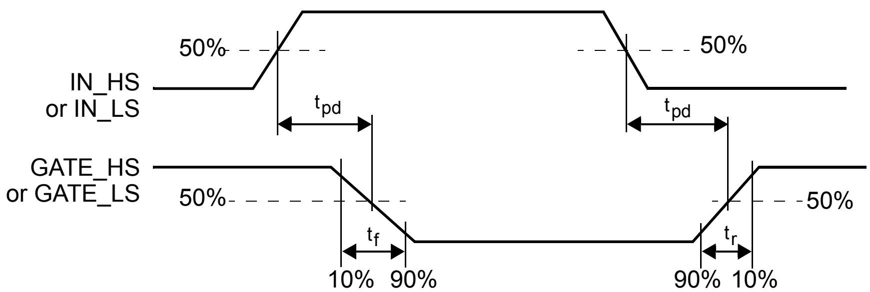


Figure 2. Timing Characteristics

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33883 is an H-bridge gate driver (or full-bridge predriver) with integrated charge pump and independent high- and low-side driver channels. It has the capability to drive large gate-charge MOSFETs and supports high PWM frequency. In sleep mode its supply current is very low.

FUNCTIONAL TERMINAL DESCRIPTION

Supply Voltage Terminals (V_{CC} and V_{CC2})

The V_{CC} and V_{CC2} terminals are the power supply inputs to the device. V_{CC} is used for the output high-side drivers and the charge pump. V_{CC2} is used for the linear regulation. They can be connected together or independent with different voltage values. The device can operate with V_{CC} up to 55 V and V_{CC2} up to 28 V.

The V_{CC} and V_{CC2} terminals have undervoltage (UV) and overvoltage (OV) shutdown. If one of the supply voltage drops below the undervoltage threshold or rises above the overvoltage threshold, the gate outputs are switched LOW in order to switch off the external MOSFETs. When the supply returns to a level that is above the UV threshold or below the OV threshold, the device resumes normal operation according to the established condition of the input terminals.

Input High- and Low-Side Terminals (IN_HSn and IN_LSn)

The IN_HSn and IN_LSn terminals are input control terminals used to control the gate outputs. These terminals are 5.0 V CMOS-compatible inputs with hysteresis. IN_HSn and IN_LSn independently control GATE_HSn and GATE_LSn, respectively.

During wake-up, the logic is supplied from the G_EN terminal. There is no internal circuit to prevent the external high-side and low-side MOSFETs from conducting at the same time.

Source Output High-Side Terminals (SRC_HSn)

The SRC_HSn terminals are the sources of the external high-side MOSFETs. The external high-side MOSFETs are controlled using the IN_HSn inputs.

Gate High- and Low-Side Terminals (GATE_HSn and GATE_LSn)

The GATE_HSn and GATE_LSn terminals are the gates of the external high- and low-side MOSFETs. The external high- and low-side MOSFETs are controlled using the IN_HSn and IN_LSn inputs.

G_EN Terminal

The G_EN terminal is used to place the device in a sleep mode. When the G_EN terminal voltage is a logic LOW state, the device is in sleep mode. The device is enabled and fully operational when the G_EN terminal voltage is logic HIGH, typically 5.0 V.

Charge Pump Out Terminal (CP_OUT)

The CP_OUT terminal is used to connect an external reservoir capacitor for the charge pump.

Charge Pump Capacitor Terminals (C1 and C2)

The C1 and C2 terminals are used to connect an external capacitor for the charge pump.

Linear Regulator Output Terminal (LR_OUT)

The LR_OUT terminal is the output of the internal regulator. It is used to connect an external capacitor.

Ground Terminals (GNDn and GND_A)

These terminals are the ground terminals of the device. They should be connected together with a very low impedance connection.

Table 1. Functional Truth Table

Conditions	G_EN	IN_HSn	IN_LSn	Gate_HSn	Gate_LSn	Comments
Sleep	0	x	x	0	0	Device is in Sleep mode. The gates are at low state.
Normal	1	1	1	1	1	Normal mode. The gates are controlled independently.
Normal	1	0	0	0	0	Normal mode. The gates are controlled independently.
Undervoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overvoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on High-Side Gate Driver	1	1	x	0	x	The device is currently in fault mode. The high-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on Low-Side Gate Driver	1	x	1	x	0	The device is currently in fault mode. The low-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.

x = Don’t care.

Driver Characteristics

Figure 3 represents the external circuit of the high-side gate driver. In the schematic, HSS represents the switch that is used to charge the external high-side MOSFET through the GATE_HS terminal. LSS represents the switch that is used to discharge the external high-side MOSFET through the GATE_HS terminal. The same schematic can be applied to the external low-side MOSFET driver simply by replacing terminal CP_OUT with terminal LR_OUT, terminal GATE_HS with terminal GATE_LS, and terminal SRC_HS with GND.

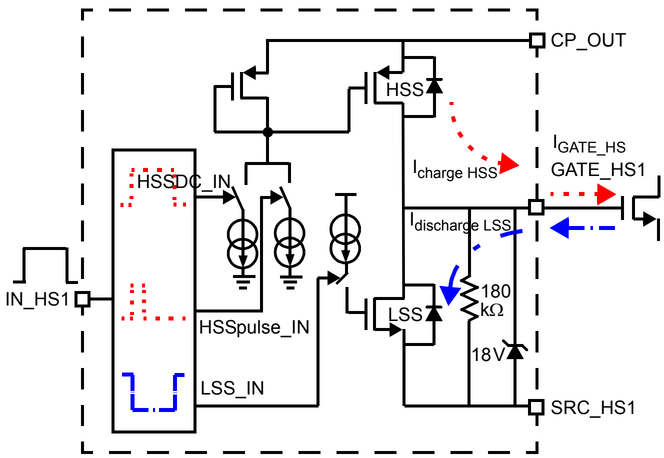
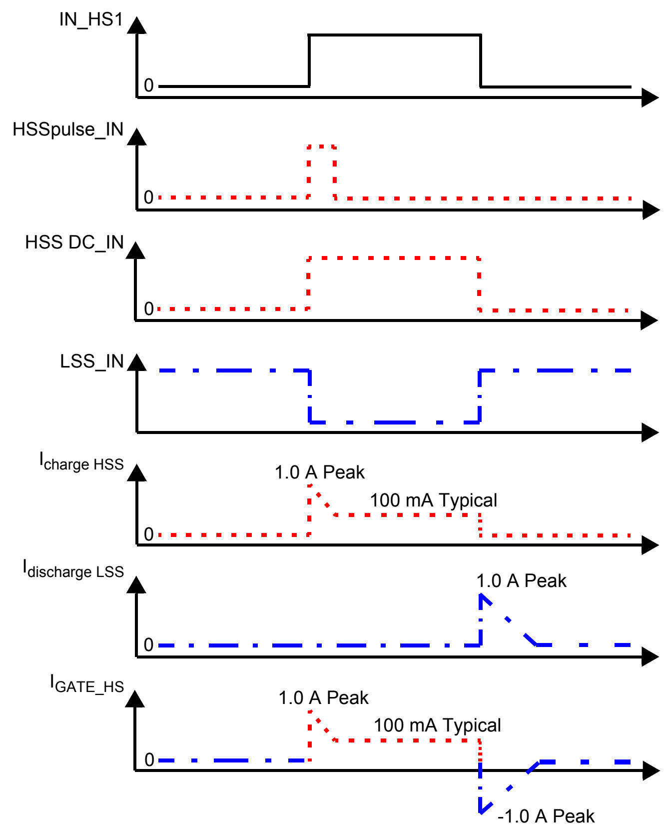


Figure 3. High-Side Gate Driver Functional Schematic

The different voltages and current of the high-side gate driver are illustrated in Figure 4. The output driver sources a peak current of up to 1.0 A for 200 ns to turn on the gate. After 200 ns, 100 mA is continuously provided to maintain the gate charged. The output driver sinks a high current to turn off the gate. This current can be up to 1.0 A peak for a 100 nF load.



Note GATE_HS is loaded with a 100 nF capacitor in the chronograms. A smaller load will give lower peak and DC charge or discharge currents.

Figure 4. High-Side Gate Driver Chronograms

APPLICATION REQUIREMENTS

Turn-On

For turn-on, the current required to charge the gate source capacitor C_{iss} in the specified time can be calculated as follows:

$$I_P = Q_g/t_r = 80\ nC/80\ ns \approx 1.0\ A$$

Where Q_g is power MOSFET gate charge and t_r is peak current for rise time.

Turn-Off

The peak current for turn-off can be obtained in the same way as for turn-on, with the exception that peak current for fall time, t_f, is substituted for t_r:

$$I_P = Q_g/t_f = 80\ nC/80\ ns \approx 1.0\ A$$

In addition to the dynamic current required to turn off or on the MOSFET, various application-related switching scenarios must be considered. These scenarios are presented in Figure 5. In order to withstand high dV/dt spikes, a low resistive path between gate and source is implemented during the OFF-state.

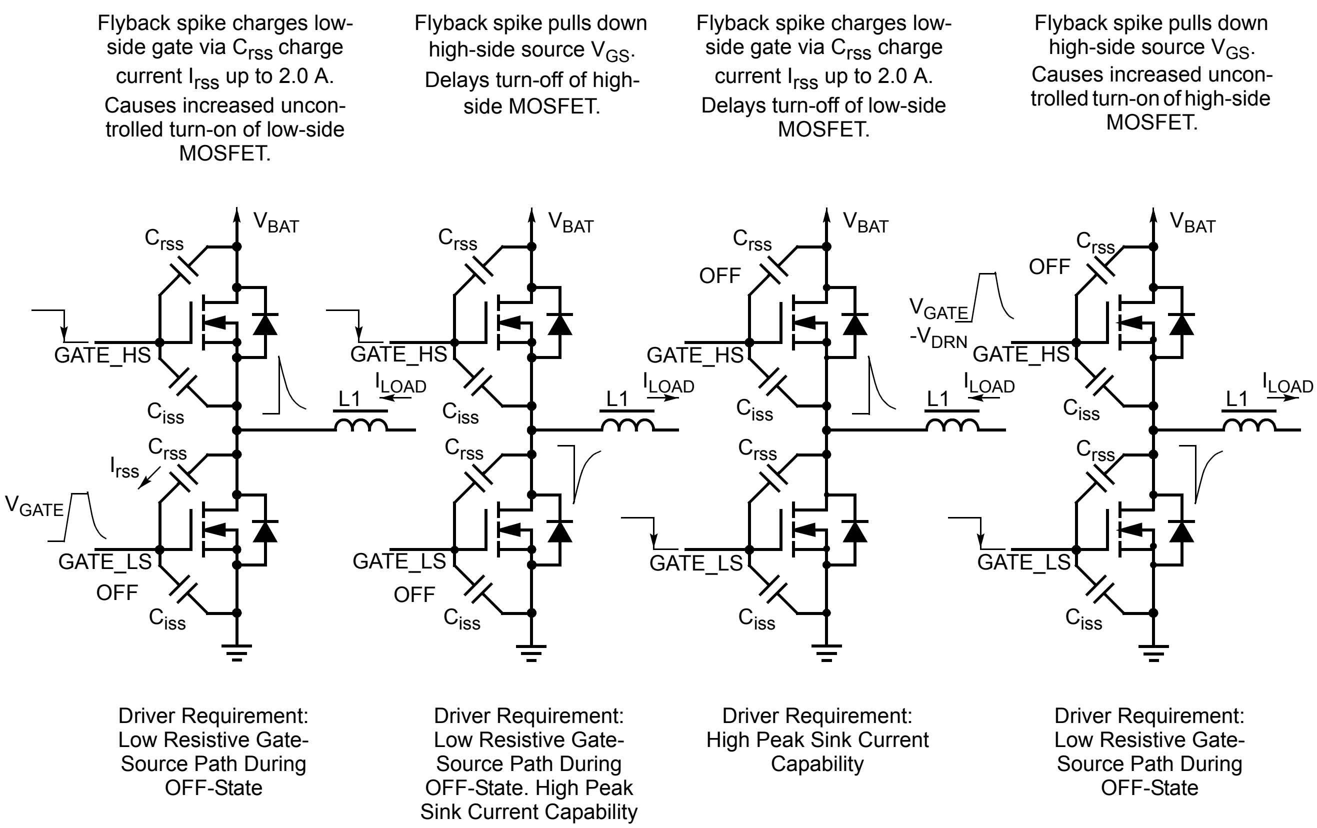


Figure 5. OFF-State Driver Requirement

Low-Drop Linear Regulator

The low-drop linear regulator is supplied by V_{CC2}. If V_{CC2} exceeds 15.0 V, the output is limited to 14.5 V (typical).

The low-drop linear regulator provides the 5.0 V for the logic section of the driver, the V_{gs_ls} buffered at LR_OUT, and the +14.5 V for the charge pump, which generates the CP_OUT The low-drop linear regulator provides 4.0 mA average current per driver stage.

In case of the full bridge, that means approximately 16 mA — 8.0 mA for the high side and 8.0 mA for the low side.

Note: The average current required to switch a gate with a frequency of 100 kHz is:

$$I_{CP} = Q_g * f_{PWM} = 80\ nC * 100\ kHz = 8.0\ mA$$

In a full-bridge application only one high side and one low side switches on or off at the same time.

Charge Pump

The charge pump generates the high-side driver supply voltage (CP_OUT), buffered at C_{CP_OUT}. Figure 6 shows the charge pump basic circuit without load.

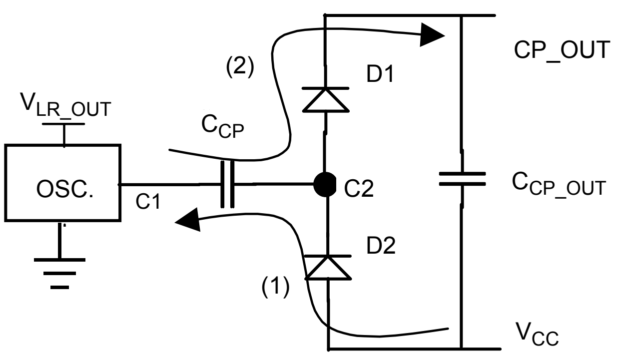


Figure 6. Charge Pump Basic Circuit

When the oscillator is in low state [(1) in Figure 6], C_{CP} is charged through D2 until its voltage reaches V_{CC} - V_{D2}. When the oscillator is in high state (2), C_{CP} is discharged though D1 in $C_{CP\_OUT,}$ and final voltage of the charge pump, V_{CP_OUT}, is V_{cc} + V_{LR_OUT} - $2V_D$. The frequency of the 33883 oscillator is about 330 kHz.

External Capacitors Choice

External capacitors on the charge pump and on the linear regulator are necessary to supply high peak current absorbed during switching.

Figure 7 represents a simplified circuitry of the high-side gate driver. Transistors Tosc1 and Tosc2 are the oscillator-switching MOSFETs. When Tosc1 is on, the oscillator is at low level. When Tosc2 is on, the oscillator is at high level. The capacitor C_{CP_OUT} provides peak current to the high-side MOSFET through HSS during turn-on (3).

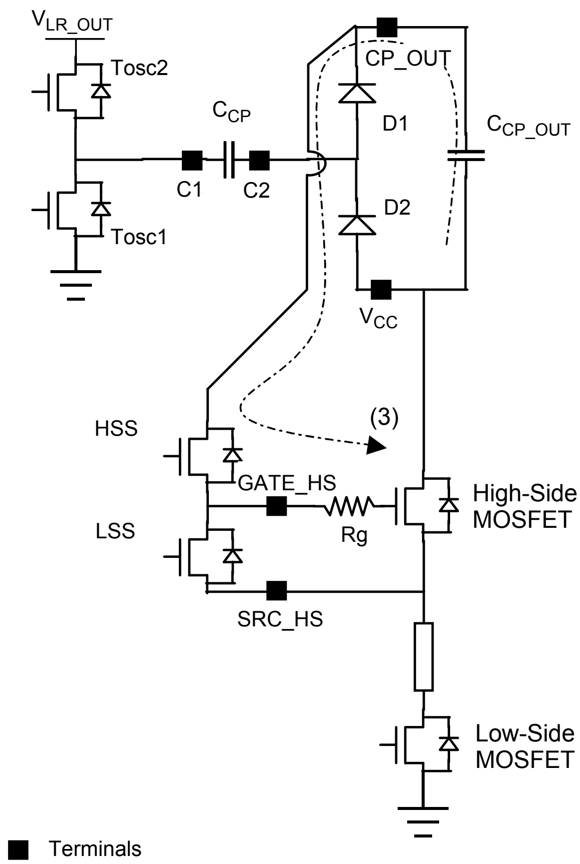
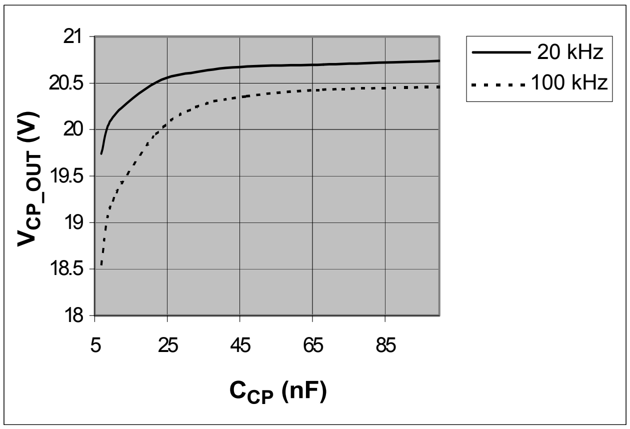


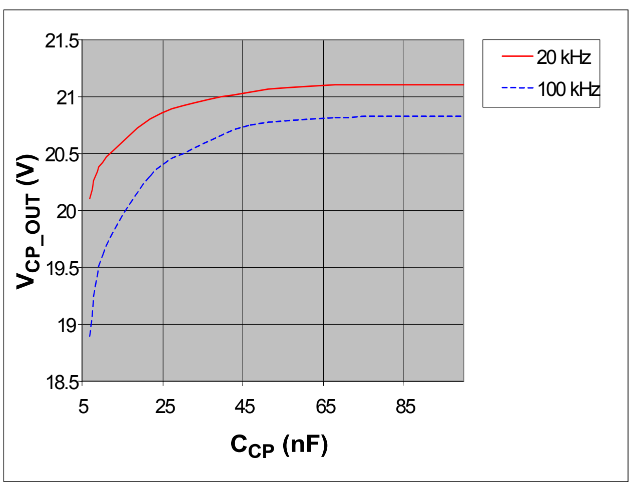
Figure 7. High-Side Gate Driver

C_{CP}

C_{CP} choice depends on power MOSFET characteristics and the working switching frequency. Figure 8 contains two diagrams that depict the influence of C_{CP} value on V_{CP_OUT} average voltage level. The diagrams represent two different frequencies for two power MOSFETs, MTP60N06HD and MPT36N06V.



MTP60N06HD (Q_g = 50 nC)



MTP36N06V (Q_g = 40 nC)

Figure 8. V_{CP_OUT} Versus C_{CP}

The smaller the C_{CP} value is, the smaller the V_{CP_OUT} value is. Moreover, for the same C_{CP} value, when the switching frequency increases, the average V_{CP_OUT} level decreases. For most of the applications, a typical value of 33 nF is recommended.

C_{CP_OUT}

Figure 9 depicts the simplified C_{CP_OUT} current and voltage waveforms. f_{PWM} is the working switching frequency.

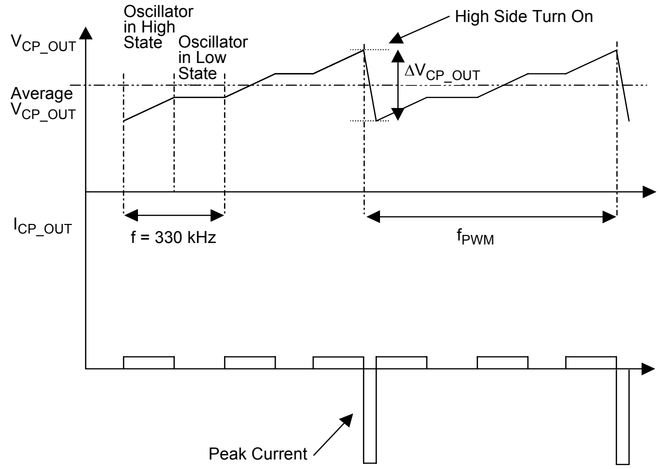


Figure 9. Simplified C_{CP_OUT} Current and Voltage Waveforms

As shown above, at high-side MOSFET turn-on V_{CP_OUT} voltage decreases. This decrease can be calculated according to the C_{CP_OUT} value as follows:

$$\Delta V_{CP\_OUT} = \frac{Q_g}{C_{CP\_OUT}}$$

Where Q_g is power MOSFET gate charge.

C_{LR_OUT}

C_{LR_OUT} provides peak current needed by the low-side MOSFET turn-on. V_{LR_OUT} decrease is as follows:

$$\Delta V_{LR\_OUT} = \frac{Q_g}{C_{LR\_OUT}}$$

Typical Values of Capacitors

In most working cases the following typical values are recommended for a well-performing charge pump:

C_{CP} = 33 nF, C_{CP_OUT} = 470 nF, and C_{LR_OUT} = 470 nF

These values give a typical 100 mV voltage ripple on V_{CP_OUT} and V_{LR_OUT} with Q_g = 50 nC.

Protection

Gate Protection

The low-side driver is supplied from the built-in low-drop regulator. The high-side driver is supplied from the internal charge pump buffered at CP_OUT.

The low-side gate is protected by the internal linear regulator, which ensures that V_{GATE_LS} does not exceed the maximum V_{GS}. Especially when working with the charge pump, the voltage at CP_OUT can be up to 65 V. The high-side gate is clamped internally in order to avoid a V_{GS} exceeding 18 V.

Gate protection does not include a flyback voltage clamp that protects the driver and the external MOSFET from a flyback voltage that can occur when driving inductive load. This flyback voltage can reach high negative voltage values and needs to be clamped externally, as shown in Figure 10.

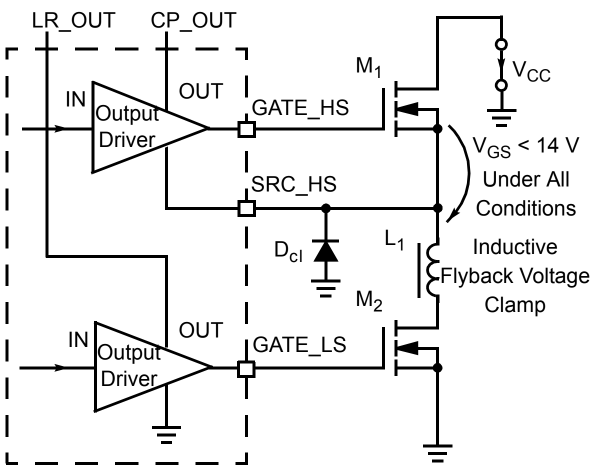


Figure 10. Gate Protection and Flyback Voltage Clamp

Load Dump and Reverse Battery

V_{CC} and V_{CC2} can sustain load a dump pulse of 40 V and double battery of 24 V. Protection against reverse polarity is ensured by the external power MOSFET with the free-wheeling diodes forming a conducting pass from ground to V_{CC}. Additional protection is not provided within the circuit. To protect the circuit an external diode can be put on the battery line. It is not recommended putting the diode on the ground line.

Temperature Protection

There is temperature shutdown protection per each half-bridge. Temperature shutdown protects the circuitry against temperature damage by switching off the output drivers. Its typical value is 175°C with an hysteresis of 15°C.

dV/dt at V_{CC}

V_{CC} voltage must be higher than (SRC_HS voltage minus a diode drop voltage) to avoid perturbation of the high-side driver.

In some applications a large dV/dt at terminal C2 owing to sudden changes at V_{CC} can cause large peak currents flowing through terminal C1, as shown in Figure 11.

For positive transitions at terminal C2, the absolute value of the minimum peak current, I_{C1}min, is specified at 2.0 A for a t_{C1}min duration of 600 ns.

For negative transitions at terminal C2, the maximum peak current, I_{C1}max, is specified at 2.0 A for a t_{C1}max duration of 600 ns. Current sourced by terminal C1 during a large dV/dt will result in a negative voltage at terminal C1 (Figure 11). The minimum peak voltage V_{C1}min is specified at -1.5 V for a duration of t_{C1}max = 600 ns. A series resistor with the charge pump capacitor (Ccp) capacitor can be added in order to limit the surge current.

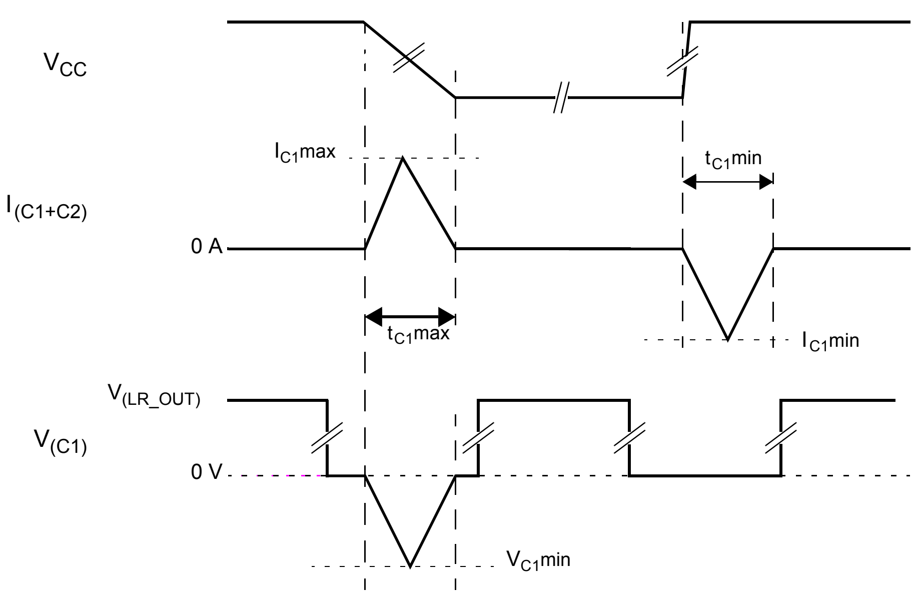


Figure 11. Limits of C1 Current and Voltage with Large Values of dV/dt

In the case of rapidly changing V_{CC} voltages, the large dV/dt may result in perturbations of the high-side driver, thereby forcing the driver into an OFF state. The addition of capacitors C3 and C4, as shown in Figure 12, reduces the dV/dt of the source line, consequently reducing driver perturbation. Typical values for R3/R4 and C3/C4 are 10 Ω and 10 nF, respectively.

dV/dt at V_{CC2}

When the external high-side MOSFET is on, in case of rapid negative change of V_{CC2} the voltage (V_{GATE_HS} - V_{SRC_HS}) can be higher than the specified 18 V. In this case a resistance in the SRC line is necessary to limit the current to 5.0 mA max. It will protect the internal zener placed between GATE_HS and SRC terminals.

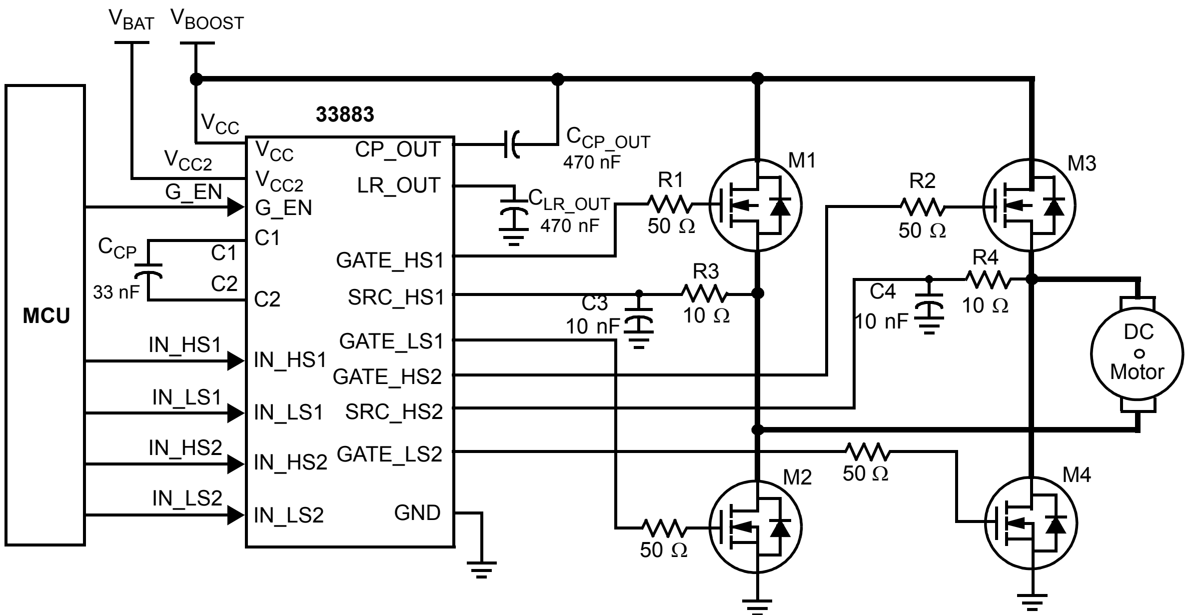
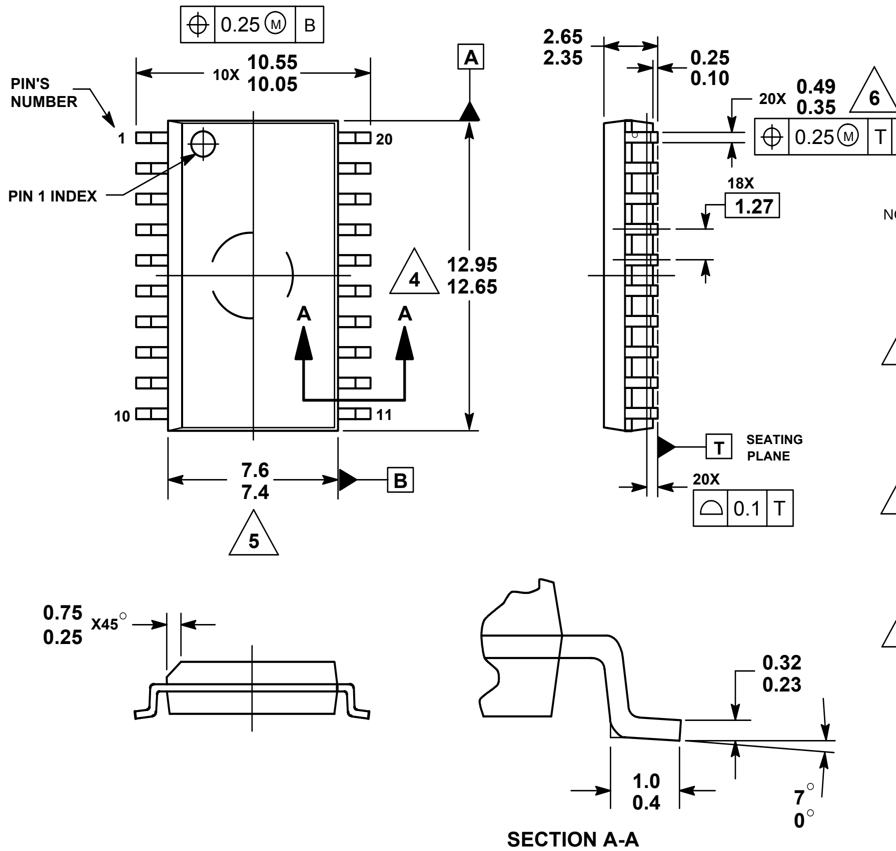


Figure 12. Application Schematic with External Protection Circuit

PACKAGE DIMENSIONS

DW SUFFIX
20-TERMINAL SOICW
PLASTIC PACKAGE
CASE 751D-06
ISSUE H



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62mm.

NOTES

NOTES

NOTES

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:
Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center
3-20-1 Minami-Azabu. Minato-ku, Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE: http://motorola.com/semiconductors