

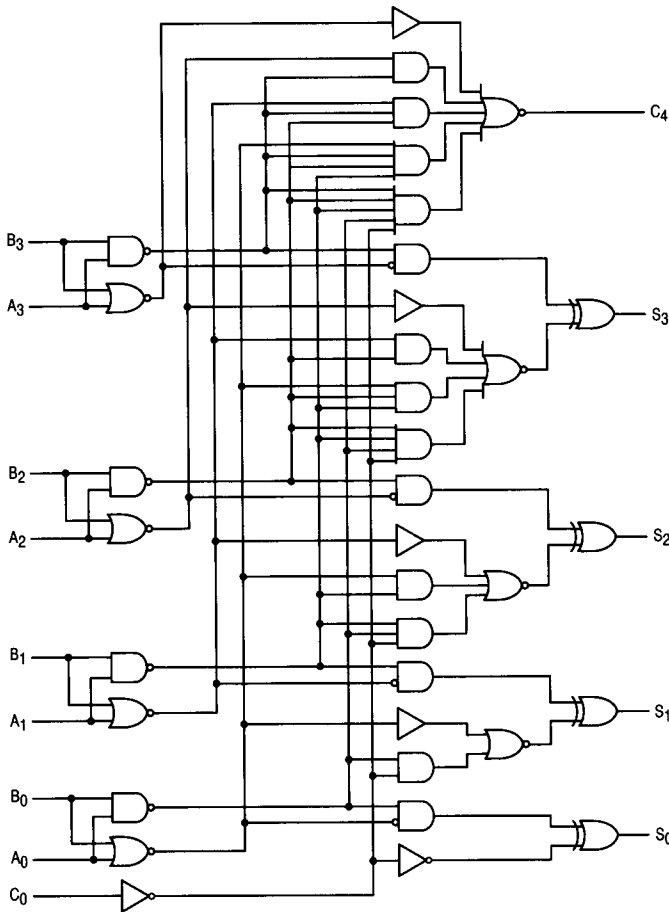


# 4-Bit Binary Full Adder With Fast Carry

ELECTRICALLY TESTED PER:  
MIL-M-38510/34201

The 54F283 high-speed 4-bit binary full adder with internal carry look-ahead accepts two 4-bit binary words (A<sub>0</sub>-A<sub>3</sub>, B<sub>0</sub>-B<sub>3</sub>) and a Carry input (C<sub>0</sub>). It generates the binary Sum outputs (S<sub>0</sub>-S<sub>3</sub>) and the Carry output (C<sub>4</sub>) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

LOGIC DIAGRAM



**Military 54F283**



AVAILABLE AS:

- 1) JAN: JM38510/34201BXA
- 2) SMD: N/A
- 3) 883: 54F283/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: E  
CERFLAT: F  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S <sub>1</sub>	1	1	2	OPEN
B <sub>1</sub>	2	2	3	VCC
A <sub>1</sub>	3	3	4	VCC
C <sub>0</sub>	4	4	5	OPEN
A <sub>0</sub>	5	5	7	VCC
B <sub>0</sub>	6	6	8	VCC
C <sub>0</sub>	7	7	9	OPEN
GND	8	8	10	GND
C <sub>4</sub>	9	9	12	OPEN
S <sub>3</sub>	10	10	13	OPEN
B <sub>3</sub>	11	11	14	VCC
A <sub>3</sub>	12	12	15	VCC
S <sub>2</sub>	13	13	17	OPEN
A <sub>2</sub>	14	14	18	VCC
B <sub>2</sub>	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

Pin Name	Equivalent	Description
A <sub>0</sub> -A <sub>3</sub>	(A1-A4)	A Operand Inputs
B <sub>0</sub> -B <sub>3</sub>	(B1-B4)	B Operand Inputs
C <sub>0</sub>		Carry Input
S <sub>0</sub> -S <sub>3</sub>	(Σ)	Sum Outputs
C <sub>4</sub>		Carry Outputs

## FUNCTIONAL DESCRIPTION

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming carry  $C_0$ . The binary sum appears on the Sum ( $S_0$ - $S_3$ ) and outgoing carry ( $C_4$ ) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

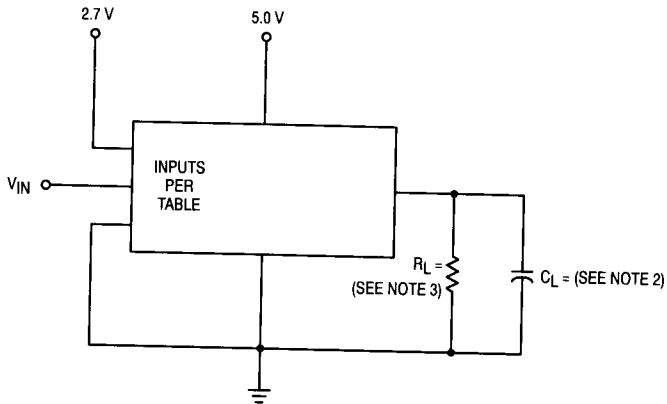
Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus  $C_0$ ,  $A_0$ ,  $B_0$  can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if  $C_0$  is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However,

other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $S_3$  dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $S_2$ ) is used merely as a means of getting a carry ( $C_{10}$ ) signal into the fourth stage (via  $A_2$  and  $B_2$ ) and bringing out the carry from the second stage on  $S_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, whether HIGH or LOW, they do not influence  $S_2$ . Similarly, when  $A_2$  and  $B_2$  are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1$ - $I_5$  that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1$ - $I_5$  are true, the output  $M_5$  is true.

## AC TEST CIRCUIT



## NOTES:

- $t_f = t_r \leq 2.5$  ns,  $PRR \leq 1.0$  MHz,  $Z_{OUT} \approx 50 \Omega$ .
- $C_L = 50$  pF  $\pm 10\%$ , including scope probe, wiring and stray capacitance without package in test fixture.
- $R_L = 499 \Omega \pm 5.0\%$ .
- Voltage measurements are to be made with respect to network ground terminal.
- Terminal conditions (pins not designated may be high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

## SWITCHING WAVEFORMS

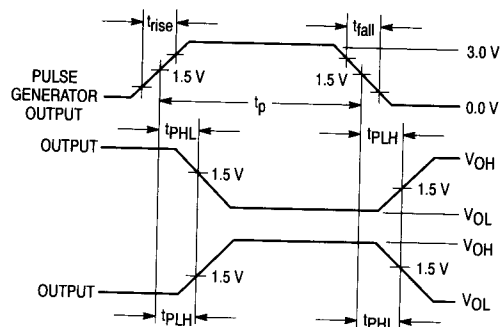


Figure A. Active-HIGH versus Active-LOW Interpretation

	C <sub>0</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	C <sub>4</sub>
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16

Active LOW: 1 + 5 + 6 = 12 + 0

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA, V <sub>IH</sub> = 2.0 V (all inputs).
V <sub>OL</sub>	Logical "0" Output Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IL</sub> = 0.8 V (all inputs).
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs = GND.
I <sub>IHH</sub>	Logical "0" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, other inputs = GND.
I <sub>OS</sub>	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs), V <sub>OUT</sub> = GND.
I <sub>IL</sub>	Logical "0" Input Current	-0.06	-1.2	-0.06	-1.2	-0.06	-1.2	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs = 5.5 V.
I <sub>IL(C<sub>0</sub>)</sub>	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs are open.
I <sub>CCL</sub>	Power Supply Current		55		55		55	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND (all inputs).
I <sub>CCZ</sub>	Power Supply Current Off		55		55		55	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (A inputs only), other inputs = GND.
I <sub>CCH</sub>	Power Supply Current Off		55		55		55	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V (all inputs).
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at) V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

## 54F283

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub>	Propagation Delay /Data-Output C <sub>0</sub> to S <sub>n</sub>	1.5	9.5	1.0	14	1.0	14	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PLH1</sub>	Propagation Delay /Data-Output C <sub>0</sub> to S <sub>n</sub>	1.5	9.5	1.0	14	1.0	14	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PHL2</sub>	Propagation Delay /Data-Output C <sub>0</sub> to C <sub>4</sub>	1.5	7.0	1.0	10	1.0	10	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PLH2</sub>	Propagation Delay /Data-Output C <sub>0</sub> to C <sub>4</sub>	1.5	7.5	1.0	10.5	1.0	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PHL3</sub>	Propagation Delay /Data-Output A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	1.5	9.5	1.0	14	1.0	14	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PLH3</sub>	Propagation Delay /Data-Output A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	1.5	9.5	1.0	14	1.0	14	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PHL4</sub>	Propagation Delay /Data-Output A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	1.5	7.0	1.0	10.5	1.0	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω
t <sub>PLH4</sub>	Propagation Delay /Data-Output A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	1.5	7.5	1.0	10.5	1.0	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω

Figure B. 3-Bit Adder

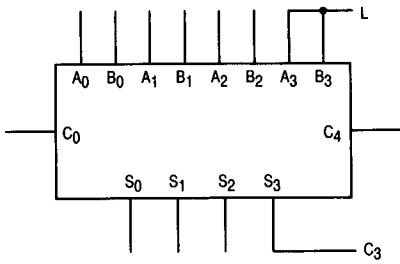


Figure C. 2-Bit and 1-Bit Adder

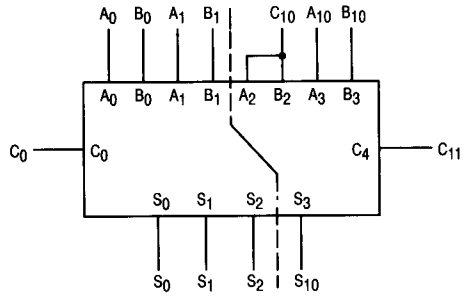


Figure D. 5 Input Encoder

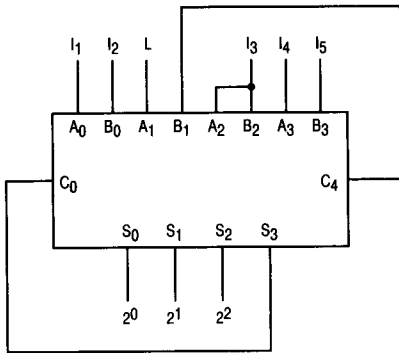


Figure E. 5 Input Majority Gate

