

**PRELIMINARY**

Notice: This is not a final specification  
Some parametric limits are subject to change

MITSUBISHI ALSTTLs  
**M74ALS649P**

T-52-31

**OCTAL BUS TRANSCEIVER/REGISTER WITH OPEN COLLECTOR OUTPUT (INVERTED)**

6249827 MITSUBISHI (DGTL LOGIC)

91D 12670 D

**DESCRIPTION**

The M74ALS649P is a semiconductor integrated circuit consisting of eight bus transceiver/registers with inverted open collector outputs.

**FEATURES**

- Bidirectional transfer or latch of two 8-bit data
- Open collector output
- Independent registers for A and B buses
- Independent clock inputs ( $T_{AB}$ ,  $T_{BA}$ )
- High fan-out ( $I_{OL}=24mA$ )
- Wide operating temperature range ( $T_a=-20\sim+75^{\circ}C$ )

**APPLICATION**

General purpose, for use in industrial and consumer digital equipment.

**FUNCTION**

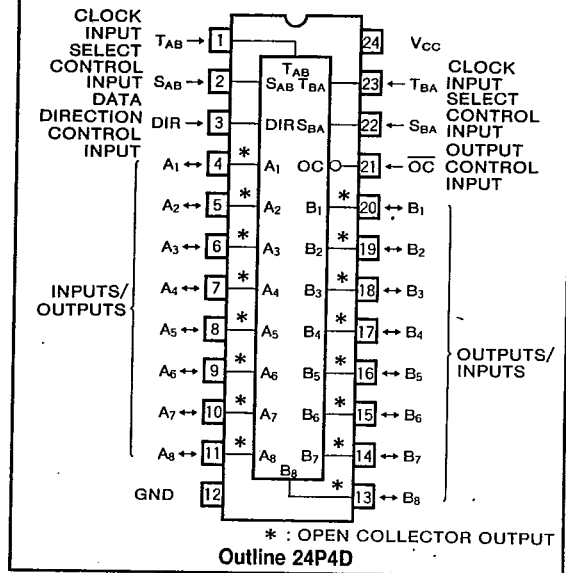
Each transceiver consists of two buffer/ register circuits with inverted open-collector outputs. The inputs and outputs are interconnected, allowing bidirectional operation.

Clock inputs  $T_{AB}$  and  $T_{BA}$  store the data signals at A and B, regardless of other inputs. When  $T_{AB}$  changes from low to high, the data at A is stored in flip-flop A; when  $T_{BA}$  changes from low to high, the data at B is stored in flip-flop B.

When output control input  $\overline{OC}$  is high, A and B are isolated. In this state, the data in flip-flop A and B are held internally until the next time  $T_{AB}$  or  $T_{BA}$  activate the store operation.

When  $\overline{OC}$  is low,  $S_{AB}$  and  $S_{BA}$  are used to select buffer or data readout operations. The Input/Output direction is controlled by data direction control input DIR.

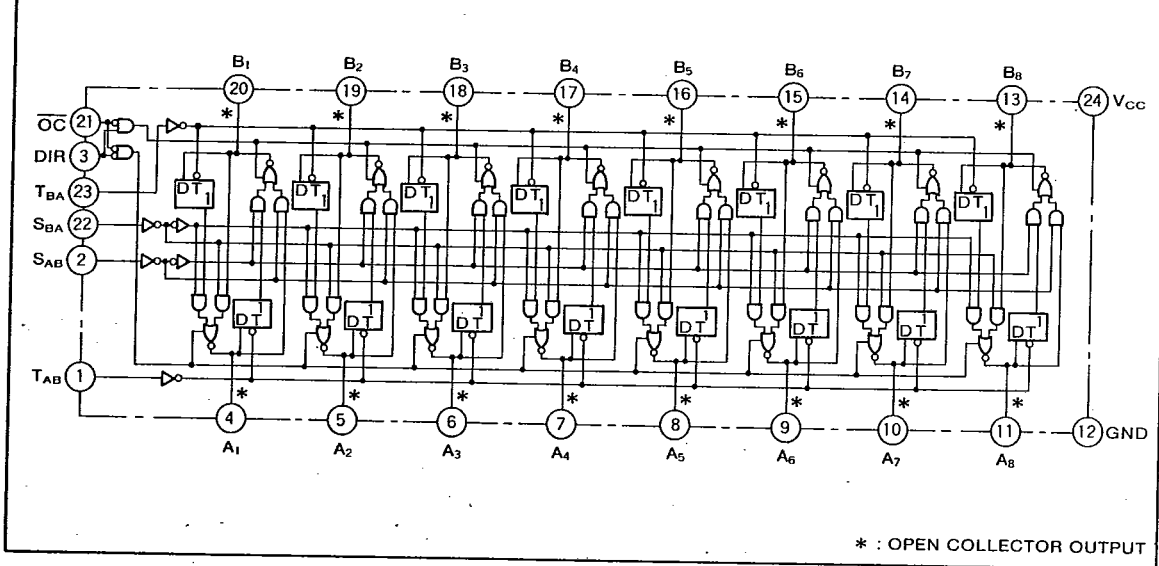
**PIN CONFIGURATION (TOP VIEW)**



When DIR is high, pins A are made the input pins and pins B are made the output pins.  $S_{AB}$  is set high to transfer data signals from A to B (inverting buffer operation), and set low to transfer the inverting data stored in flip-flop A to B bus (readout operation).

When DIR is low, pins B are made the input pins and pins A are made the output pins.  $S_{BA}$  is set high to transfer data from B to A (inverting buffer operation), and set low to transfer the inverting data stored in flip-flop B to A bus (readout operation).

**LOGIC DIAGRAM**



**OCTAL BUS TRANSCEIVER/REGISTER WITH OPEN COLLECTOR OUTPUT (INVERTED)**

**FUNCTION TABLE** (Note 1)

Inputs						Input/Output		Function
OC	DIR	T <sub>AB</sub>	T <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A	B	
X	X	↑	X	X	X	I	B <sup>0</sup>	Store
X	X	X	↑	X	X	A <sup>0</sup>	I	
H	X	↑	↑	X	X	I	I	
H	X	H or L	H or L	X	X	I	I	Hold (A and B are isolated)
L	L	X	X	X	L	$\overline{O}$	I	Buffer
L	L	X	H or L	X	H	$\overline{O}$	I	Read
L	H	X	X	L	X	I	$\overline{O}$	Buffer
L	H	H or L	X	H	X	I	$\overline{O}$	Read

Note 1. I : Input pin

$\overline{O}$  : Output pin (inverted output)

↑ : Transition from low to high (positive-edge trigger)

X : Irrelevant

A<sup>0</sup>, B<sup>0</sup> : The data output functions may be enabled or disabled by various signals at  $\overline{OC}$  and DIR. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

**ABSOLUTE MAXIMUM RATINGS** (T<sub>a</sub> = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.5~+7	V
V <sub>I</sub>	Input voltage	A, B	-0.5~+7	V
		DIR, $\overline{OC}$ , T <sub>AB</sub> , T <sub>BA</sub> , S <sub>AB</sub> , S <sub>BA</sub>	-0.5~+7	V
V <sub>O</sub>	Output voltage	High-level state	-0.5~+7	V
T <sub>opr</sub>	Operating free-air ambient temperature range		-20~+75	°C
T <sub>stg</sub>	Storage temperature range		-65~+150	°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>OH</sub>	High-level output voltage			5.5	V
I <sub>OL</sub>	Low-level output current	0		24	mA
T <sub>opr</sub>	Operating free-air ambient temperature range	-20		+75	°C

**OCTAL BUS TRANSCEIVER/REGISTER WITH OPEN COLLECTOR OUTPUT (INVERTED)**

**ELECTRICAL CHARACTERISTICS** ( $T_a = -20 \sim +75^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{IC}$	Input clamp voltage	$V_{CC}=4.5\text{V}, I_{IC}=-18\text{mA}$			-1.2	V
$I_{OH}$	High-level output current	$V_{CC}=4.5\text{V}, V_O=5.5\text{V}$			0.1	mA
$V_{OL}$	Low-level output voltage	$V_{CC}=4.5\text{V}$	$I_{OL}=12\text{mA}$		0.25	0.4
			$I_{OL}=24\text{mA}$		0.35	0.5
$I_I$	Input current at maximum voltage	DIR, OC, $T_{AB}, T_{BA}, S_{AB}, S_{BA}$ A, B	$V_{CC}=5.5\text{V}, V_I=7\text{V}$		0.1	
			$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$		0.1	
$I_{IH}$	High-level input current (Note 2)	DIR, OC, $T_{AB}, T_{BA}, S_{AB}, S_{BA}$ A, B	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$		20	
			$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$		20	
$I_{IL}$	Low-level input current (Note 3)	DIR, OC, $T_{AB}, T_{BA}, S_{AB}, S_{BA}$ A, B	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$		-0.2	
					-0.2	
$I_{CCH}$	Supply current, all outputs high	$V_{CC}=5.5\text{V}$		40	60	mA
$I_{CCL}$	Supply current, all outputs low	$V_{CC}=5.5\text{V}$		45	70	mA
$I_{CCZ}$	Supply current, all outputs disabled	$V_{CC}=5.5\text{V}$		45	70	mA

\*: All typical values are at  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ .

Note 2. For A and B,  $I_{IH}$  includes off-state high-level output current  $I_{OZH}$ .

Note 3. For A and B,  $I_{IL}$  includes off-state low-level output current  $I_{OZL}$ .

**SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test conditions/Limits (Note 6)									Unit	
				$V_{CC}=5\text{V}$	$V_{CC}=4.5\sim 5.5\text{V}$							
				$C_L=15\text{pF}$	$C_L=50\text{pF}$							
				$R_L=680\Omega$	$R_L=680\Omega$							
				$T_a=25^\circ\text{C}$			$T_a=0\sim 70^\circ\text{C}$			$T_a=-20\sim +75^\circ\text{C}$		
		Inputs	Outputs	Typ	Min	Typ*	Max	Min	Typ*	Max		
$f_{max}$	Maximum clock frequency	$T_{BA}, T_{AB}$	A, B		30			28			MHz	
$t_{PLH}$	Propagation time	$T_{BA}, T_{AB}$	A, B		19		.62	19		63	ns	
$t_{PHL}$			A, B		6		20	6		21	ns	
$t_{PLH}$		A, B	B, A		13		50	13		51	ns	
$t_{PHL}$						2		10	2		11	ns
$t_{PLH}$	Propagation time (Note 4)	$S_{BA}, S_{AB}$	A, B		20		55	20		56	ns	
$t_{PHL}$						6		22	6		23	ns
$t_{PLH}$	Propagation time (Note 5)	$S_{BA}, S_{AB}$	A, B		20		55	20		56	ns	
$t_{PHL}$						6		22	6		23	ns
$t_{PLH}$	Propagation time	$\overline{\text{OC}}$	A, B		8		25	8		26	ns	
$t_{PHL}$						2		20	2		21	ns
$t_{PLH}$		DIR	A, B		8		25	8		26	ns	
$t_{PHL}$						2		20	2		21	ns

\*: All typical values are at  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ .

Note 4. These parameters are measured when B or A is low.

Note 5. These parameters are measured when B or A is high.

**TIMING REQUIREMENT** ( $V_{CC}=4.5\text{V}\sim 5.5\text{V}, C_L=50\text{pF}, R_L=680\Omega$ )

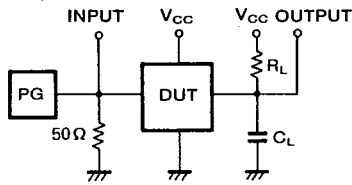
Symbol	Parameter	Limits						Unit		
		$T_a=0\sim 70^\circ\text{C}$			$T_a=-20\sim +75^\circ\text{C}$					
		Min	Typ*	Max	Min	Typ*	Max			
$t_{W(TH)}$	Pulse width	$T_{AB}, T_{BA}$ "H"		16.5			17.5			ns
$t_{W(TL)}$		$T_{AB}, T_{BA}$ "L"		16.5			17.5			
$t_{SU(D)}$	Setup time before T $\uparrow$	A, B		10			11			ns
$t_{H(D)}$	Hold time after T $\uparrow$	A, B		0			1			ns

\*: All typical values are at  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ .

†: Transition from low to high.

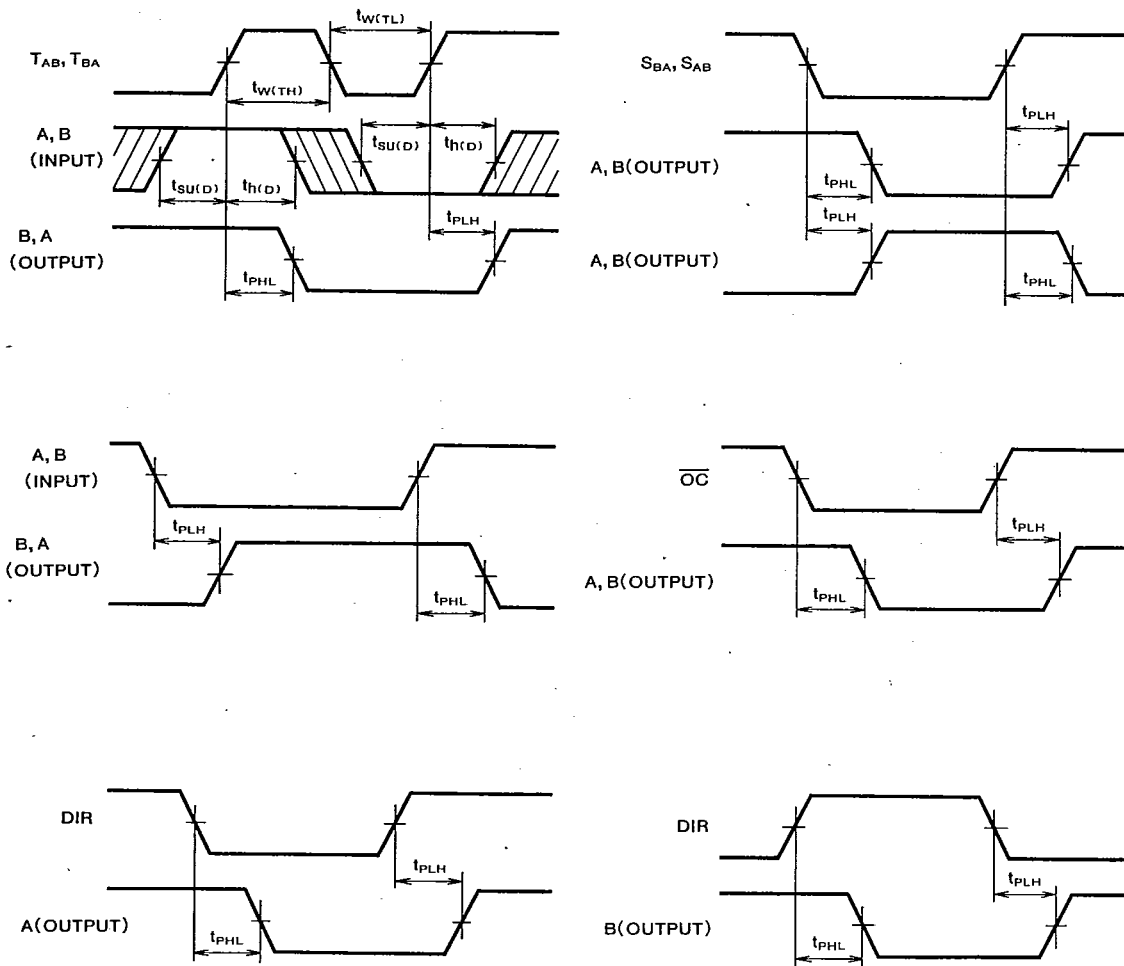
**OCTAL BUS TRANSCEIVER/REGISTER WITH OPEN COLLECTOR OUTPUT (INVERTED)**

Note 6: Measurement circuit



- (1) The pulse generator (PG) has the following characteristics:  
 $PRR \leq 1\text{MHz}$   
 $t_r = 2\text{ns}, t_f = 2\text{ns}$   
 $V_{IH} = 3.5\text{V}, V_{IL} = 0.3\text{V}$   
 duty cycle = 50%  
 $Z_o = 50\Omega$
- (2)  $C_L$  includes probe and jig capacitance.

**TIMING DIAGRAM (Reference level = 1.3V)**



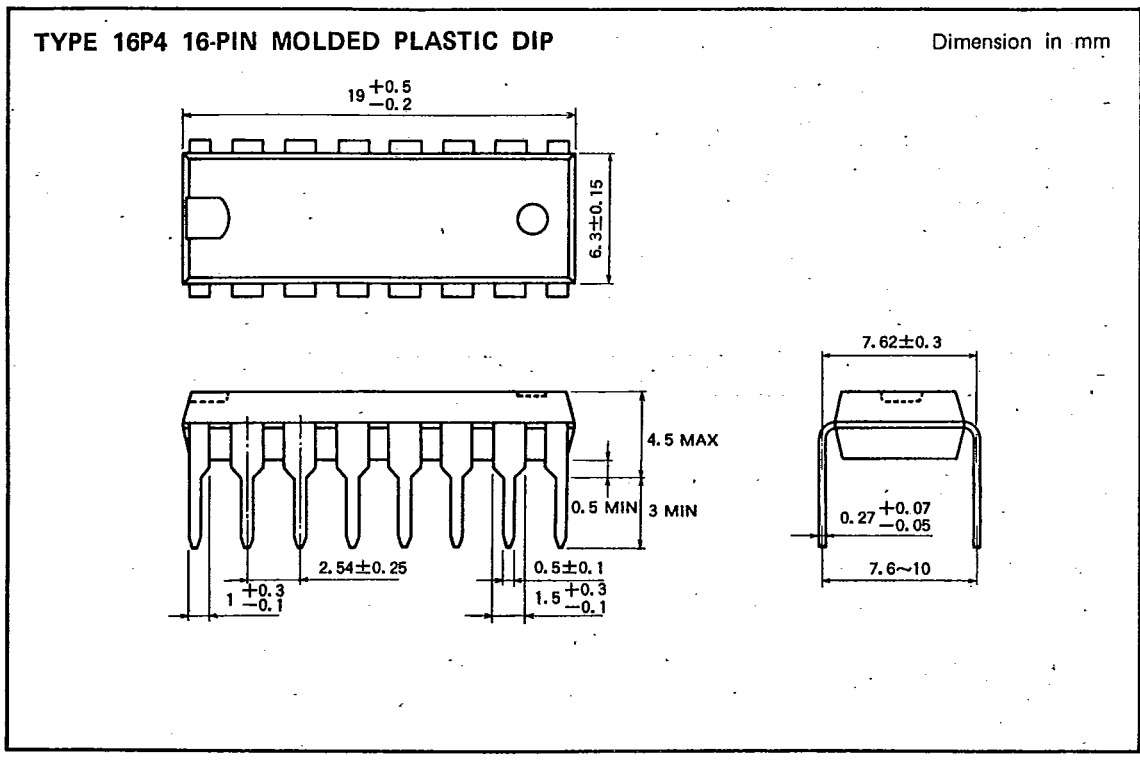
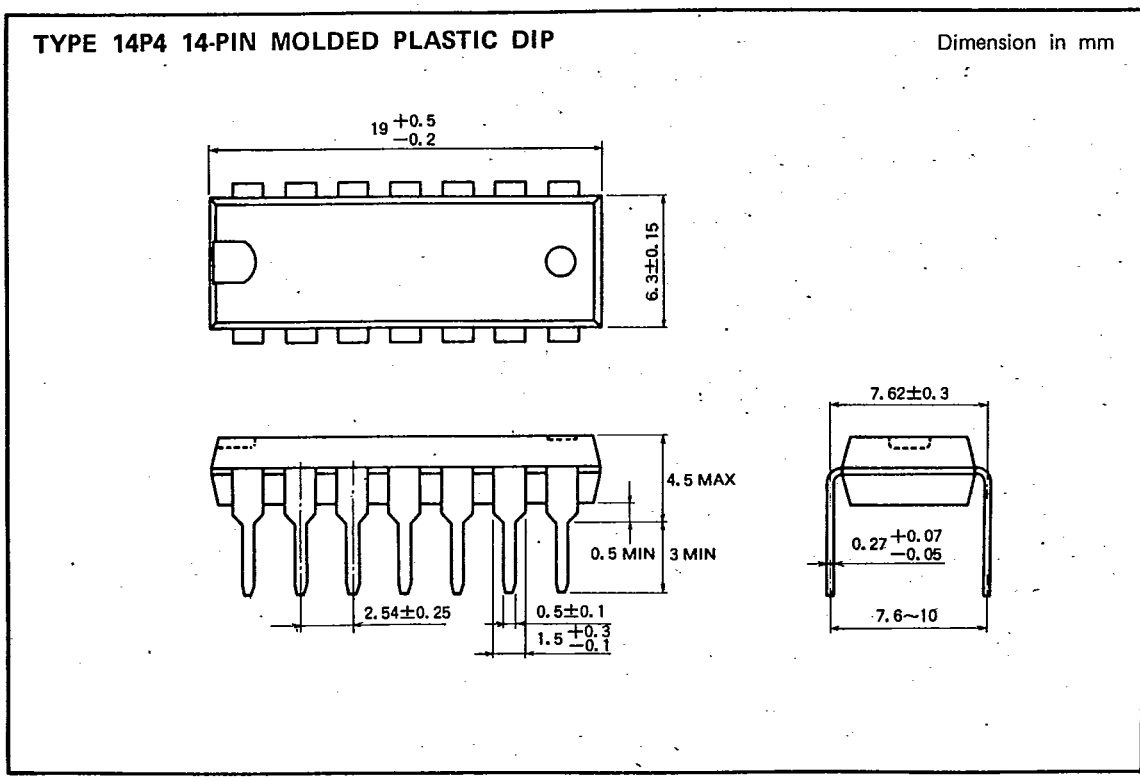
Note 7: The shaded area indicate the period when the input is permitted to change for predictable output performance.

PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC}

91D 12323

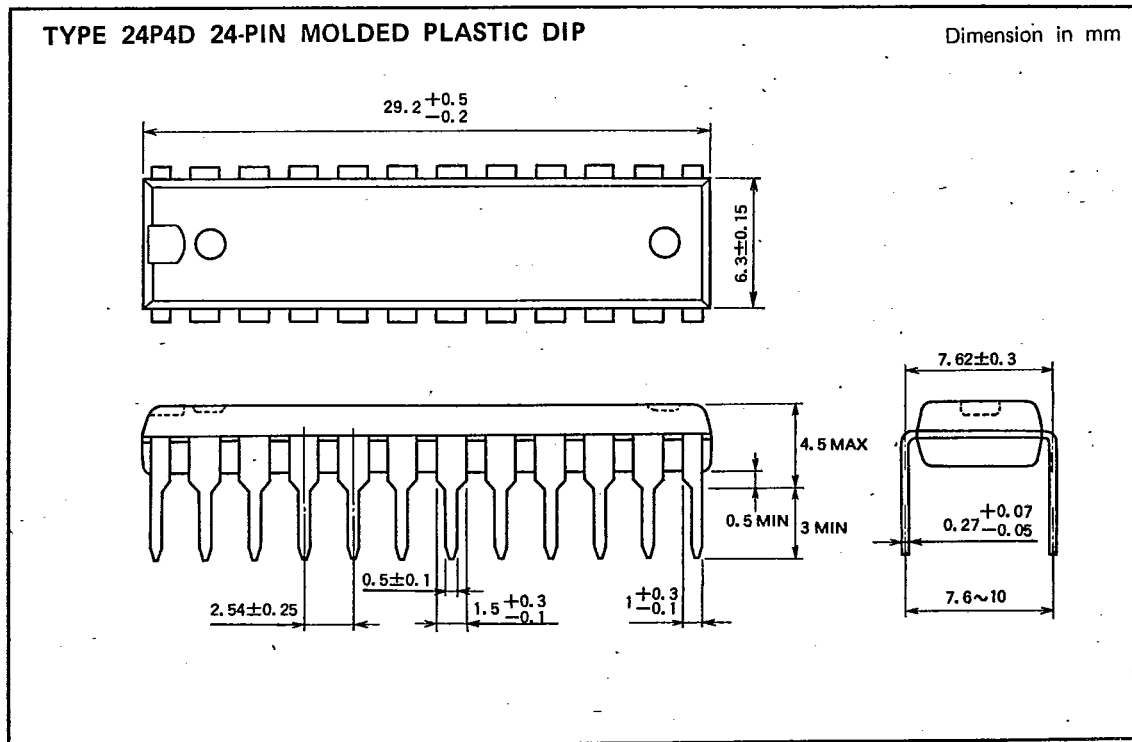
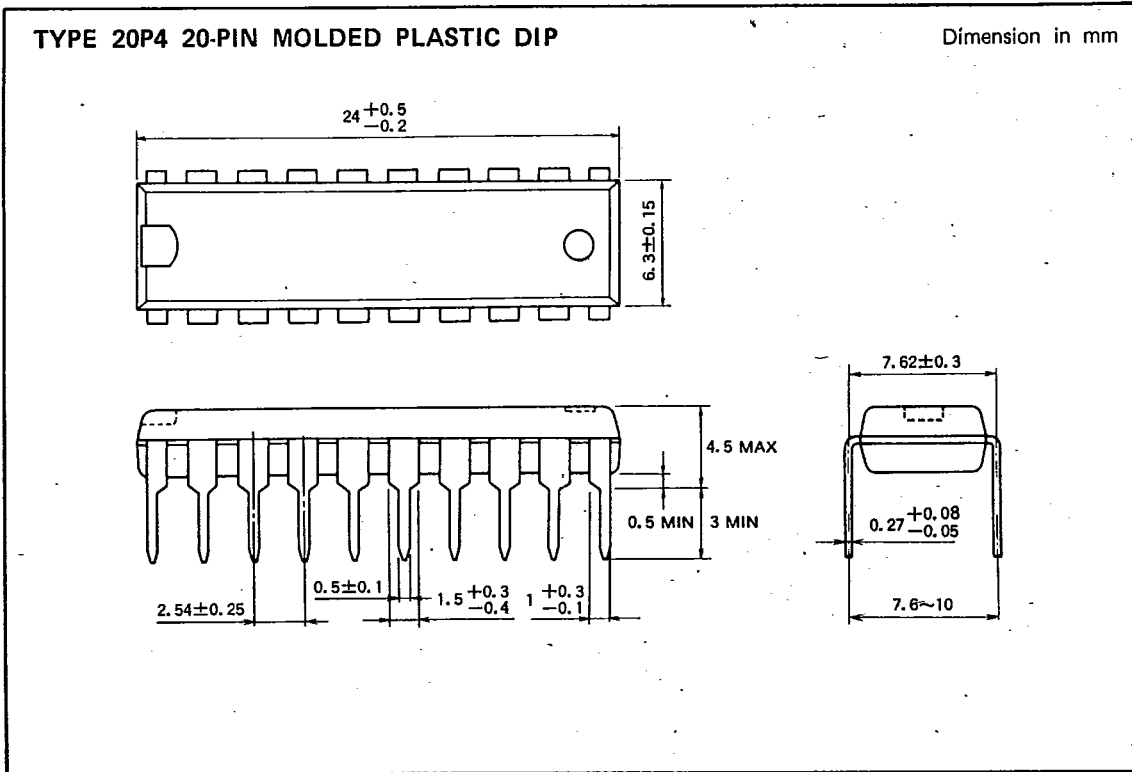
D T-9020



PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12324 D T-90-20



**TYPE DESIGNATION TABLE**

MITSUBISHI (DCTL LOGIC)

91D D ■ 6249827 0012784 7 ■ MIT3

T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type	Circuit function	Package Outlines
M74ALS00ADP	★ Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	★ Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	★ Hex Inverter	14P2P
M74ALS05ADP	★★ Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	★ Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	★★ Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	★ Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	★ Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	★★ Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	★★ Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	★★ Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	★ Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	★★ Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	★★ Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	★ Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	★★ Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	★ Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	★★ 3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	★ 3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	★★ Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	★ Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	★★ Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	★★ Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	★★ Synchronous 4-Bit Binary Counter	16P2P
M74ALS174ADP	★ Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	★★ Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	★★ Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	★ Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	★ Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	★★ Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	★★ Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	★ Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	★★ Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	★★ 8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	★★ Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	★★ Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	★★ Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	★★ Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	★★ Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	★★ Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	★★ Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	★★ Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	★★ Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	★★ Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	★★ Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	★★ Hex Noninverting Buffer	14P2P

★: New product   ★★: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

**DESCRIPTION**

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012785 9 ■ MIT3

T-90-20

**DESCRIPTION**

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

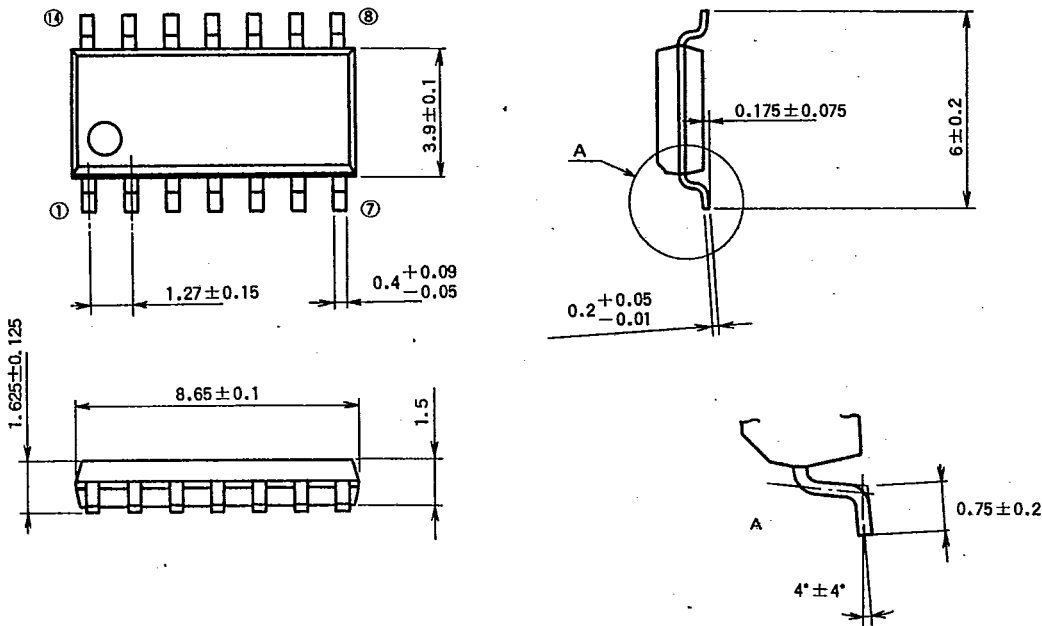
MITSUBISHI ALSTTLs  
**PACKAGE OUTLINES**

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012786 0 ■ MIT3

T-90-20

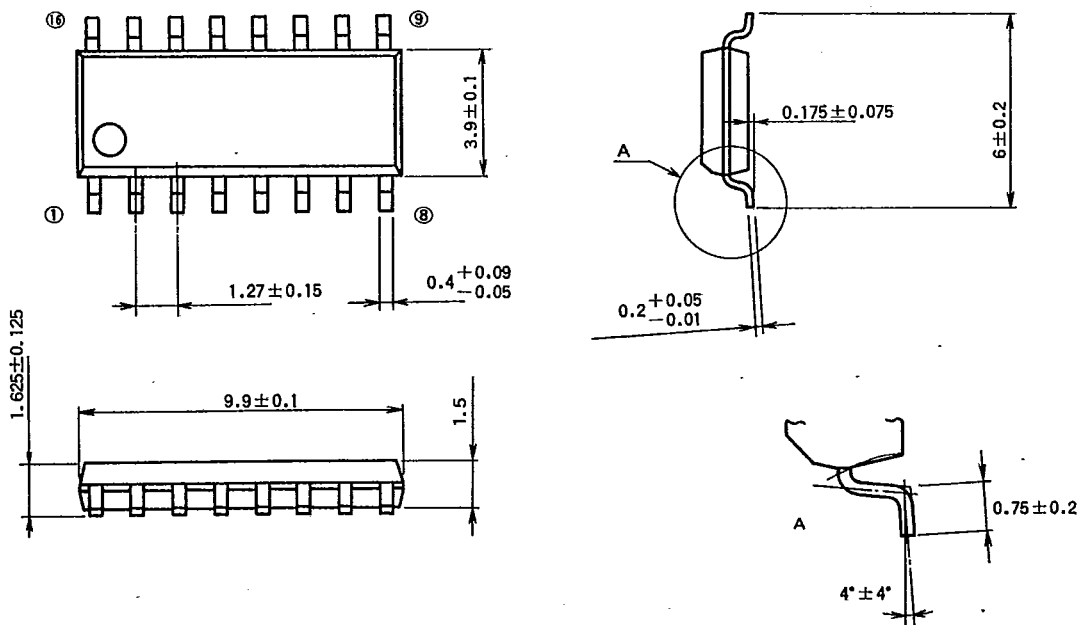
**TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)**

Dimension in mm



**TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)**

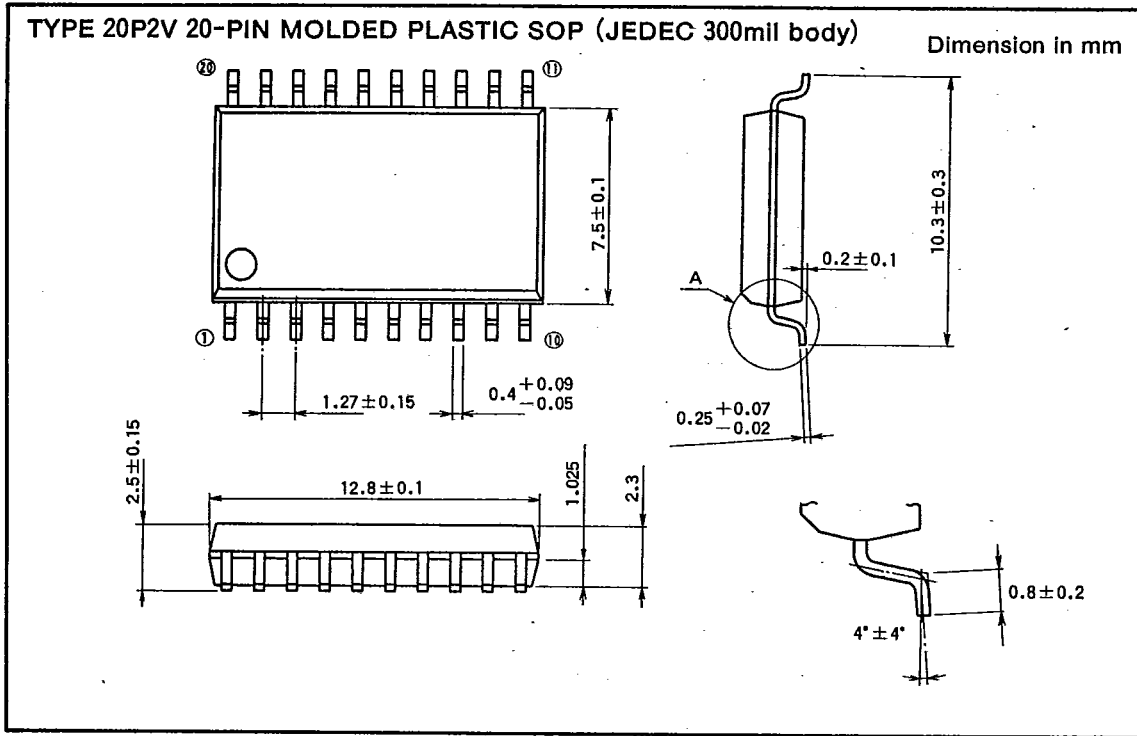
Dimension in mm



MITSUBISHI ALSTTLs  
**PACKAGE OUTLINES**

MITSUBISHI (DGTL LOGIC) 9LD D ■ 6249827 0012787 2 ■ MIT3

T-90-20



1146 E-07

3-6

