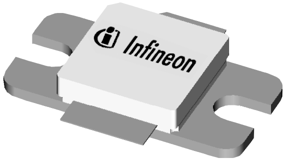
Thermally-Enhanced High Power RF LDMOS FETs
30 Watt, 1805 – 1880 MHz, 1930 – 1990 MHz

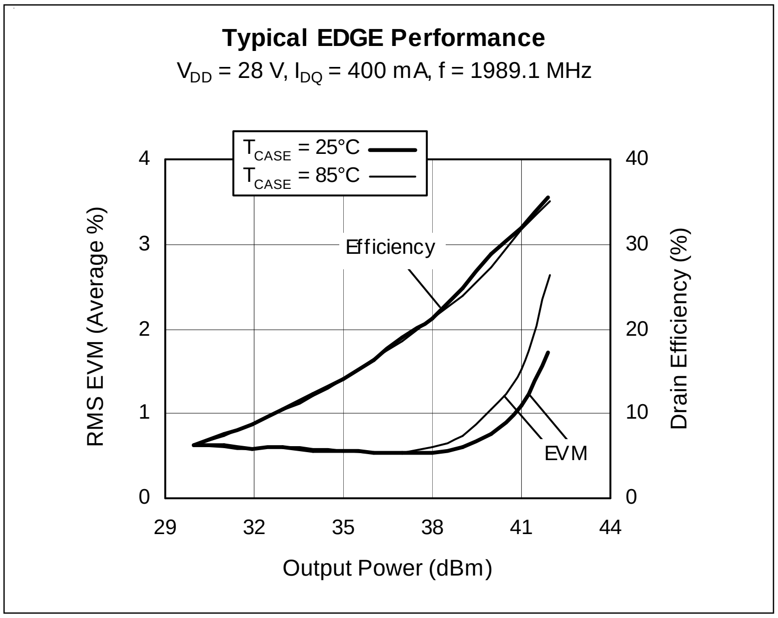
Description

The PTF180301E and PTF180301F are 30-watt, internally-matched *GOLDMOS* FETs intended for GSM EDGE and CDMA applications in the DCS/PCS band. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTF180301E
Package 30265



PTF180301F*
Package 31265


Typical EDGE Performance
V_{DD} = 28 V, I_{DQ} = 400 mA, f = 1989.1 MHz

ESD: Electrostatic discharge sensitive device—observe handling precautions!

Features

- Thermally-enhanced packaging
- Broadband internal matching
- Typical EDGE performance
  - Average output power = 15 W
  - Gain = 16.5 dB
  - Efficiency = 34%
- Typical CW performance
  - Output power at P–1dB = 40 W
  - Gain = 15.5 dB
  - Efficiency = 47%
- Integrated ESD protection: Human Body Model, Class 1 (minimum)
- Excellent thermal stability
- Low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 30 W (CW) output power

RF Characteristics at T_{CASE} = 25°C unless otherwise indicated

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 400 mA, P_{OUT} = 15 W, f = 1989.8 MHz

Characteristic	Symbol	Min	Typ	Max	Units
Error Vector Magnitude	EVM (RMS)	—	1.5	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	–62	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	–73	—	dBc
Gain	G_{ps}	—	16.5	—	dB
Drain Efficiency	η_D	—	34	—	%

**See Infineon distributor for future availability.*

RF Characteristics (cont.)

Two-Tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 400 mA, P_{OUT} = 30 W PEP, f = 1990 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Units
Gain	G_{ps}	14.5	16.5	—	dB
Drain Efficiency	η_D	35	36	—	%
Intermodulation Distortion	IMD	—	–30	–27	dBc

DC Characteristics at T_{CASE} = 25°C unless otherwise indicated

Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.27	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 400 mA	V_{GS}	2.5	3.2	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	100	nA

Maximum Ratings

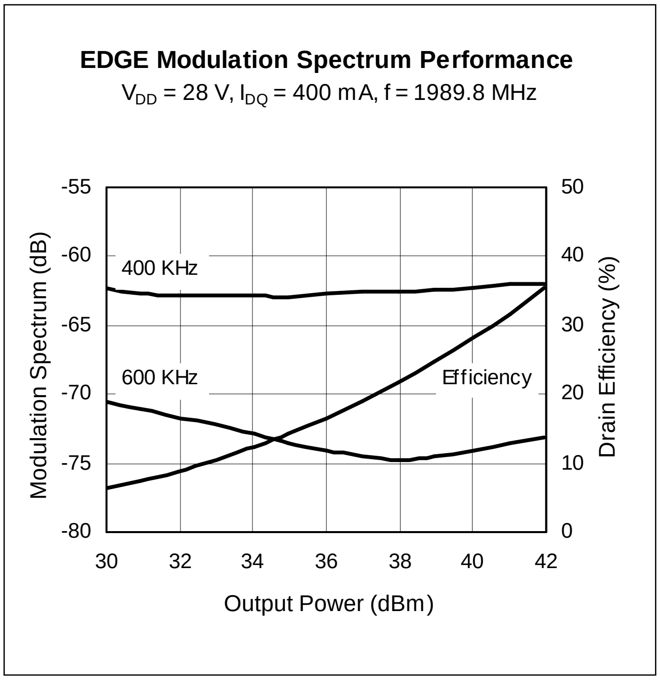
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	145	W
Above 25°C derate by		0.83	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 30 W CW)	$R_{\theta JC}$	1.2	°C/W

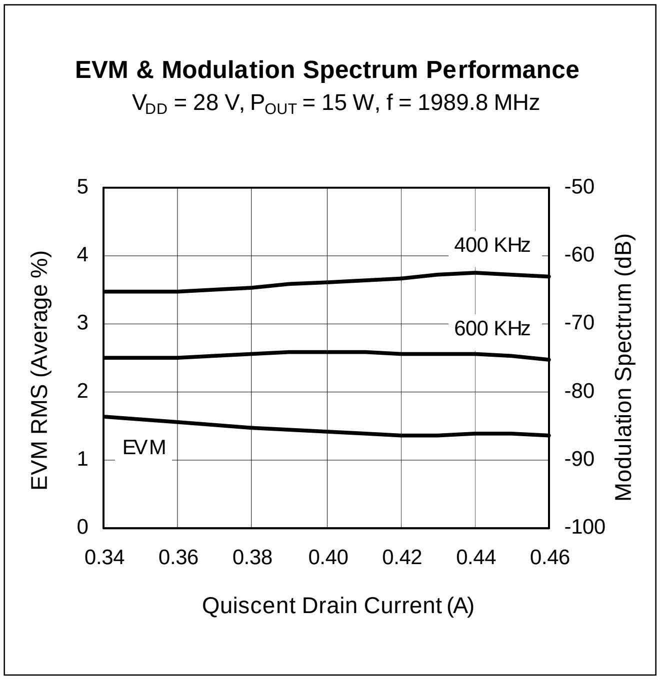
Ordering Information

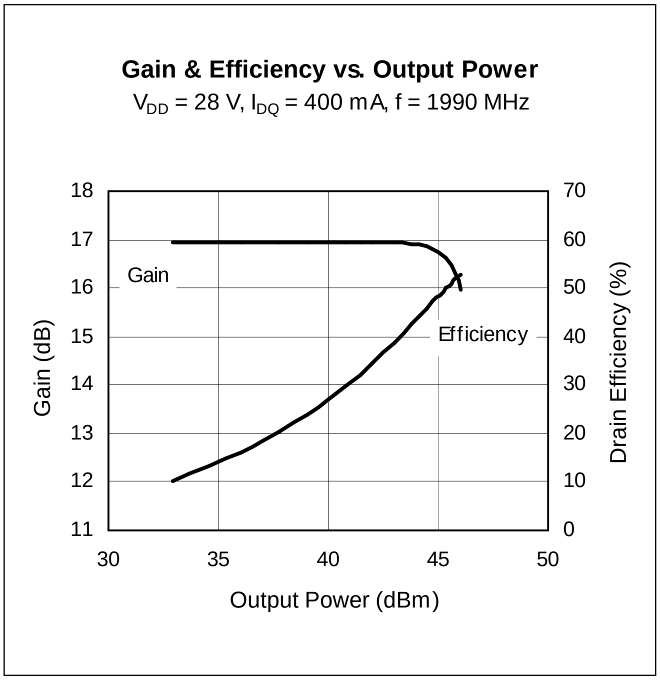
Type	Package Outline	Package Description	Marking
PTF180301E	30265	Thermally-enhanced slotted flange, single-ended	PTF180301E
PTF180301F*	31265	Thermally-enhanced earless flange, single-ended	PTF180301F

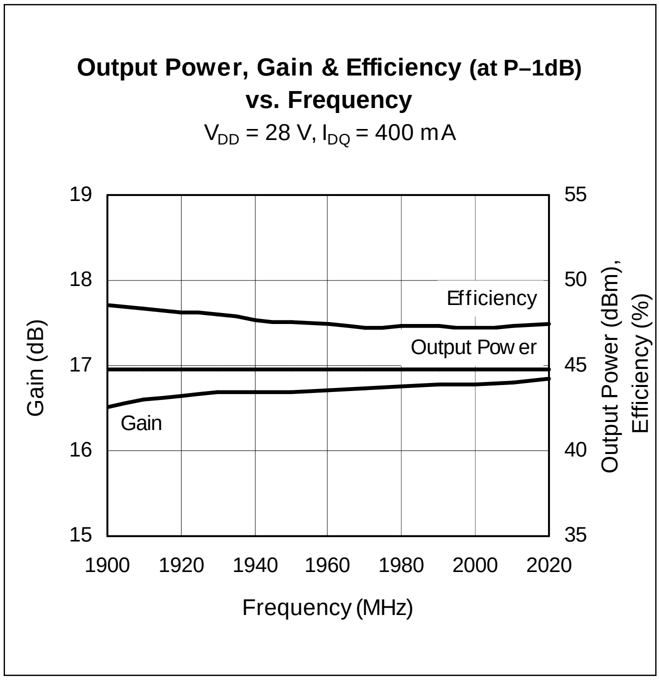
**See Infineon distributor for future availability.*

Typical Performance (data taken in production test fixture)



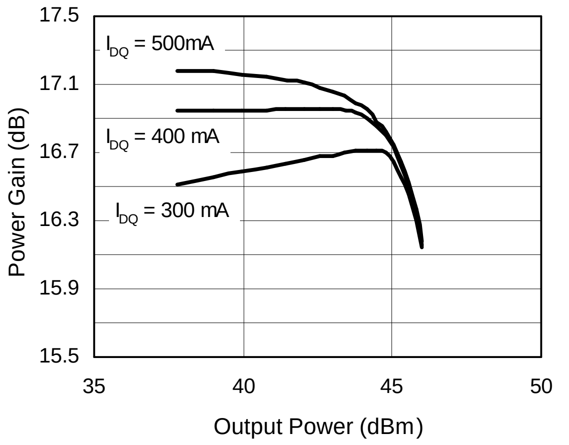






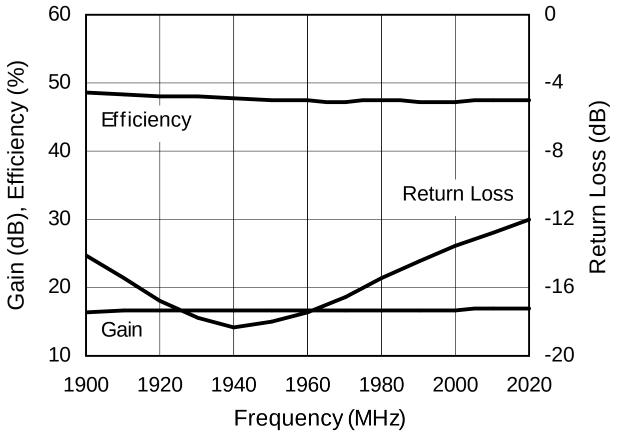
All published data at T_{CASE} = 25°C unless otherwise indicated

Typical Performance (cont.)



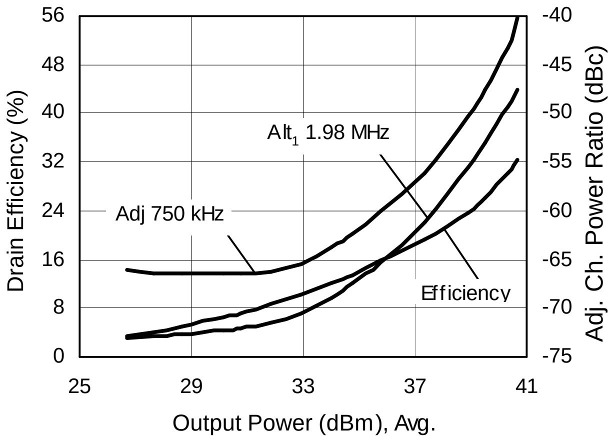
Gain vs. Output Power

V_{DD} = 28 V, f = 1990 MHz



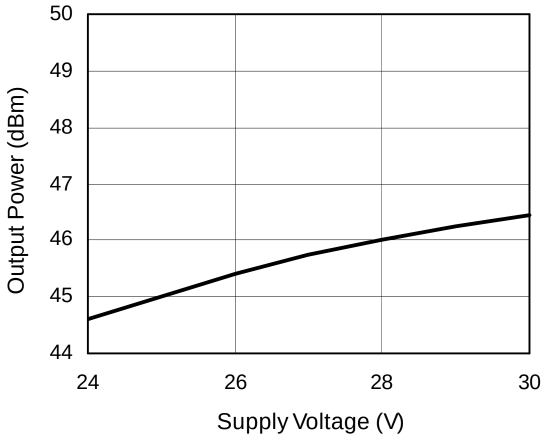
Broadband Performance

V_{DD} = 28 V, I_{DQ} = 400 mA, P_{OUT} = 30 W



IS-95 CDMA Performance

V_{DD} = 28 V, I_{DQ} = 400 mA, f = 1990 MHz

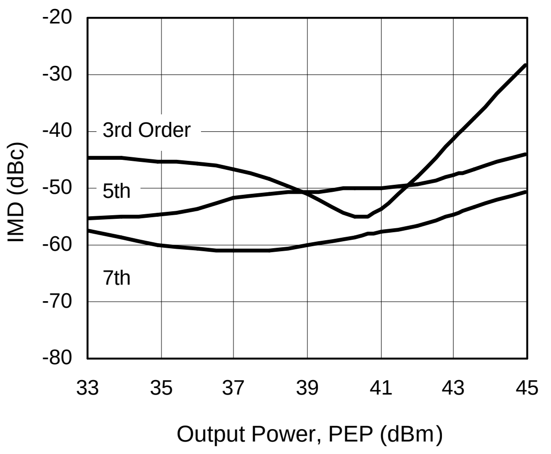


Output Power (P–1dB) vs. Supply Voltage

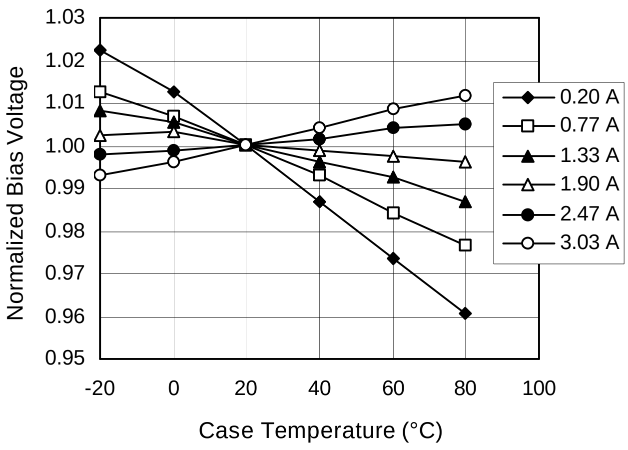
I_{DQ} = 400 mA, f = 1990 MHz

Typical Performance (cont.)

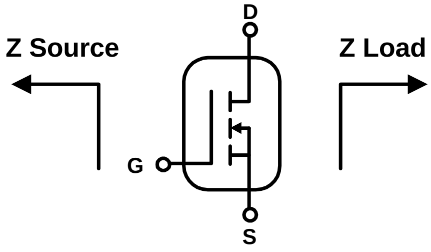
Intermodulation Distortion vs. Output Power
V_{DD} = 28 V, I_{DQ} = 400 mA, f_1 = 1989 MHz, f_2 = 1990 MHz

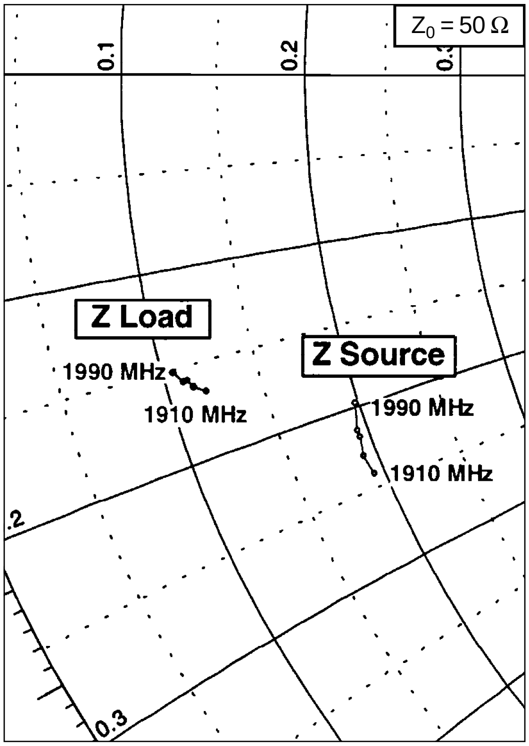


Gate-Source Voltage vs. Case Temperature
Voltage normalized to typical gate voltage.
Series show current.



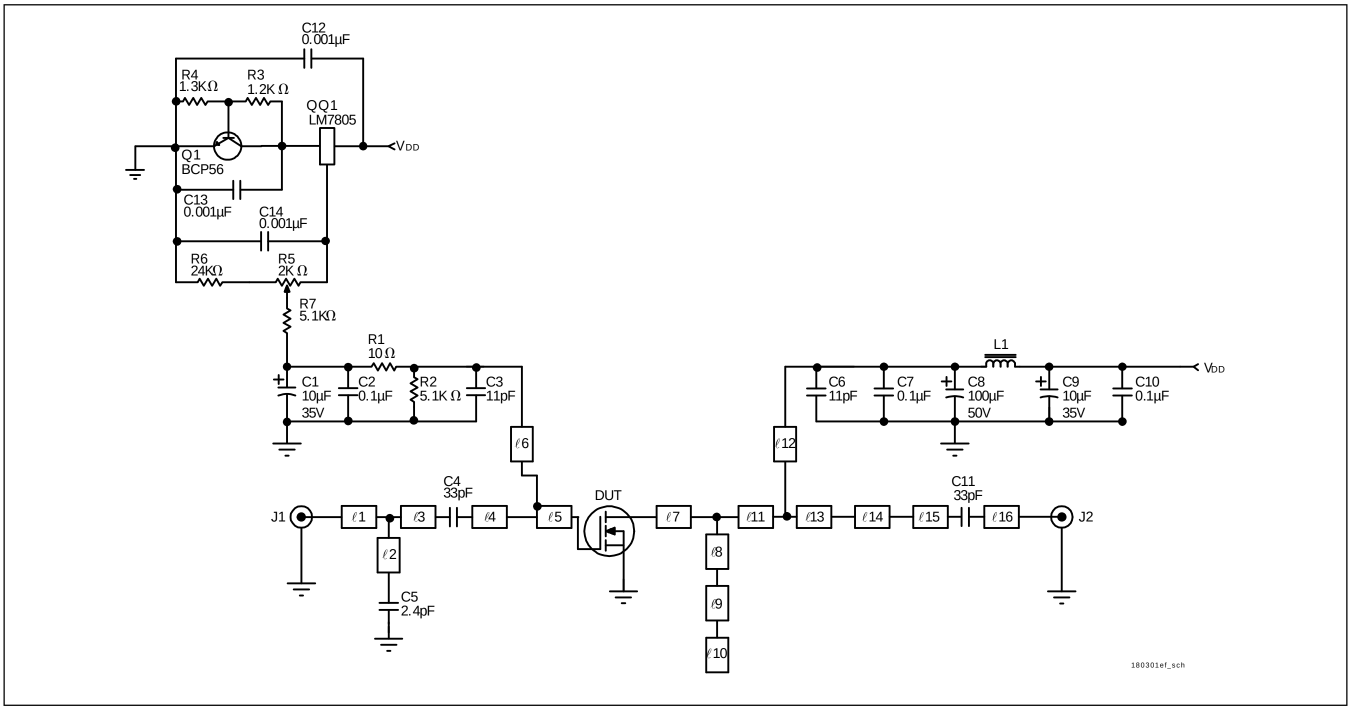
Broadband Circuit Impedance





Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
1910	9.7	–12.1	6.0	–8.3
1930	9.6	–11.5	5.7	–8.1
1950	9.7	–10.9	5.6	–7.9
1960	9.7	–10.7	5.5	–7.9
1990	9.9	–9.9	5.3	–7.6

Reference Circuit



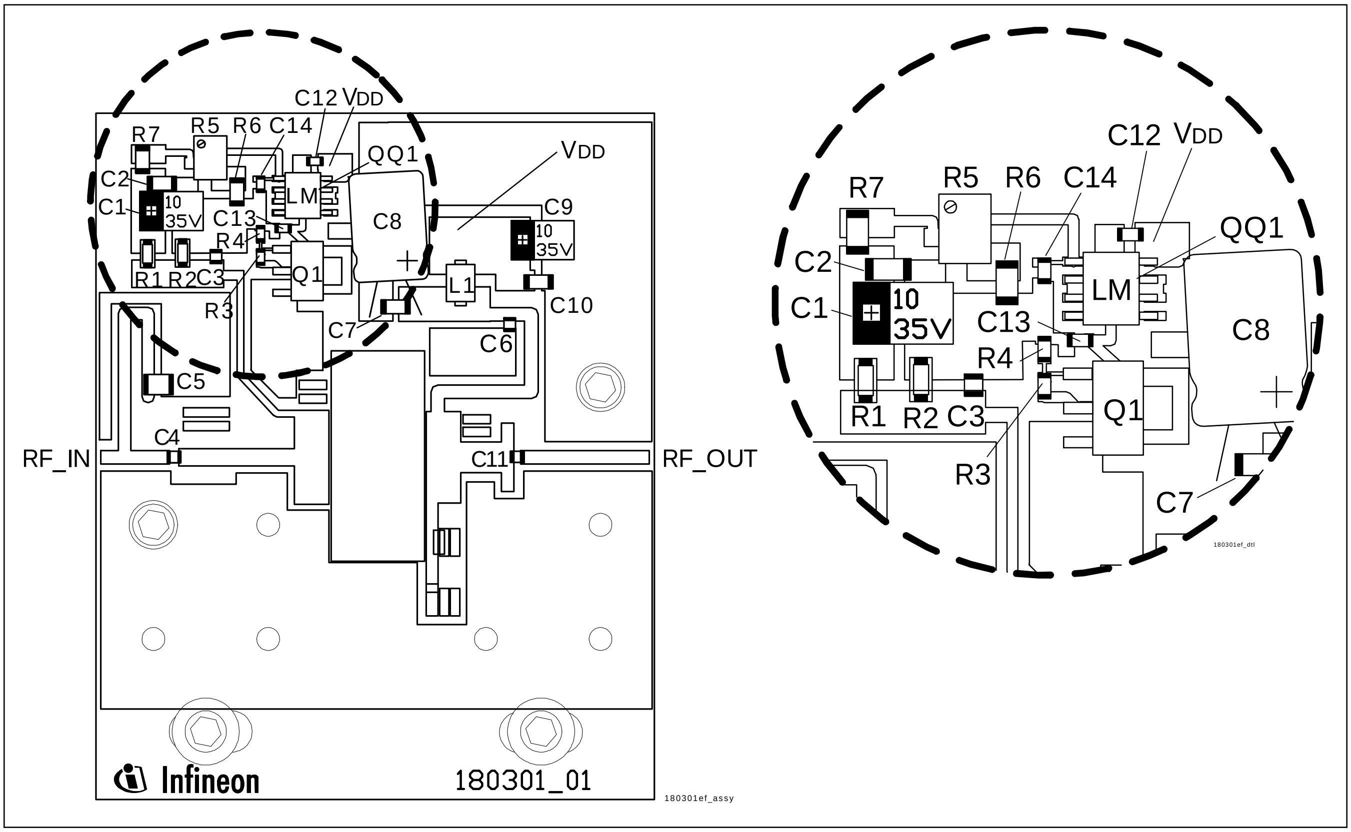
Reference Circit Schematic for f = 1990 MHz

Circuit Assembly Information			
DUT	PTF180301E or PTF180301F	LDMOS Transistor	
PCB	0.76 mm [.030”] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	**Electrical Characteristics at 1960 MHz***	**Dimensions: L x W (mm)**	**Dimensions: L x W (in.)**
ℓ1	0.033 λ, 50.0 Ω	2.67 x 1.42	0.105 x 0.056
ℓ2	0.329 λ, 50.0 Ω	27.05 x 1.32	1.065 x 0.052
ℓ3	0.062 λ, 50.0 Ω	5.08 x 1.42	0.200 x 0.056
ℓ4	0.16 λ, 42.0 Ω	12.70 x 1.83	0.500 x 0.072
ℓ5	0.032 λ, 11.6 Ω	3.61 x 10.03	0.142 x 0.395
ℓ6	0.206 λ, 70.0 Ω	17.40 x 0.71	0.685 x 0.028
ℓ7	0.008 λ, 11.6 Ω	0.64 x 10.03	0.025 x 0.395
ℓ8	0.037 λ, 56.0 Ω	2.92 x 1.17	0.115 x 0.046
ℓ9	0.037 λ, 34.0 Ω	2.92 x 2.46	0.115 x 0.097
ℓ10	0.041 λ, 56.0 Ω	3.30 x 1.17	0.130 x 0.046
ℓ11	0.017 λ, 11.6 Ω	1.27 x 10.03	0.050 x 0.395
ℓ12	0.269 λ, 50.0 Ω	21.97 x 1.45	0.865 x 0.057
ℓ13	0.033 λ, 11.6 Ω	2.49 x 10.03	0.098 x 0.395
ℓ14	0.055 λ, 28.0 Ω	4.32 x 3.30	0.170 x 0.130
ℓ15	0.018 λ, 14.3 Ω	1.32 x 7.87	0.052 x 0.310
ℓ16	0.186 λ, 50.0 Ω	15.24 x 1.42	0.600 x 0.056

**Electrical characteristics are rounded.*

Reference Circuit (cont.)



Reference circuit assembly (not to scale)[1]

Component	Description	Manufacturer	P/N or Comment
C1, C9	Capacitor, 10 µF, 35 V, Tant TE Series	Digi-Key	PCS6106TR-ND, SMD
C2, C7, C10	Capacitor, 0.1 µF	Digi-Key	PCC104BCT
C3, C6	Capacitor, 11 pF	ATC	100A 110
C4, C11	Capacitor, 33 pF	ATC	100A 330
C5	Capacitor, 2.4 pF	ATC	100B 2R4
C8	Capacitor, 100 µF, 50 V	Digi-Key	P5571-ND
C12, C13, C14	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
L1	Ferrite	Philips	BDS4.6/3/8.9-4S2
Q1	Transistor	National Semiconductor	BCP56
QQ1	Voltage regulator	Infineon Technologies	LM7805
R1	Resistor, 10 ohm, 1/4 W	Digi-Key	P10ECT-ND
R2, R7	Resistor, 5.1 k-ohm, 1/4 W	Digi-Key	P5.1KECT-ND
R3	Resistor, 1.2 k-ohm, 1/10 W, 0603	Digi-Key	PI.2KGCT-ND
R4	Resistor, 1.3 k-ohm, 1/10 W, 0603	Digi-Key	PI.3KGCT-ND
R5	Potentiometer 2 k-ohm, 1/4 W	Digi-Key	3224W-202ETR-ND
R6	Resistor, 24 k-ohm, 1/4 W, 1206	Digi-Key	P24KECT-ND

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[1] *Gerber files for this circuit are available on request.*

Package Outline Specifications*

Package 30265

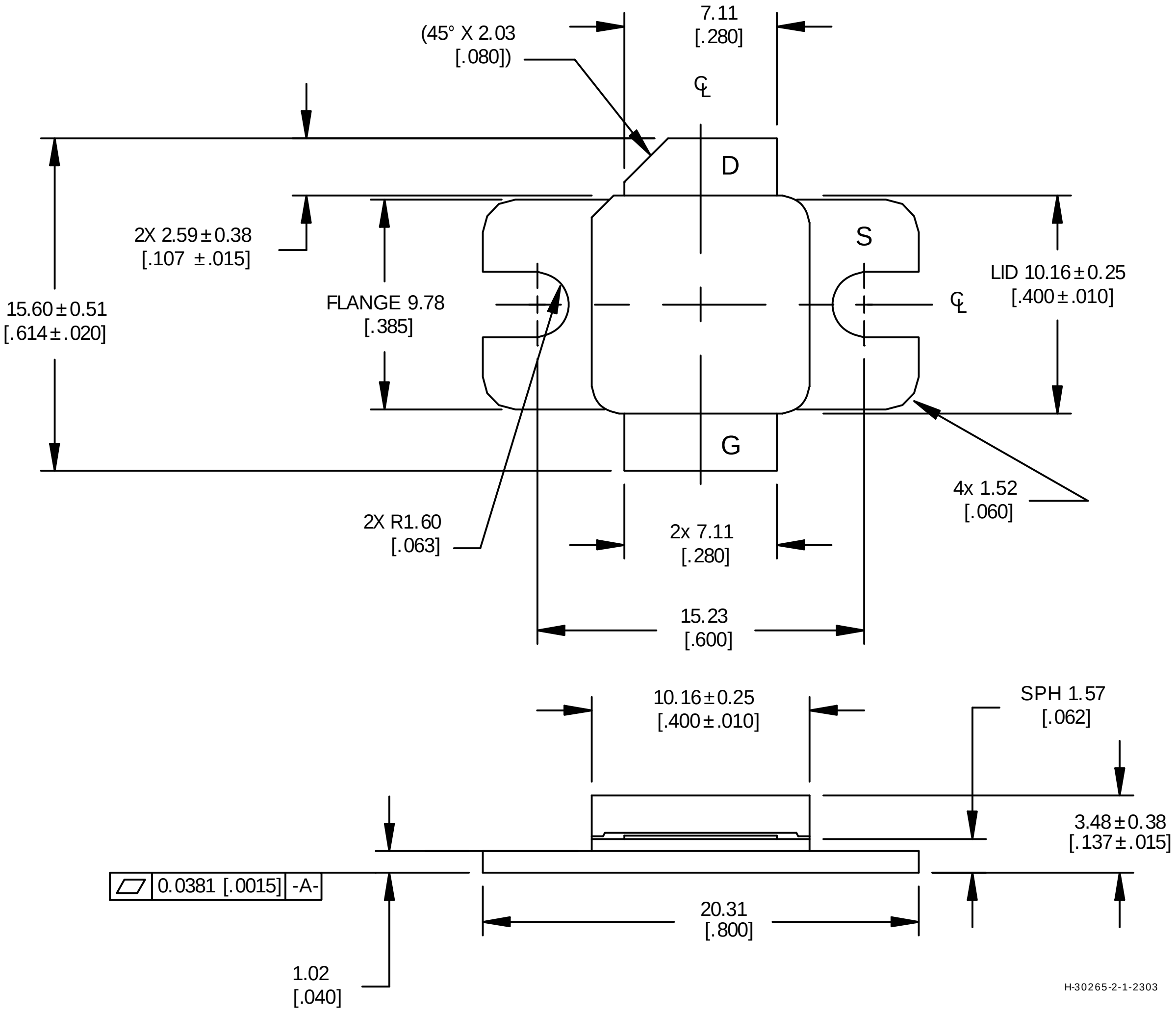

Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.

Find the latest and most complete information about products and packaging at the Infineon Internet page
http://www.infineon.com/rfpower

**Information not yet available for Package 31265. See your Infineon distributor for future availability.*

Revision History: 2004-10-07 Data Sheet

Previous Version: none

Page	Subjects (major changes since last revision)

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