MPEG audio source decoder

SAA2500

FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and interchannel crosstalk
- Demultiplexing of ancillary data in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sampling frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision: 16, 18, 20 or 22 bit
- Low power consumption

GENERAL DESCRIPTION

The SAA2500 performs the audio decoding function as defined for ISO/MPEG Layers I and II.

FUNCTIONAL DESCRIPTION

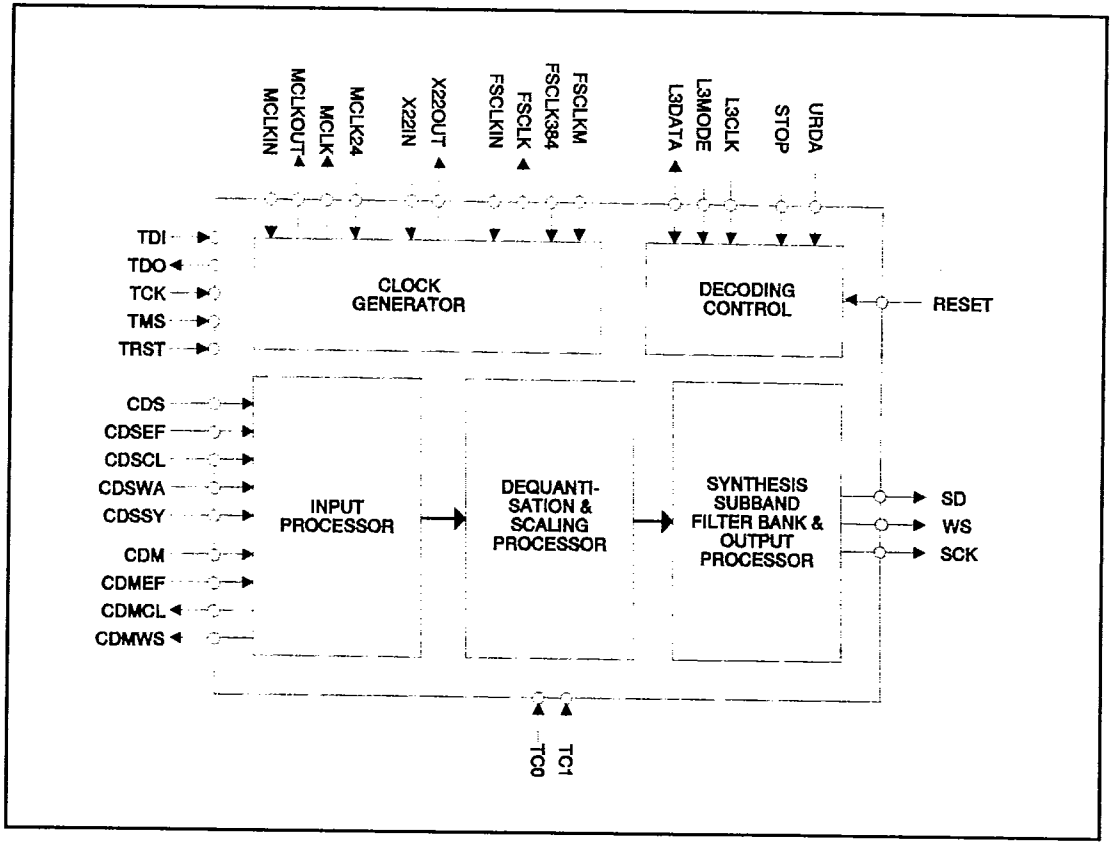
Coding System

The perceptual audio encoding/decoding scheme defined within the ISO/IEC 11172-3 MPEG Standard allows for a high reduction in the amount of data needed for digital audio while maintaining a high perceived sound quality. The coding is based upon a psycho-acoustic model of the human auditory system. The coding scheme exploits the fact that the human ear does not perceive weak spectral components that are in the proximity (both in time and frequency) of loud components. This phenomenon is called masking.

For Layers I and II of ISO/MPEG the broadband audio signal spectrum is split into 32 sub-bands of equal bandwidth. For each sub-band signal a masking threshold is calculated. The sub-band samples are then re-quantised to such an accuracy that the spectral distribution of the re-quantisation noise does not exceed the masking threshold. It is this reduction of representation accuracy which yields the data reduction. The re-quantised sub-band signals are multiplexed, together with ancillary information regarding the actual re-quantisation, into a MPEG audio bitstream.

During decoding, the SAA2500 demultiplexes the MPEG audio bitstream, and with knowledge of the ancillary information, reconstructs and combines the sub-band signals into a broadband audio output signal.

BLOCK DIAGRAM



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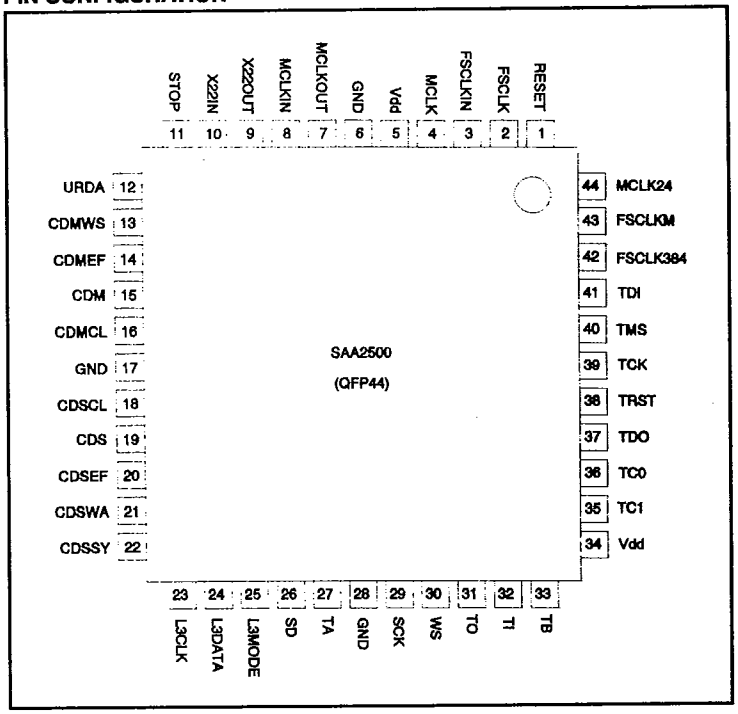
PIN CONFIGURATION



PINNING INFORMATION

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	Master reset	I
FSCLK	2	Sampling rate clock; buffered signal	O
FSCLKIN	3	Sampling rate clock input	I
MCLK	4	Master clock; buffered signal	O
V_{DD}	5	Positive power supply	
GND	6	Ground	
MCLKOUT	7	Master clock oscillator output	O
MCLKIN	8	Master clock oscillator input or signal input	I
X22OUT	9	22.579MHz clock oscillator output	O
X22IN	10	22.579MHz clock oscillator input or signal input	I
STOP	11	Stop decoding	I
URDA	12	Unreliable input data; interrupt decoding	I
CDMWS	13	Coded data (master input) word select	O
CDMEF	14	Coded data (master input) error flag	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	Coded data (master input) bit clock	O
GND	17	Ground	

PINNING INFORMATION (Continued)

SYMBOL	PIN	DESCRIPTION	TYPE
CDSCL	18	Coded data (slave input) bit clock	I
CDS	19	ISO/MPEG coded data (slave input)	I
CDSEF	20	Coded data (slave input) error flag	I
CDSWA	21	Coded data (slave input) window signal	I
CDSSY	22	Coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock	I
L3DATA	24	L3 interface serial data	I/O
L3MODE	25	L3 interface address/data select	I
SD	26	Baseband audio I^2S data	O
TA	27	Do not connect; reserved	O
GND	28	Ground	
SCK	29	Baseband audio data I^2S clock	O
WS	30	Baseband audio data I^2S word select	O
TO	31	Connect to TI	O
TI	32	Connect to TO	I
TB	33	Do not connect; reserved	O
V_{DD}	34	Positive power supply	
TC1	35	Do not connect; factory test control 1, with integrated pulldown resistor	I
TC0	36	Do not connect; factory test control 0, with integrated pulldown resistor	I
TDO	37	Boundary scan test data output	O
TRST	38	Boundary scan test reset; this pin should be grounded for normal operation	I
TCK	39	Boundary scan test clock	I
TMS	40	Boundary scan test mode select	I
TDI	41	Boundary scan test data input	I
FSCLK384	42	Sampling rate clock frequency indication	I
FSCLKM	43	Sampling rate clock source selection for the master input	I
MCLK24	44	Master clock frequency indication	I

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage		−0.5	6.5	V
V_I	Input voltage	Note 1	−0.5	V_{DD} + 0.5	V
I_{DD}	Supply current		—	100	mA
I_I	Input current		—	10	mA
I_O	Output current	2mA outputs	—	10	mA
I_O	Output current	4mA outputs	—	20	mA
P_{TOT}	Total power dissipation	V_{DD} = 5V ± 5%	—	240	mW
T_{STG}	Storage temperature range		−65	150	°C
T_{AMB}	Operating ambient temperature range		−40	85	°C
V_{ES1}	Electrostatic handling	Note 2	−2000	2000	V
V_{ES2}	Electrostatic handling	Note 3	200	200	V

NOTES:
1. Input voltage should not exceed 6.5V unless otherwise specified.
2. Equivalent to discharging a 100pF capacitor through a 1.5kΩ series resistor.
3. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor.

DC CHARACTERISTICS

T_{AMB} = −40 to +85°C; V_{DD} = 5V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	Quiescent supply current	Note 1	—	—	100	µA
Inputs						
V_{IH}	Input voltage HIGH (CMOS)		0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input voltage LOW (CMOS)		0	—	0.3V_{DD}	V
V_{IH}	Input voltage HIGH (TTL)		2.0	—	V_{DD}	V
V_{IL}	Input voltage LOW (TTL)		0	—	0.8	V
V_{TLH}	Positive going threshold (CMOS Schmitt trigger)		—	—	0.8V_{DD}	V
V_{THL}	Negative going threshold (CMOS Schmitt trigger)		0.2V_{DD}	—	—	V
V_{HYS}	Hystersis voltage (CMOS Schmitt trigger)		—	0.3V_{DD}	—	V
$\|I_I\|$	Input current		—	—	10	µA
R_{PULL}	Pull-up resistor		15	—	160	kΩ
Outputs						
V_{OL}	Output voltage LOW	Note 2	—	—	0.5	V
V_{OH}	Output voltage HIGH	Note 2	V_{DD} − 0.5	—	—	V
$\|I_{OZ}\|$	3-State off leakage current		—	—	10	µA

NOTES:
1. Inputs TC1 and TC0 connected to V_{SS}; inputs TRST, TMS and TDI connected to V_{DD}.
2. Output current I_O = 2mA for L3DATA (Pin 24); I_O = 4mA for all other outputs.

AC CHARACTERISTICS

T_{AMB} = −40 to +85°C; V_{DD} = 5V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clocks						
C_I	Input capacitance		—	—	10	pF
MCLKIN						
f	Clock frequency (MCLK24 = 1)		—	24.576	27	MHz
f	Clock frequency (MCLK24 = 0)		—	12.288	13.5	MHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns
X22IN						
f	Clock frequency		—	—	22.579	MHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns
FSCLKIN						
f	Clock frequency (FSCLK384 = 1)		—	—	18.432	MHz
f	Clock frequency (FSCLK384 = 0)		—	—	12.288	MHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns
CDSCL						
f	Clock frequency		—	—	448	MHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns
L3CLK						
f	Clock frequency		—	—	TBF	kHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns
TCK						
f	Clock frequency		—	—	TBF	kHz
t_R	Rise time		—	—	4	ns
t_F	Fall time		—	—	4	ns
t_H	HIGH time		TBF	—	—	ns
t_L	LOW time		TBF	—	—	ns