82344

ISA BUS CONTROLLER

DESCRIPTION

The 82344 ISA Bus Controller replaces several of the LSI controllers used in PC/AT-type designs with one single 160-pin quad flatpack. The Bus Controller provides the functions of DMA, page address register, timer, interrupt control, Port B logic, slot bus refresh address generation, and real time clock.

The Bus Controller directly drives the refresh addresses onto the AT slot address bus during refresh cycles in response to a refresh cycle command from the System Controller. To avoid problems with sensitive slot bus add-in cards, the Bus Controller features "bus quiet" mode. When no valid slot bus accesses are occurring, none of the slot bus data, address or control lines are driven.

Built-in sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems. When activated by the CPU via I/O write to an internal indexed configuration register, the DMA subsystem and the AT slot bus subsystems are shut off. The SYSCLK can be individually controlled. The interrupt controllers and the timers continue to operate. If an interrupt occurs due to an external source or one of the timers, the Bus Controller "wakes up" and in turn wakes the System Controller.

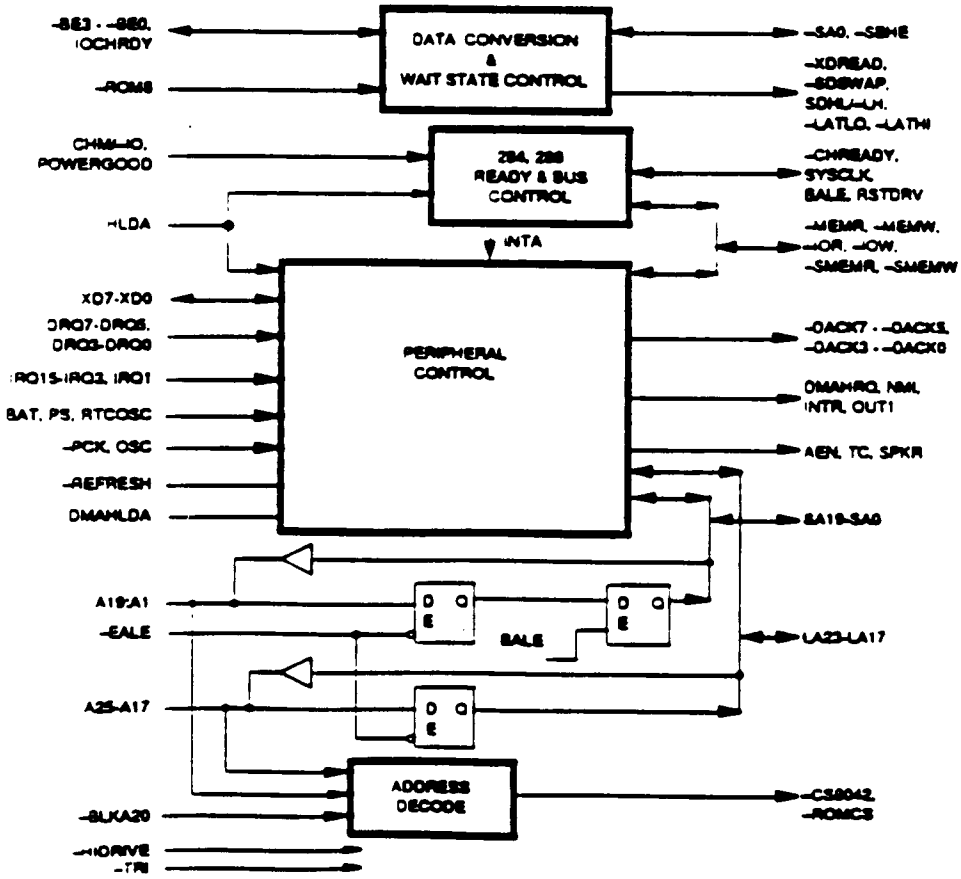
The upgraded DMA channels provide a superset of AT functionality by allowing DMA to the entire 64 Mbyte memory range of the 82340DX chip set. Additional functionality is provided via DMA wait state, clock, and –MEMR timing programmability.

A –HIDRIVE pin can be externally strapped to provide for 12 or 24 mA drive to the slot bus. If left open, an internal pull-up causes the drive current to default to 24 mA. This allows systems designed with one to four slots to select a lower drive level and reduce bus ringing. A –ROM8 pin selects the bus and bus size to use for BIOS ROM accesses. The choices are 8- or 16-bit wide ROMs.

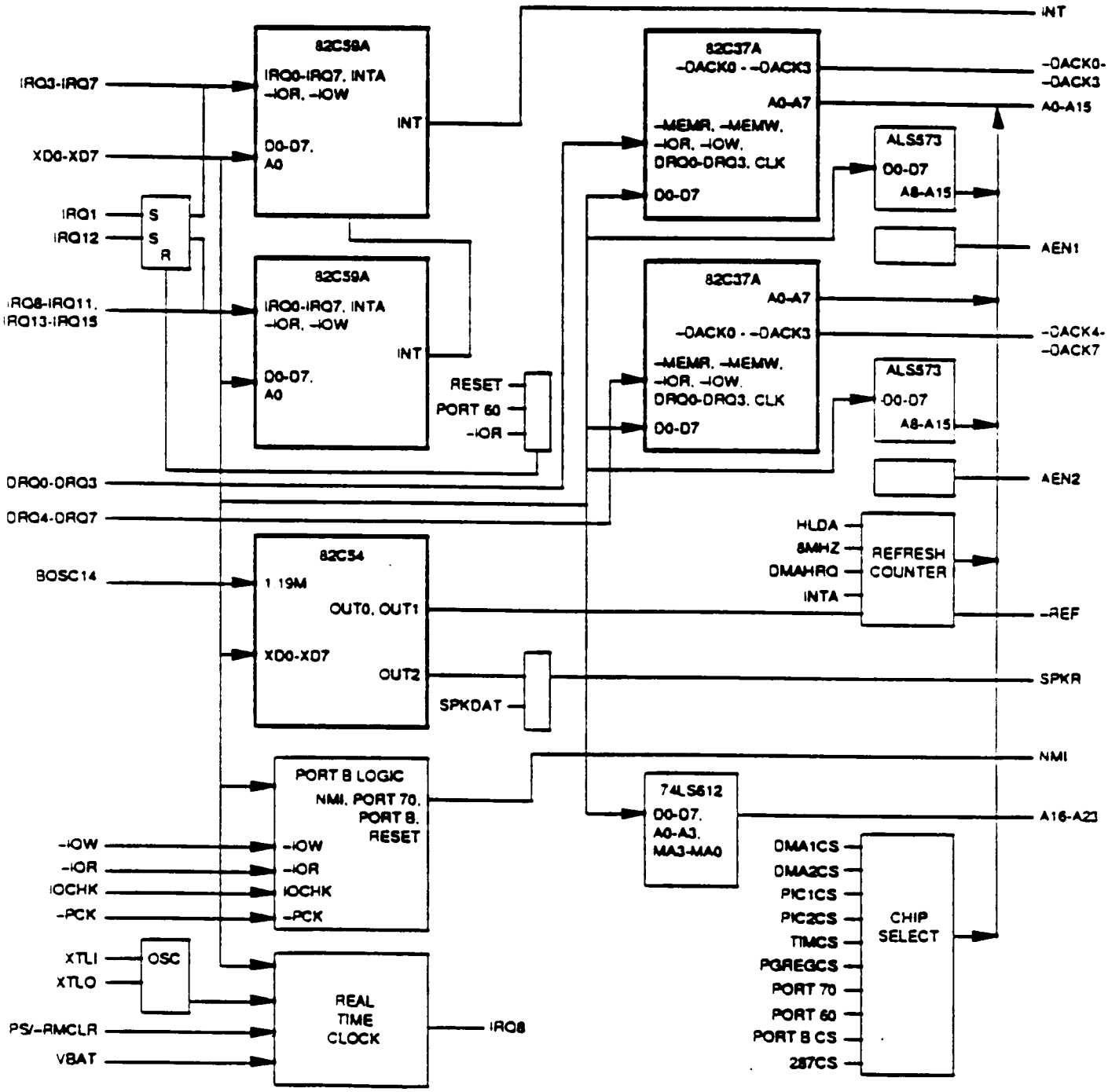
A three-state test control pin has been added for board level testability.

The Bus Controller features several megacells, implemented in 1.5-micron CMOS technology, and is intended to work in 286-, 386SX-, or 386DX-based systems with CPU clock speeds up to 33 MHz and bus speeds up to 16 MHz.

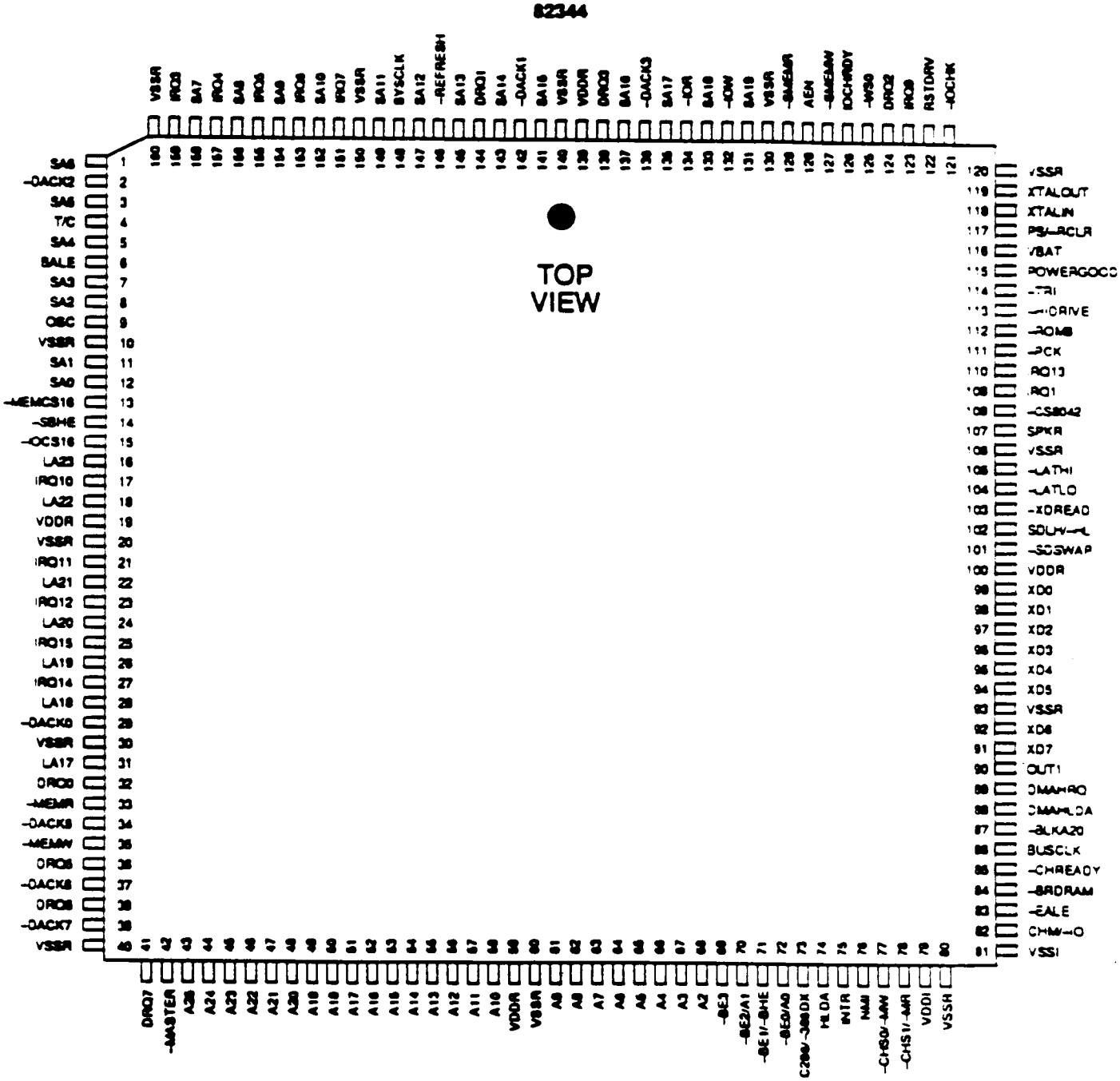
BLOCK DIAGRAM



PERIPHERAL CONTROL BLOCK DIAGRAM



PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE			
A25, A24	43, 44	O-TS	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are high impedance at all other times. A25 and A24 are driven from the alternate 612 registers during DMA and refresh cycles and are driven low during master cycles.
A23-A2	45-58, 61-68	IO-TTL	Address bus - These pins are outputs during DMA, master, or standard refresh modes. They are inputs at all other times. As inputs, they are passed to the SA and LA buses and A15-A2 are used to address I/O registers internal to the bus control chip. As outputs, they are driven from different sources depending on which mode the Bus Controller is in. While in refresh mode, these pins are driven from the 612 and refresh address counter. While in DMA mode, they are driven from the 612 and DMA controller subsection. If the Bus Controller is in master mode, the pins A23-A17 are driven from the inputs LA23-LA17 and the pins A16-A2 are driven from the inputs SA16-SA2.
–BE3	69	IO-TTL	Byte Enable 3, active low - This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and –SBHE. As an output in 386DX mode SA1, SA0, and –SBHE are used to determine the value of –BE3. This pin should be left unconnected when using this part in 286 mode. The pin has an internal pull-up.
–BE2/A1	70	IO-TTL	Byte Enable 2, active low, or A1 - This pin has a dual function depending on the state of the C286/–386DX input. If C286/–386DX is high (286 mode), then the pin is treated as address bit 1. If C286/–386DX is low (386DX mode), the pin is treated as –BE2. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and –SBHE. As an output in 386DX mode, SA1, SA0, and –SBHE are used to determine the value of –BE2. When in 286 mode, it is interpreted as address A1 and passed to SA1. As an output in 286 mode it is driven from the SA1 input.
–BE1/–BHE	71	IO-TTL	Byte Enable 1 or Byte High Enable, active low - This pin has a dual function depending on the state of the C286/–386DX input. If C286/–386DX is high (286 mode), then the pin is treated as –BHE. If C286/–386 is low (386 mode), the pin is treated as –BE1. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386 mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and –SBHE. As an output in 386 mode, SA1, SA0, and –SBHE are used to determine the value of –BE1. When in 286 mode, it is interpreted as –BHE and passed to –SBHE. As an output in 286 mode, it is driven from the –SBHE input.
–BE0/A0	72	IO-TTL	Byte Enable 0, active low, or A0 - This pin has a dual function depending on the state of the C286/–386DX input. If C286/–386DX is high (286 mode), then the pin is treated as address bit 0. If C286/–386DX is low (386 mode), the pin is treated as –BE0. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386 mode, it is decoded along with the other Byte Enable signals ' generate SA1, SA0, and –SBHE. As an output in 386 mode, SA1, SA0, and –SBHE are used to determine the value of –BE0. When in 286 mode, it is interpreted as A0 and passed to SA0. As an output in 286 mode, it is driven from the SA0 input.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
C286/–386DX	73	I-TPU	CPU is 286 or 386DX - This pin defines the type of address bus to which the bus controller chip is interfaced. If the pin is tied high, the address bus is assumed to be emulating 286 signals. In this mode, A25, A24, and –BE3 would be left unconnected. The pins –BE2/A1, –BE1/–BHE and –BE0/A0 would take on the 286 functions. If the pin is tied low, A25, A24 can be used to generate up to 64 Mbyte addressing for DMA, and the byte enable pins will take on the normal 386DX addressing functions. This pin has an internal pull-up to cause the chip to default to 286 mode if left unconnected. This pin is a hard wiring option and must not be changed dynamically during operation. When strapped for 286 mode, the Bus Controller is assumed to be interfaced to the 82343 System Controller which in turn may be strapped for 286 or 386SX operation. The 82344 is strapped for 286 operation when used with the 82343 strapped for 386SX operation.
HLDA	74	I-TTL	Hold Acknowledge - This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and command pins. When HLDA is low, the Bus Controller is defined as being in the CPU mode. In the CPU mode, the local address bus (A bus) pins are inputs. The system address bus (SA and LA) pins along with the command pins (–MEMR, –MEMW, –IOR and –IOW) are outputs. When HLDA is high, the Bus Controller can be in DMA, refresh, or master modes. In both DMA and refresh modes, the commands and all address buses (A, SA and LA) are outputs. In master mode, the commands and system address bus (SA and LA) pins are inputs and the local address bus (A bus) pins are outputs. The SA bus is passed directly to the A bus except bits 17, 18, and 19 are ignored. LA23-LA17 is passed directly to A23-A17.
INTR	75	O	Interrupt Request - INTR is used to interrupt the CPU and is generated by the 8259 megacells any time a valid interrupt request input is received.
NMI	76	O	Non-Maskable Interrupt - This output is used to drive the NMI input to the CPU. This signal is asserted by either a parity error (indicated by –PCK being asserted after the ENPARCK bit in Port B has been asserted), or an I/O channel error (indicated by –IOCHCK being asserted after the ENIOCK bit in Port B has been asserted). The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.
SYSTEM CONTROLLER INTERFACE			
–CHS0/–MW	77	IO-TTL	Channel Status 0 or active low Memory Write - This input is used along with –CHS1 and CHM/–IO to determine what type of bus cycle the Bus Controller is to perform. This input has the same meaning and timing requirements as the S0 signal for a 286 microprocessor. –CHS0 going active indicates a write cycle unless –CHS1 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a –MEMW signal for DMA or bus master access to system memory.
–CHS1/–MR	78	IO-TTL	Channel Status 1 or active low Memory Read - This input is used along with –CHS0 and CHM/–IO to determine the bus cycle type. This input has the same meaning and timing requirements as the S1 signal for a 286 microprocessor. –CHS1 going active indicates a read cycle unless –CHS0 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
			System Controller. It is then a –MEMR signal for DMA or bus master access to system memory.
CHM/–IO	82	I-TTL	Channel Memory or active low I/O select - This input is used along with –CHS0 and –CHS1 to determine the bus cycle type. This input has the same meaning and timing requirements as the M/–IO signal for a 286 microprocessor. CHM/–IO is sampled anytime –CHS0 or –CHS1 is active. If sampled high, it indicates a memory read or write cycle. If sampled low, an I/O read or write cycle should be executed. This input is synchronized to the BUSCLK input.
–EALE	83	I-TTL	Early Address Latch Enable, active low - This input is used to latch the A25-A2 and Byte Enable signals. The latches are open when –EALE is low and hold their value when –EALE is high. The latched addresses are fed directly to the LA23-LA17 bus to provide more address setup time on the bus before a command goes active. The lower latched addresses are latched again with an internal ALE signal as soon as –CHS0 or –CHS1 is sampled active and fed to the SA19-SA0 and –SBHE outputs. In a 386DX system, this input is connected directly to the –ADS output from the CPU. In a 286 system, this input is connected to the –EALE output from the 82343 System Controller.
–BRDRAM	84	I-TTL	On-board DRAM, active low - An input from the System Controller indicating that the on-board DRAM is being addressed.
–CHREADY	85	O	Channel Ready, active low - This output is maintained in the active state when no bus accesses are active. This indicates that the Bus Controller is ready to accept a new command. During normal bus accesses, –CHREADY is negated as soon as a valid bus requested is sampled on the –CHS0 and –CHS1 inputs. It is asserted again to indicate that the Bus Controller is ready to complete the current cycle. The bus command signals are then terminated on the next falling edge of the BUSCLK input.
BUSCLK	86	I-CMOS	Bus Clock - This is the main clock input for the Bus Controller. It runs at twice the frequency desired for the SYSCLK output. All inputs are synchronous with the falling edge of this input.
–BLKA20	87	I-TTL	Block A20, active low - This input is used while CPUHLDA is low to force the LA20 and SA20 outputs low anytime it is active. When –BLKA20 is negated LA20 and SA20 are generated from A20.
DMAHRQ	89	O	Hold Request - This output is generated by the DMA controller any time a valid DMA request is received. It is connected to the DMAHRQ pin on the System Controller.
DMAHLDA	88	I-TTL	DMA Hold Acknowledge - An input from the System Controller which indicates that the current hold acknowledge state is for the DMA controller or other bus master.
OUT1	90	O	Output 1 - Indicates a refresh request to the System Controller. This is the 15 µsec output of timer channel 1.
ROM INTERFACE			
–ROM8	112	I-TPU	8/16 bit ROM select - This input indicates the width of the ROM BIOS. If –ROM8 is low, the Bus Controller chip generates 8- to 16-bit conversions for ROM accesses. Data buffer controls are generated assuming the ROM is on the MD bus. If –ROM8 is high, data buffer controls are generated assuming 16-bit wide ROMs are on the MD bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE			
–IOR	134	IO-TTL	I/O Read, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –IOR is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–IOW	132	IO-TTL	I/O Write, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –IOW is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–MEMR	33	IO-TTL	Memory Read, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This signal does not pulse low for DMA addresses above 16 Mbytes. DMA above 16 Mbytes is only performed to the system board, never to the slot bus. This pin requires an external 10K ohm pull-up resistor.
–MEMW	35	IO-TTL	Memory Write, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.
–SMEMR	129	IO-TTL	Memory Read, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. –SMEMR is active on memory read cycles to addresses below 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.
–SMEMW	127	IO-TTL	Memory Write, active low - This signal is an input when CPUHLDA is high and –MASTER is low. It is an output at all other times. When CPUHLDA is low, –MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and –MASTER is high, it is driven by the 8237 DMA controller megacells. –SMEMW is active on memory write cycles to addresses below 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.
LA23-LA17	16, 18, 22, 24, 26, 28 31	IO-TTL	Latchable Address bus - This bus is an input when CPUHLDA is high and –MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the LA bus is driven by the latched values from the A bus. When CPUHLDA is high and –MASTER is high, the SA bus is driven by the 612 memory mapper for DMA cycles and normal refresh. The LA bus is latched internally with the –EALE input.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SA19-SA0	131, 133, 135 137, 141, 143, 145, 147, 149 152, 154, 156, 158, 1, 3, 5, 7, 8, 11, 12	IO-TTL	System Address bus - This bus is an input when CPUHLDA is high and –MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and –MASTER is high, the SA bus is driven by the 8237 DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the –CHS0 and –CHS1 inputs. They are latched with an internally generated ALE signal.
–SBHE	14	IO-TTL	System Byte High Enable, active low - This pin is controlled the same way as the SA bus. It is generated from a decode of the –BE inputs in CPU mode. It is forced low for 16-bit DMA cycles and forced to the opposite value of SA0 for 8-bit DMA cycles.
–REFRESH	146	IT-OD	Refresh signal, active low - This I/O signal is pulled low whenever a de-coupled refresh command is received from the System Controller. It is used as an input to sense refresh requests from external sources such as the System Controller for coupled refresh cycles or bus masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. –REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
SYSCLK	148	O	System Clock - This output is half the frequency of the BUSCLK input. The bus control outputs BALE and the –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
OSC	9	I-TTL	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
RSTDRV	122	O	Reset Drive, active high - This output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSCLK input.
BALE	6	O	Buffered Address Latch Enable, active high - A pulse which is generated at the beginning of any bus cycle initiated from the CPU. BALE is forced high anytime CPUHLDA is high.
AEN	128	O	Address Enable - This output goes high anytime the inputs CPUHLDA and –MASTER are both high.
T/C	4	O	Terminal Count - This output indicates that one of the DMA channels terminal count has been reached. This signal directly drives the system bus.
–DACK7- –DACK5, –DACK3 - –DACK0	39, 37, 34, 136, 2, 142, 29	O	DMA Acknowledge, active low - These outputs are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is set active low on reset. Since the 8237 megacells are internally cascaded together, the polarity of the –DACK signals must not be changed. This signal directly drives the system bus.
DRQ7-DRQ5 DRQ3-DRQ0	41, 38, 36, 138, 124, 144, 32	I-TSPU	DMA Request - These asynchronous inputs are used by an external device to indicate when they need service from the internal DMA controllers. DRQ0-DRQ3 are used for transfers from 8-bit I/O adapters to/from system memory. DRQ5-DRQ7 are used for transfers from 16-bit I/O adapters to/from system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-ups.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
IRQ15-IRQ9 IRQ7-IRQ3, IRQ1	25, 27, 110, 23, 21, 17, 123, 151, 153, 155, 157, 159, 109	I-TSPU	**Interrupt Request** - These are the asynchronous interrupt request inputs for the 8259 megacells. IRQ0, IRQ2, and IRQ8 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 8254 counter 0. IRQ2 is used to cascade the two 8259 megacells together. IRQ8 is output from the RTC megacell to the 8259 megacell. All IRQ input pins are active high and have internal pull-ups .
–MASTER	42	I-TTL	**Master, active low** - This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external bus master has control of the bus.
–MEMCS16	13	I-TTL	**Memory Chip Select 16 bit** - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the Sytem Controller requests a 16-bit memory cycle and –MEMCS16 is sampled high.
–IOCS16	15	I-TTL	**I/O Chip Select 16 bit** - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and –IOCS16 is sampled high.
–IOCHK	121	I-TTL	**I/O Channel Check, active low** - This input is used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHK assertion by a peripheral device generates an NMI to the processor. The state of the –IOCHK signal is read as data bit D6 of the Port B register
IOCHRDY	126	I-TTL	**I/O Channel Ready** - This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data, or strobe-in write data in this amount of time must use –IOCHRDY to extend these cycles.
–WS0	125	I-TTL	**Wait State 0, active low** - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWERGOOD	115	I-TSPU	**System power on reset** - This input signals that power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
PERIPHERAL INTERFACE			
–CS8042	108	O	**Chip Select for 8042, active low** - This output is active any time an SA address is decoded at 60h or 64h. It is intended to be connected to the chip select of the keyboard controller.
XTALIN	118	I-CMOS	**Crystal Input** - An internal oscillator input for the real time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.
XTALOUT	119	O	**Crystal Output** - An internal oscillator output for the real time clock crystal. See XTALIN. This pin is a no connect when an external oscillator is used.
PS/ –RCLR/IRQ8	117	I-TSPU	**Power Sense, active high** - Used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the RTC may not be valid. This pin is connected to an external RC network. When bit 6 of configuration register BUSCTL = 1, this pin becomes IRQ8 in from an external real time clock.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
VBAT	116	I	Voltage Battery - Connected to the RTC hold-up battery between 3.5 and 5 volts.
SPKR	107	O	Speaker - This output drives an externally buffered speaker. This signal is created by gating the output of timer 2. Bit 1 of Port B, 61H, is used to enable the speaker output, and bit 0 is used to gate the output of the timer.
DATA BUFFER INTERFACE			
XD7-XD0	91, 92, 94-99	IO-TTL	Peripheral data bus - The bidirectional X data bus outputs data on an INTA cycle or I/O read cycle to any valid address within the Bus Controller. It is configured as an input at all other times.
-SDSWAP	101	O	System Data Swap, active low during some 8-bit accesses - It indicates that the data on the SD bus must be swapped from low byte to high byte or vice versa depending on the state of the SDLH/-HL pin. -SDSWAP is active for 8-bit DMA cycles when an odd address access occurs for data more than one byte wide. For non-DMA accesses, -SDSWAP is active for any bus cycle to an 8-bit peripheral that is addressing the odd byte.
SDLH/-HL	102	O	System Data Low to High, or High to Low - This signal is used to determine which direction data bytes must be swapped when -SDSWAP is active. When SDLH/-HL is high, it indicates that data on the low byte must be transferred to the high byte. When SDLH/-HL is low, it indicates that data on the high byte must be transferred to the low byte. SDLH/-HL is low for 8-bit DMA memory read cycles. For non-DMA accesses, SDLH/-HL is low for any memory write or I/O write when -SBHE is low. SDLH/-HL is high at all other times.
-XDREAD	103	O	Peripheral Data Read - This output is active low any time an INTA cycle occurs or an I/O read occurs to the address space from 0000h to 00FFh, which is defined as being resident on the peripheral bus.
-LATLO	104	O	Latch Low byte - This output is generated for all I/O read and memory read bus accesses to the low byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and Bus Controller.
-LATHI	105	O	Latch High byte - This output is generated for all I/O read and memory read bus accesses to the high byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and Bus Controller.
-PCK	111	I-TPU	Parity Check input, active low with pull-up - Indicates that a parity error has occurred in the on-board memory array. Assertion of this signal (if enabled) generates an NMI to the processor. The state of the -PCK signal is read as data bit D7 of the Port B register.
-HIDRIVE	113	I-TPU	High Drive Enable - This pin is a wire strap option. When this input is low, all bus drivers defined with an IOL spec of 24 mA will sink the full 24 mA of current. When this input is high, all pins defined as 24 mA have the output low drive capability cut in half to 12 mA. Note that all AC specifications ar done with the outputs in the high drive mode and a 200 pF capacitive load. -HIDRIVE has an internal pull-up and can be left unconnected if 12 mA drive is desired. It is tied low if 24 mA drive is desired.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
TEST MODE PIN			
–TRI	114	I-TPU	Three-state - This pin is used to control the three-state drive of all outputs and bidirectional pins on the chip. If this pin is pulled low, all pins on the chip except XTALOUT are in a high impedance mode. This is useful during system test when test equipment or other chips drive the signals or for hardware fault tolerant applications. –TRI has an internal pull-up.
POWER AND GROUND PINS			
The power connections are split into an internal supply for the core-logic, and a pad-ring supply for the I/O drivers. Each supply should be individually bypassed with decoupling capacitors.			
VDDR	19, 59, 100, 139	PWR	Pad-ring power connection, nominally +5 volts. These pins along with the VSSR pins should be separately bypassed.
VSSR	10, 20, 30, 40, 60, 80, 93, 106, 120, 130, 140, 150, 160	GND	Pad-ring ground connection, nominally 0 volts. These pins along with the VDDR pins should be separately bypassed.
VDDI	79	PWR	Internal core-logic power connection, nominally +5 volts. This pin along with the VSSI pin should be separately bypased.
VSSI	81	GND	Internal core-logic ground connection, nominally 0 volts. This pin along with the VDDI pin should be separately bypassed.

SIGNAL TYPE LEGEND

Signal Code	Signal Type
I-TTL	TTL level input
I-TPD	Input with 30k ohm pull-down resistor
I-TPU	Input with 30k ohm pull-up resistor
I-TSPU	Schmitt-trigger input with 30k ohm pull-up resistor
I-CMOS	CMOS level input
IO-TTL	TTL level input/ouput
IT-OD	TTL level input/open drain output
IO-OD	Input or open drain, slow turn on
O	CMOS and TTL level compatible output
O-TTL	TTL level output
O-TS	Three-state level output
I1	Input used for testing purposes
GND	Ground
PWR	Power

FUNCTIONAL DESCRIPTION

DETAILED SUBSYSTEM SPECIFICATION

The sections that follow cover detailed operational information for the various logical groupings of 82344 ISA Bus Controller subsystems. In most of these sections, the effect of any applicable configurable elements that can be controlled via indexed configuration registers is discussed at length. Operation of these registers is repeated in summary form in the "Configuration Register Operational Summary" section. However, some lesser configurable functions are described only in this section. Do not assume that the information in that section is discussed elsewhere.

MAJOR LOGIC BLOCK CHIP SELECT GENERATION

The 82344 ISA Bus Controller utilizes six megacells: two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer, and one real time clock. Programmable I/O access is required for these and other internal logic blocks. The logic block chip select subsection consists of decodes of the signals –MASTER, CPUHLDA and the address bus A15-A0. This decode is used to generate the chip select signals to each major logic block within the Bus Controller.

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Timing

The DMA subsection consists of two 8237 megacells, two 8-bit latches to hold the middle range address bits during a DMA cycle and 1.25 74LS612 page register equivalents to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to allow separate programming of the number of wait states for 8- and 16-bit DMA cycles. Defaults are standard AT-compatible wait states. The timing for the leading edge of the –XMEMR signal is also programmable. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8-bit I/O adapters and the other three are used for 16-bit I/O adapters. All channels are capable of addressing all memory locations in a 64 Mbyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to allow for 15 possible interrupt sources. Two of these interrupt request lines are used internally, so there are a total of 13 possible external interrupts.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters are driven by a common clock input. The output of counter zero is routed to the interrupt controller subsection to be used as interrupt request zero. The output from counter one drives the OUT1 pin to initiate refresh cycles. Counter two's output is gated with a signal from the Port B register and is then output as SPKR to drive the speaker.

The RTC megacell is a direct replacement for the 146818A real time clock component. Clock functions include the following:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- 114 bytes of User RAM

Address bits A15-A0 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

For all the address decodes shown, the inputs CPUHLDA and –MASTER must be low to generate a megacell chip select.

TABLE 1. A15-A0 ADDRESS DECODES

A15-8	A7	A6	A5	A4	A3	A2	A1	A0	Address	Chip Select Generated
0	0	0	0	0	X	X	X	X	000-00F	DMA1 (8237)
0	0	0	1	X	X	X	X	X	020-03F	Interrupt 1 (8259)
0	0	1	0	0	0	0	X	X	040-043	Counter (8254)
0	0	1	1	0	0	0	0	0	060	Reset IRQ1 and IRQ12
0	0	1	1	0	X	X	X	1	061-06F	Port B (Odd Only)
0	0	1	1	1	0	0	0	0	070	NMI Logic
0	0	1	1	1	0	0	0	0	070-071	Real Time Clock Access Ports
0	1	0	0	0	X	X	X	X	080-08F	DMA Page Registers
0	1	0	0	1	0	0	1	0	92	Port A*
0	1	0	1	X	X	X	X	X	0A0-0BF	Interrupt 2 (8259)
0	1	1	0	X	X	X	X	0	0C0-0DE	DMA2 (Even Only)
0	1	1	1	X	X	X	X	X	0E0-0EF	Configuration Registers*
1	1	1	1	X	X	X	X	X	0F0-0FF	Coprocessor CS and RESET*

*These entries are shown for completeness only. They are decoded and controlled by the System Controller except for ECh and EDh, which are also used by the Bus Controller's configuration registers.

DMA SUBSECTION

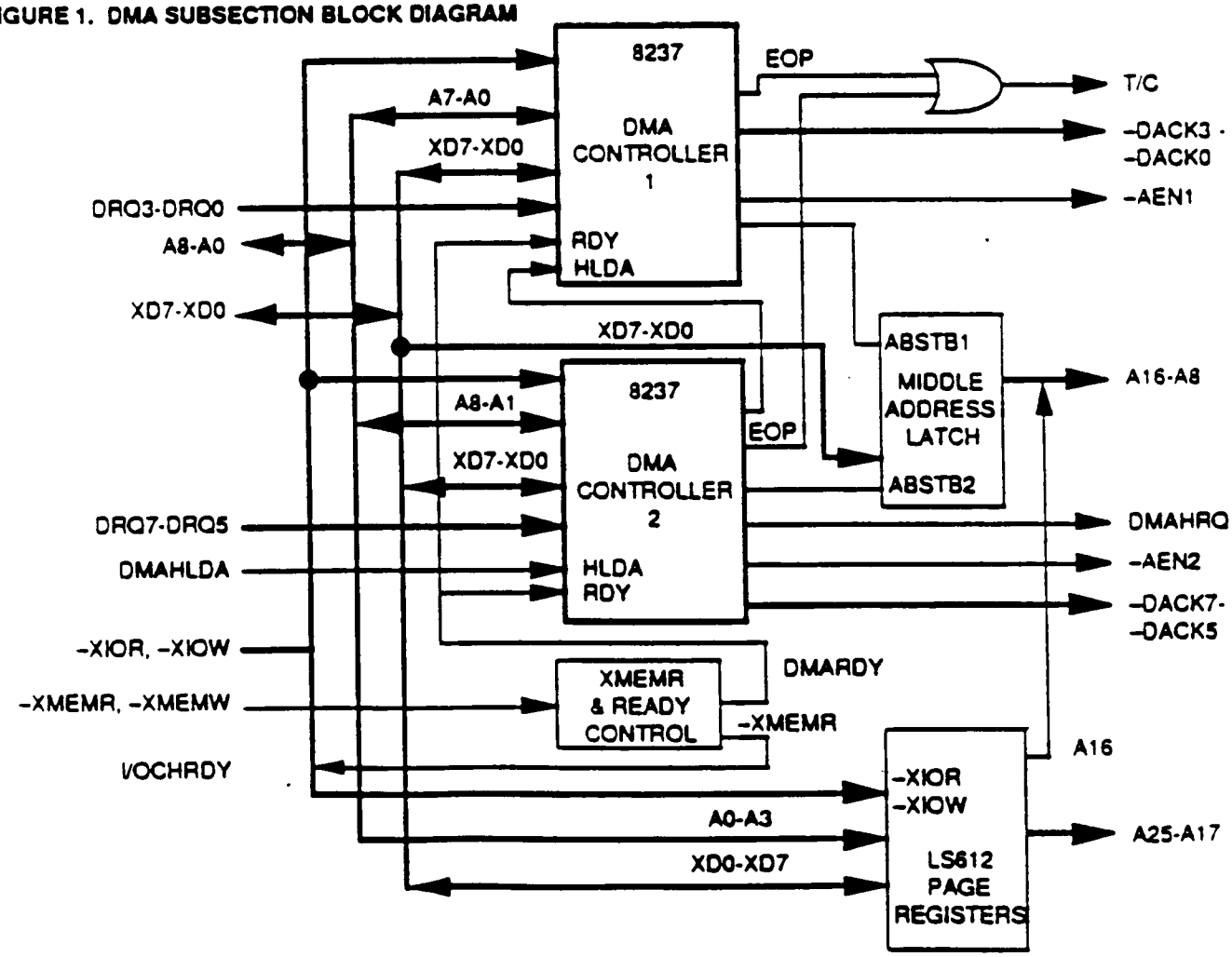
The DMA subsection controls DMA transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller will drive the CPU and the slot address buses. DMAs can occur over the full 16M range available on the slot bus and the 64M range of system board DRAM and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237-compatible. Internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus, and 1.25 74LS612 memory mappers are provided to generate the upper address bits. Since a single 74LS612 is only capable of accessing 16 Mbytes in an AT-compatible fashion, two additional bits are required to extend the architecture for a 64 Mbyte system. Therefore, an extra 1/4 of a 74LS612 is implemented. This is discussed in the section "Page Registers" and is functional only when used with the 82340DX chip set.

DMA Controllers

The Bus Controller supports seven DMA channels using two 8237 equivalent megacells capable of running at SYSCLK or SYSCLK/2. This option is programmable via the indexed configuration register, ROMDMA. DMA controller 1 contains channels 0 through 3. These channels support 8-bit I/O adapters. Channels 0 through 3 are used to transfer data between 8-bit peripherals and 8- or 16-bit memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space when used with the 82340DX chip set. Each channel can transfer data in 64 kilobyte pages.

DMA controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA controller 1, so it is not available externally. Channels 5 through 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. A full 26-bit address is output for each channel so they can all transfer data throughout the entire 64 Mbyte system address space. Each channel can transfer data in 128 kilobyte pages. Channels 5, 6 and 7 are meant to transfer 16-bit words only and cannot address odd bytes in system memory.

FIGURE 1. DMA SUBSECTION BLOCK DIAGRAM



DMA Controller Registers
The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA2 are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's address or word count register, the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only, the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16-bit registers. The value on the data bus is written into the upper or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the clear byte pointer flip-flop command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count register will read/write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 8237 data sheet for more information on programming the 8237 megacell.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DREQ and –DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the –DACK signals active low.

When programming the 16-bit channels (channels 5, 6 and 7), the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the mode registers, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

Middle Address Bit Latches
The middle DMA address bits are held in an internal 8-bit register. The DMA controller will drive the value to be loaded onto the internal data bus and then issue an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

TABLE 2. 8237 READ/WRITE ADDRESS

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Channel 0 Base and Current Address Register
0C2	001	Channel 0 Base and Current Word Count Register
0C4	002	Channel 1 Base and Current Address Register
0C6	003	Channel 1 Base and Current Word Count Register
0C8	004	Channel 2 Base and Current Address Register
0CA	005	Channel 2 Base and Current Word Count Register
0CC	006	Channel 3 Base and Current Address Register
0CE	007	Channel 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-flop
0DA	00D	Read Temporary Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

Page Registers

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
612AXS	Enable FF	4XX Enable	1	1	1	1	1	FF PTR

An extended 74LS612 cell is used in the Bus Controller to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do no increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16-bit channels (channels 5, 6 and 7) are every 128 kilobytes. There are a total of 16 8-bit registers and eight 2-bit registers in the extended 612 megacell.

The indexed configuration register ROMDMA is used to program the extended DMA features. In addition to the description below, see the section "Configuration Register Operational Summary" for more information. Bit 7 enables the extended DMA functions. The 82340DX chip set contains a superset of the PC/AT DMA design which allows full access to the entire 64M range of the 82340DX chip set. In order to do this, a second 612 memory mapper subset is added to allow access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. At power-on-reset, this bit defaults to 0 for complete AT-compatibility.

Bit 6 enables EISA compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX in accordance with Table 3. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used.

Bit 0 allows access to either the lower address bits, A16-A23 of the DMA page register when set to 0 or allows access to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. As an example, when bit 7 = 1 and bit 0 = 0, a write to address 8Ah will update A16-A23 in the lower DMA page register space. Bit 0 auto-increments on any write to the DMA register space between 80h and 8Fh. Therefore, if the next operation is a write to 8Ah, the upper address bits A24 and A25 are updated. The next access to this register space automatically accesses the lower byte of that address. Whenever D7 = 0, this bit is reset and held at logic 0. This bit is reset to 0 on POR.

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080h and 08Fh not shown in Table 4 and are not used by the DMA channels, but can be read or written to by the CPU. Address 08Fh (and 48Fh) is used to drive a value onto the upper address bits A25-A17 of the CPU's address bus during a refresh cycle.

Important Difference for 82340SX Chip Set Users

The 82340SX chip set for use in 286- and 386SX-based systems has a 32 Mbyte limit for its largest memory map. However, only the standard DMA operation below 16 Mbytes is supported. When the Bus Controller is strapped for 286 mode via no connect or external pull-up on the 286/–386 pin, bits 6 and 7 of the 612AXS indexed register are held low. This disables extended DMA mode. Attempts to write a 1 to these bits via software has no effect and subsequent reads of the bits will return a 0.

TABLE 3. DMA PAGE REGISTER ACCESS OPTION 1

A25-A24 Address		A23-A16 Address	DMA Channel
B6=1	B6=0	B6=X	
487h	NA	87h	0
483h	NA	83h	1
481h	NA	81h	2
482h	NA	82h	3
488h	NA	88h	5
489h	NA	89h	6
48Ah	NA	8Ah	7
48Fh	NA	8Fh	–REFRESH

TABLE 4. DMA PAGE REGISTER ACCESS OPTION 1

A25-A24 Address	A23-A16 Address	DMA Channel
B0=1, B7=1	B0=0, B7=1	
87h	87h	0
83h	83h	1
81h	81h	2
82h	82h	3
88h	88h	5
89h	89h	6
8Ah	8Ah	7
8Fh	8Fh	–REFRESH

Address Generation

The DMA addresses are set up such that there is an upper address portion, used to select a specific page, a middle address portion used to select a block within the page and a lower address portion.

The upper address portion is generated by the page registers, in the 74LS612 equivalent megacell. The page registers for each channel must be set up by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8-bit channels (channels 0 through 3) and 128 kilobytes for 16-bit channels (channels 5, 6 and 7). The DMA page register values are output on A25-A16 for 8-bit channels and A25-A17 for 16-bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are, 256 bytes for 8-bit channels (channels 0 through 3) and 512 bytes for 16-bit channels (channels 5, 6 and 7). This middle address portion is output by the 8237 megacells onto the internal data bus during state S1. The internal middle address bit latches will latch this value in. The middle address bit latches are output on A15-A8 for 8-bit channels and A16-A9 for 16-bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on A7-A0 for 8-bit channels and A8-A1 for 16-bit channels. A0 and –SBHE are forced low during 16-bit DMA operations. –SBHE is forced to the opposite value of A0 for 8-bit DMA.

–SBHE is configured as an output during all DMA operations and will be driven as the inversion of A0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

TABLE 5. DMA ADDRESSING FOR SLOT BUS ACCESSES

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			S/LA20	S/LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		–A0	–SBHE	
		VSS		–SBHE

Table 5 shows the mapping from the DMA subsystem signals to slot bus signals for both the 82340DX and 82340SX chip sets. For the latter chip set, the equivalent signals are also driven onto the local address bus. Table 6 shows the mapping of DMA subsystem signals to local address bus signals for the 82340DX system.

Ready Control

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. The Bus Controller ready control logic forces the preprogrammed number of wait states on every DMA transfer. POR defaults to one wait state for both 8- and 16-bit transfers. Other options can be programmed after Power on Reset in the indexed configuration register ROMDMA. The external signal I/OCHRDY goes into the ready control logic to further extend transfer cycles if needed. To add extra wait states, an external device should pull I/OCHRDY low within the setup time before the second phase of the internal DMA clock no later than the last forced wait state cycle. The current DMA cycle will then be extended by inserting wait states until I/OCHRDY is returned high. I/OCHRDY going high must meet the setup time at the beginning of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4.

External Cascading

An external DMA controller or bus master can be attached to an AT-compatible design through the Bus Controller's DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channels DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding –DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the seven channels is programmed in cascade mode and that channel is acknowledged, the Bus Controller will not drive the data bus, the command signals or the address bus.

TABLE 6. DMA ACCESSES ON SYSTEM BOARD DRAM

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9			A25	A24
M8			A24	A24
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	*	A2
		A0	*	**

*Byte Enables BE0-BE3# Controlled:

Case	A0	A1	BE3#	BE2#	BE1#	BE0#
1	0	0	High	High	High	Low
2	0	1	High	High	Low	High
3	1	0	High	Low	High	High
4	1	1	Low	High	High	High

**Byte Enables BE0-BE3# Controlled:

Case	A0	BE3#	BE2#	BE1#	BE0#
1	0	High	High	Low	Low
2	1	Low	Low	High	High

An external device can become a bus master and control the system address, data and command buses in much the same manner. One of the external channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's –DACK line goes active, the external device can then pull the –MASTER signal low. As in the DMA controller cascading, the Bus Controller does not drive the address, data and command signals while the cascaded channel's –DACK signal is active.

TABLE 7. DMA ADDRESSING SYSTEM BOARD MEMORY IN 286/386SX MODE

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	A1	A2
		A0	A0/–BLE	A1
		VSS		A0/–BLE
		–A0	–BHE	
		VSS		–BHE

Programming DMA Options

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Timing

The original PC/AT DMA specification is lacking in the true speed one normally associates with DMA activity. For compatibility, the Bus Controller fully supports that specification as its POR defaults. However, a variety of programmable options are provided in order to enhance DMA performance, if desired. The extended DMA support for 64 Mbyte memory space in the 82340DX chip set has previously been addressed in the "Page Registers" section. In the following sections, programmable wait state, DMA clock, and –MEMR timing are discussed. Actual programming of the ROMDMA registers in order to effect the desired system performance changes is covered in the "Configuration Register Operational Summary" section.

DMA Wait States
Zero, one, or two wait states can be independently programmed for 8-bit and 16-bit DMA transfers. (Default = one wait state.)

DMA Clock
The DMA clock can be programmed to occur at the normal SYSCLK/2 rate (bit 1 = 0) or at SYSCLK rate (bit 1 = 1).

–MEMR Delay
To maintain an AT-compatible design, the Bus Controller POR default inserts a one DMA clock cycle delay in the falling edge of the –MEMR signal. –MEMR will go low one DMA clock later than the –MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time the –MEMR signal from the megacell goes high. This maybe reprogrammed to remove this one clock cycle delay on the falling edge of –MEMR by setting bit 0 of ROMDMA to a 1.

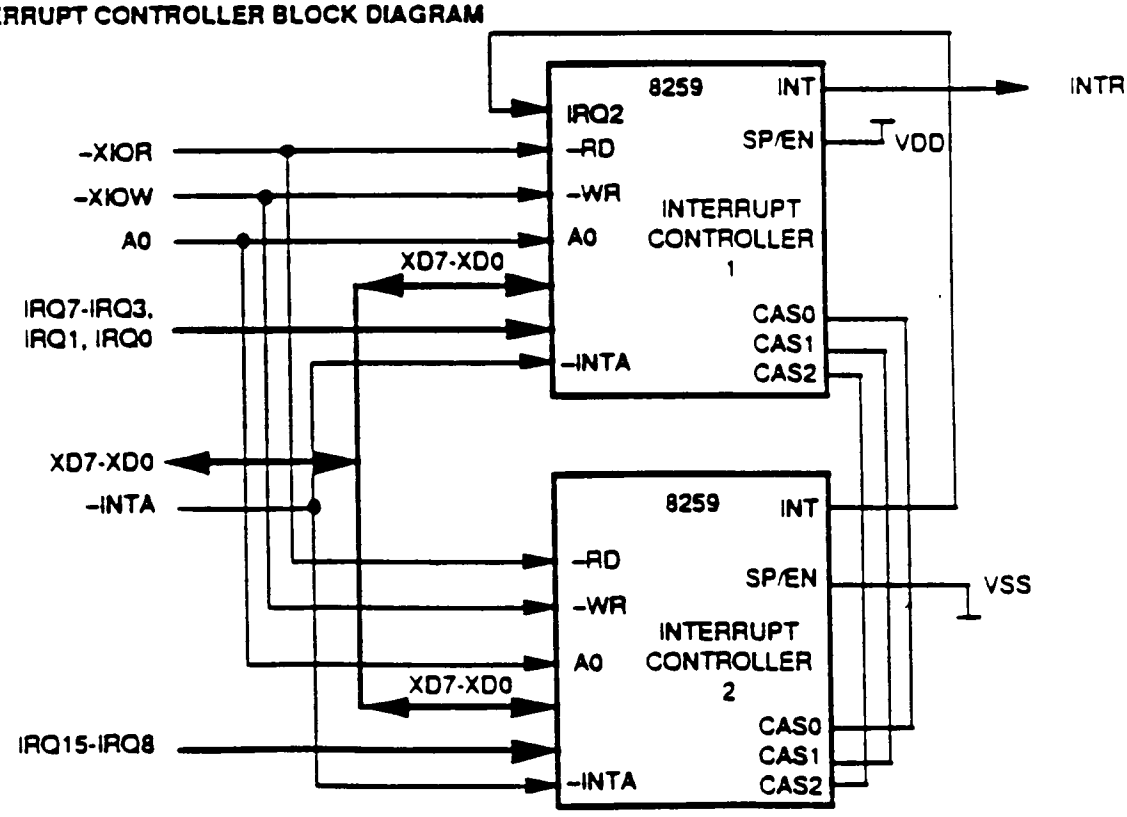
INTERRUPT CONTROLLER SUBSECTION
The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally on the Bus Controller and two of the interrupt request inputs are connected to internal circuitry. This allows a total of 13 external interrupt requests.

All external interrupt request signals have an internal pull-up resistor to eliminate noise on unconnected request pins.

The following interrupt request signals are different from the standard interrupt request in some way.

IRQ0 This interrupt is connected to the OUT0 of the 8254 megacell and is not available as an external input.

FIGURE 2. INTERRUPT CONTROLLER BLOCK DIAGRAM



IRQ2 IRQ2 is used to cascade the two 8259 megacells together and is not available as an external input.

–IRQ8 –IRQ8 input is internally connected to the real time clock megacell's interrupt pin.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the –INTA pulses from the CPU. On the first –INTA cycle the cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second –INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the Bus Controller, they should never be programmed to operate in the buffered mode. See the section "ISA Bus Controller/System Controller Interchip Communication" for special use of interrupt control during sleep mode.

Interrupt Controller Registers
The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 8 shows the correct addressing for each of the 8259 registers.

TABLE 8. INTERRUPT CONTROLLER WRITE OPERATIONS

INT1	INT2	XD4	XD3	Register Function
020H	0A0H	1	X	Write ICW1
021H	0A1H	X	X	Write ICW2
021H	0A1H	X	X	Write ICW3
021H	0A1H	X	X	Write ICW4 (if needed)
021H	0A1H	X	X	Write OCW1
020H	0A0H	0	0	Write OCW2
020H	0A0H	0	1	Write OCW3

TABLE 9. INTERRUPT CONTROLLER READ OPERATIONS

INT1	INT2	Register Function
020H	0A0H	Interrupt Request Register, In-Svc Register or Poll Command
021H	0A1H	Interrupt Mask Register

Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3 and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 8259 megacell, ICW3 is optional. But since the two 8259's in this chip are cascaded together they should always be programmed in cascade mode and ICW3 will always be needed. Refer to the 8259 data sheet for more information on programming the 8259 megacell.

When reading at address 020h or 0A0h hex, the register read will depend on how Operation Control Word 3 was set up prior to the read.

COUNTER/TIMER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in Figure 3. The clocks for each of the three internal counters are tied to the 14.318 MHz oscillator through a divide by 12 counter. The gate inputs of counters zero and one are tied high to enable those counters at all times. The gate input of counter two is tied to bit 0 of the Port B register inside the Bus Controller.

One of the 8254 megacell counter outputs is directly available at an external pin. Counter zero's output is connected to the IRQ0 input of interrupt controller one. Counter one's output goes to the pin OUT1. Finally, counter two's output goes to an AND gate which drives the output pin SPKR. The other input on this AND gate is connected to bit 1 of the Port B register.

Counter/Timer Registers

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 10 shows the correct addressing for each of the 8254 registers.

The write control word at address 043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

FIGURE 3. COUNTER/TIMER BLOCK DIAGRAM

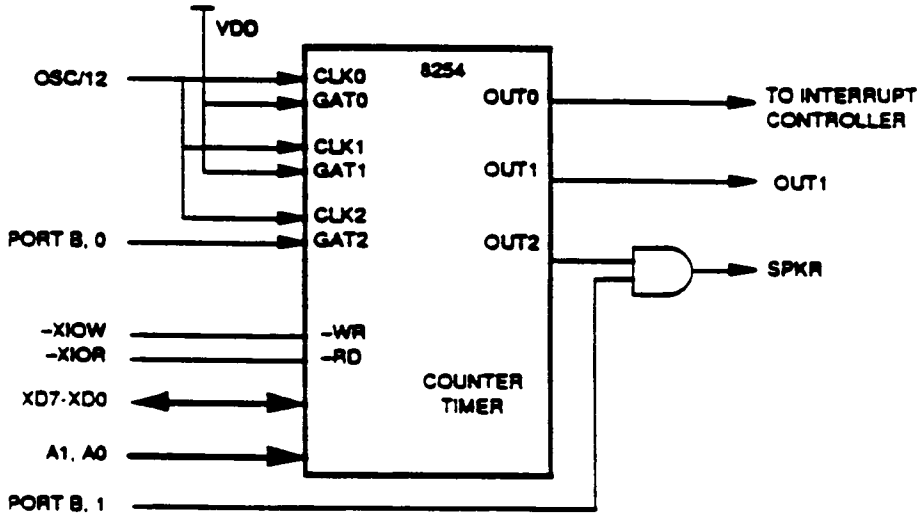


TABLE 10. COUNTER/TIMER ADDRESSING REGISTERS

Addr	-XIOR	-XIOW	Register Function
040H	1	0	Write Initial Count to Counter
040H	0	1	Read Count/Status from Counter 0
041H	1	0	Write Initial Count to Counter 1
041H	0	1	Read Count/Status from Counter 1
042H	1	0	Write Initial Count to Counter 2
042H	0	1	Read Count/Status from Counter 2
043H	1	0	Write Control Word
043H	0	1	No Operation

REAL TIME CLOCK

The Bus Controller contains an enhanced 146818 real time clock megacell. It is 100% compatible with the 146818 and contains additional battery backed RAM within its address space in order to support non-volatile configuration register storage. Enough storage is provided to store the Bus Controller's and System Controller's configuration data. Additional storage is provided in order to support future chip set enhancements.

Real Time Clock Programmer's Model

The RTC memory consists of ten RAM bytes which contain the time, calendar, and alarm data, four control and status bytes, and 114 general purpose RAM bytes. The address map of the real time clock is shown in Table 11.

All 128 bytes are directly readable and writeable by the processor program except for the following:

1) Registers C and D are read-only.
2) Bit 7 of Register A is read-only.
3) Bit 7 of the seconds byte is read-only.

This RTC configuration represents an extension to the 146818 architecture. An additional 64 bytes of standby RAM have been added to the 146818 memory map. This area provides space to store chip set configuration data and provides ample additional storage in order to support future chip set versions and extra BIOS scratch pad memory.

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Time of Day Register Descriptions

The contents of the time of day registers can be either in binary or BCD format. They are relatively straightforward, but are detailed here for completeness. The address map of these registers is shown in Table 12 and below.

TABLE 11. REAL TIME CLOCK ADDRESS MAP

Addr	Function	Range
0	Seconds (Time)	0-59
1	Seconds (Alarm)	0-59
2	Minutes (Time)	0-59
3	Minutes (Alarm)	0-59
4	Hours (Time)	1-12; 12 Hour Mode
4	Hours (Time)	0-23; 24 Hour Mode
5	Hours (Alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99
10	RTC Register A	(Read/Write)
11	RTC Register B	(Read/Write)
12	RTC Register C	(Read-only)
13	RTC Register D	(Read-only)
14-127	User RAM (Standby)	

TABLE 12. TIME OF DAY REGISTER ADDRESS

Addr	Function	Range
0	Seconds (Time)	0-59
1	Seconds (Alarm)	0-59
2	Minutes (Time)	0-59
3	Minutes (Alarm)	0-59
4	Hours (Time)	1-12; 12 Hour Mode
4	Hours (Time)	0-23; 24 Hour Mode
5	Hours (Alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds:
The range of this register is 0-60 in BCD mode, and 0-3BH in binary mode.

Address 1 - Seconds Alarm:
The range of this register is 0-60 in BCD mode, and 0-3BH in binary mode.

Address 2 - Minutes:
The range of this register is 0-60 in BCD mode, and 0-3BH in binary mode.

Address 3 - Minutes Alarm:
The range of this register is 0-60 in BCD mode, and 0-3BH in binary mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 5 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01H-0CH	Binary	AM
81H-8CH	Binary	PM

Address 6 - Day of Week:
The range of this register is 1-7 in BCD mode, and 1-7H in binary mode.

Address 7 - Date:
The range of this register is 1-31 in BCD mode, and 1-1FH in binary mode.

Address 8 - Month:
The range of this register is 1-12 in BCD mode, and 1-0CH in binary mode.

Address 9 - Year:
The range of this register is 0-99 in BCD mode, and 0-63H in binary mode.

RTC Control Register Descriptions
The 146818 megacell has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Addr	Function	Type
10	RTC Register A	R/W
11	RTC Register B	R/W
12	RTC Register C	R-O
13	RTC Register D	R-O
14-63	User RAM (Standby)	R/W

Register A Description
This register contains control bits for the selection of periodic interrupt, input divisor, and the update in progress status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select Bit 0	RS0
1	Rate Select Bit 1	RS1
2	Rate Select Bit 2	RS2
3	Rate Select Bit 3	RS3
4	Divisor Bit 0	DV0
5	Divisor Bit 1	DV1
6	Divisor Bit 2	DV2
7	Update in Progress	UIP

Bits 0 through 3 - The four rate selection bits (RS0 to RS3) select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by RESET. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate
0	None
1	3.90625 ms
2	7.8125 ms
3	122.070 µs
4	244.141 µs
5	488.281 µs
6	976.562 µs
7	1.953125 ms
8	3.90625 ms
9	7.8125 ms
0AH	15.625 ms
0BH	31.25 ms
0CH	62.5 ms
0DH	125 ms
0EH	250 ms
0FH	500 ms

Bits 4 through 6 - The three divisor selection bits (DV0 through DV2) are fixed to provide for only a 5-state divider chain, which would be used with a 32 KHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed, the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, Divider Running
6	Reset Mode, Divider in Reset State

Bit 7 - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a 1, the update cycle is in progress or will soon begin. When UIP is a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar and alarm information in RAM is fully available to the program when the UIP

bit is 0. The UIP bit is a read-only bit, and is not affected by RESET. Writing the SET bit in register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description
Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12 Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Not Used	
4	Update End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 - The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is 1). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is 0. DSE is not changed by any internal operations or reset.

The elimination of this feature will be considered, since the start date of daylight savings time is currently being changed.

Bit 1 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (1) or the 12-hour mode (0). This is a read/write bit, which is affected only by software.

Bit 2 - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM signifies binary data, while a 0 signifies BCD data.

Bit 3 - This bit is unused in this version of the RTC, but is used for Square Wave Enable in the 146818.

Bit 4 - The UIE (update end interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in register C to assert an IRQ. The RESET pin being asserted or the SET bit going high, clears the UIE bit.

Bit 5 - The alarm interrupt enable (AIE) bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in register C to assert an IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an IRQ signal. The RESET pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 - The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic interrupt flag (PF) bit in register C to cause the IRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in register A. A 0 in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by an internal functions, but is cleared to 0 by a reset.

Bit 7 - When the SET bit is a 0, the update cycle functions normally be advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes wihtough an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description
Register C contains status information about interrupts and internal operation of the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Not Used. Read as 0	
1	Not Used. Read as 0	
2	Not Used. Read as 0	
3	Not Used. Read as 0	
4	Update Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	IRQ Pending Flag	IRQF

Bits 0 through 3 - The unused bits of status register 1 are read as 0's and cannot be written.

Bit 4 - The update ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting the IRQ. UF is cleared by a register C read or a reset.

Bit 5 - A 1 in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A 1 in the AF causes the IRQ pin to go low, and a 1 to appear in the IRQF bit, when the AIE bit also is a 1. A reset or a read of register C clears AF.

Bit 6 - The periodic interrupt flag (PF) is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an IRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of register C.

Bit 7 - The interrupt request flag (IRQF) is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the IRQ pin is asserted. All flag bits are cleared after register C is read by the program or when the RESET pin is asserted.

Register D Description

This register contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Valid RAM Data and Time	VRT

Bits 0 through 6 - The remaining bits of register D are unused. They cannot be written, but are always read as 0's.

CMOS Standby RAM Description

The 114 general purpose RAM bytes are not dedicated to RTC use within the 146818. They are fully available during the update cycle.

General Operational Notes

Set Operation:
Before initializing the internal registers, the SET bit in register B should be set to a 1 to prevent time/calendar updates from occurring. The program initialized the ten locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of register B. All ten time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the RTC makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the ten data bytes.

BCD VS Binary Format:
The 24/12 bit in register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high order bit of the hours byte represents PM when it is a 1.

Update Operation:
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 KHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation:
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is in any byte from 0C0H to 0FFH. An alarm interrupt each hour is created with "don't care" code in the hours alarm location. Similarly, an alarm is geerated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts:
The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 µs. The update ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in register B enable the three interrupts. Writing a 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enable, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a 1 in register C. Each of the three interrupt sources have separate flag bits in register C, which are set independent of the state of corresponding enable bits in register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control

The divider control bits are fixed for only 32.768 KHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the 146818RTC.

Square Wave Output Selection

This version of the 146818 does not support the square wave output function.

Periodic Interrupt Selection

The periodic interrupt allows the IRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle

The 146818RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV0 through DV2 divider is not clear, and the SET bit in register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing

update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 KHz time base update cycle takes 1984 µs, during which, the time, calendar, and alarm bytes are not accessible by the processor program. The 146818RTC protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update is progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during uprate are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in register C should be cleared.

The second method uses the update in progress bit (UIP) in register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is a read in the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a penodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is set high between the setting of the PF bit in register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

Power-down Mode

The RTC megacell is compatible with existing PC designs using the 146818A. The passive components that are critical for low power operation are shown in the Figure 4.

In Figure 4, the POWERGOOD signal from the power supply is used to control the power-down mode of the RTC.

When POWERGOOD is low, the RTC enters power-down mode. In this mode, all outputs are three-stated and read or write operations are inhibited. Any operation in progress (address entered but the data not yet accessed) is terminated and must restart from the beginning of the bus cycle for proper operation. A write operation in progress is completed if the write strobe has been low for a specified minimum time. Any write operation stopped prior to the minimum write strobe setup time will not have guaranteed results, since the data path is not double-buffered.

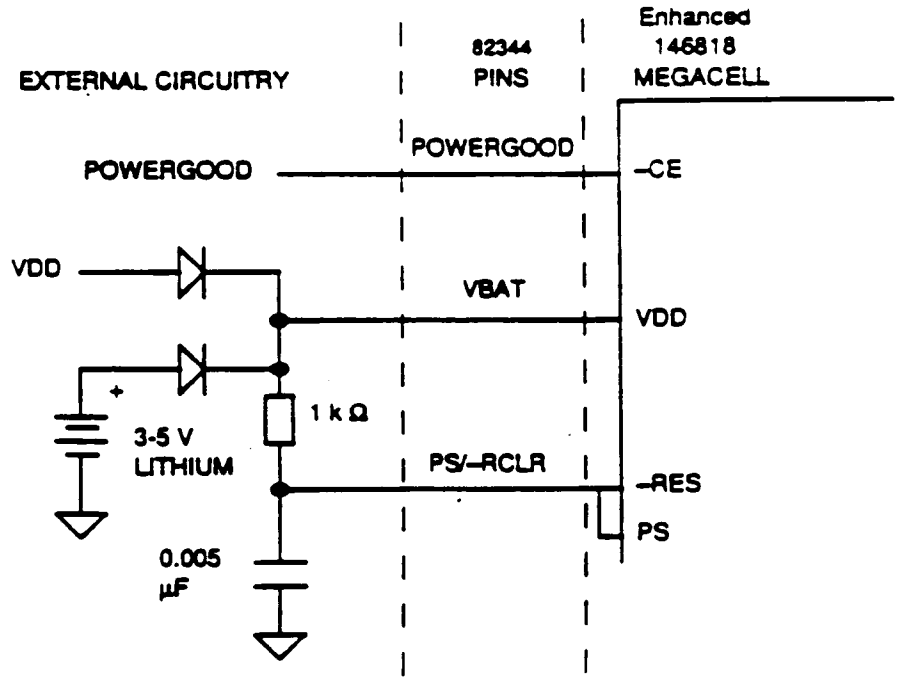
The Power Sense signal is used to reset the state of the Valid RAM and Time (VRT) bit. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

With a power consumption target specification of 5 µA, and a lithium battery with a capacity of 100 mA-Hr, time will be properly kept for approximately 2.25 years.

Disabling Internal RTC

When bit 6 of configuration register BUSCTL = 1, the internal RTC is disabled. The PS/–RCLR pin is configured as IRQ8 input from an external RTC. External logic must provide the external RTC with RTCAS, RTCDS, RTCRW.

FIGURE 4. RTC LOW POWER OPERATION CIRCUIT



BUS CONTROLLER REFRESH SUBSYSTEM

The System Controller performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. The Bus Controller actually performs the off-board refresh when commanded by the System Controller. Refresh may be performed in a coupled or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the System Controller has complete control over the timing of on-board DRAM refresh and and off-board refresh but the timing of each is independent. See the section "System Board DRAM Refresh" in the 82343 or 82346 data sheet for more information.

PORT B AND NMI LOGIC

The Bus Controller generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 070H with D7 low. Once enabled, an NMI can be generated by the IOCHCK input going low or the –PARERROR input going low. Each of these NMI sources has an enable bit in the Port B register to allow these inputs to cause an NMI when set high, or ignore the input if the bit is low.

The Port B register at I/O address 061 hex is included in the Bus Controller chip. This register contains bits to control the speaker output and NMI circuitry. Bits 0 through 3 are read/write bits, while bits 4 through 7 are read-only. Each bit of the register is defined below. Bits 0 through 3 are all set low by a reset.

Port B, 0 Speaker Timer 2 Gate (TIM2GAT_SPK). This bit goes to the gate 2 input on the 8254 megacell to enable counter 2 to produce a speaker frequency.

Port B, 1 Speaker Data (SPK_DAT). This bit is gated with the output of counter 2 from the 8254 megacell. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When this bit is low, the SPKR output is forced low.

Port B, 2 Enable RAM Parity Check (–ENA_RAM_PCK). When this bit is set low, it allows parity errors from the on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.

Port B, 3 Enable I/O Check (–ENA_IO_CK). When this bit is set low, it allows an NMI to be generated if the IOCHCK input is pulled low. Otherwise, the IOCHCK input is ignored and can not generate an NMI.

Port B, 4 Refresh Detect (REFDET). This bit is tied to a toggle flip-flop which is clocked by –REFRESH. It will toggle to the opposite state every time a refresh cycle occurs.

Port B, 5 Timer Output bit 2 state (OUT2). This bit indicates the current state of the OUT2 signal from the 8254 megacell.

Port B, 6 Channel Check (CHAN_CHK). This bit indicates that a peripheral device is reporting an error. It can only be set if –ENA_IO_CK is set low. IOCHERR should be cleared by writing a high to ENA_IO_CK.

Port B, 7 Parity Check (PCK). This bit indicates that an on-board RAM parity error has occurred. It can only be set if –ENA_RAM_PCK is set 0. –PCK should be cleared by writing a 1 to –ENA_RAM_PCK.

ISA BUS INTERFACE SUBSECTION

The 82344 ISA Bus Interface can be controlled from four possible sources. Three of these sources are generated in the Bus Controller chip. They are CPU mode, DMA mode, and refresh mode. The fourth possible source is a bus master.

In CPU mode, the Bus Controller receives bus cycle commands from the System Controller, executes them and responds back to the System Controller when the bus cycle is complete. When in this mode, the 288 megacell is responsible for generating the command (–IOR, –IOW, –MEMR, –MEMW, –SMEMR, and –SMEMW) signals, BALE and the timing for when the SA bus will be valid. The Bus Controller samples the inputs –MEMCS16, –IOCS16, IOCHRDY, and –WS0 and combines these with internally defined definitions to determine the length in wait states of each bus cycle.

Refresh modes are initiated as described above. During refresh the bus controller will drive the –REFRESH signal, a refresh address and –MEMR command onto the bus to implement the refresh cycle. The refresh circuit samples IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The outputs AEN and BALE are both driven high during the refresh cycles.

In DMA mode, the Bus Controller is driven from one of the 8237 DMA controller megacells. The DMA controllers generate the command and address signals. BALE is forced high for all DMA cycles. The bus controller asserts the AEN signal to indicate that the current address on the bus is for memory only and not to be decoded as an I/O address. The DMA section samples IOCHRDY to extend bus cycles longer than the internally defined cycle length.

Bus master mode is an extension of DMA mode. A master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the Bus Controller relinquishes control of the bus to the master. While in master mode, the Bus Controller buffers the address lines and drives them onto the local address bus (A bus) to be used to address on-board memory.

Extended Slot Bus Timing Options

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL	NA Ctrl	RTC Ctrl	10/16 IO	1	ADDLY	RLX Timing	16 WS	8 WS

Four bus control options are provided and are programmable via the indexed BUSCTL register. On reset, the four control bits are reset to 0. This specifies the full PC/AT-compatibility mode.

When bit 0 = 1, an extra wait state is added for 8-bit slot bus accesses. This yields five rather than the normal four wait states. This allows slower boards to operate with equivalent performance when higher bus speeds are used.

When bit 1 = 1, an extra wait state is added for 16-bit slot bus accesses. This yields two instead of the normal one for I/O accesses and one instead of zero for memory accesses.

When bit 2 = 1, an extra command delay is added for 16-bit memory cycles.

When bit 3 = 1, an extra command delay is added for 8- and 16-bit I/O cycles and for 8-bit memory cycles.

Note: Zero wait state is possible on extremely fast boards that can pull the 0WS line fast enough and more than five wait states are possible if IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if IOCHRDY has previously been activated.

ROM ACCESS CONTROL SUBSECTION

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Timing

Bits 6 and 7 of the ROMDMA configuration register allow programming the number of wait states for ROM accesses in the E0000h to FFFFFh BIOS area. Range is from 1 to 3 slot bus cycle wait states. The POR default is three wait states. Shadow RAM features of the Sytem Controller are recommended to speed BIOS access. ROM decode logic in the Bus Controller provides a single ROM chip select for this BIOS region. A chip select also results from decode of the middle BIOS address space between FE0000h and FFFFFFh and also the upper BIOS space from FFFE0000h to FFFFFFFFh.

ISA BUS CONTROLLER/SYSTEM CONTROLLER INTERCHIP COMMUNICATION

The asynchronous interface to the Bus Controller is handled by a group of signals from the System Controller. –CHS0, –CHS1 and CHM/–IO define which type of cycle is to be executed as follows:

CHM/–IO	–CHS1	–CHS0	Bus Cycle
0	0	0	–INTA
0	0	1	–IOR
0	1	0	–IOW
0	1	1	Reserved
1	0	0	–REFRESH
1	0	1	–MEMR
1	1	0	–MEMW
1	1	1	Reserved

POWER SAVING SLEEP MODE

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	Enable	1	1	1	1	1	1	SYSCLK

Bit 7 of the sleep register is set to 1 in order to enable sleep function. It is write-only at indexed register port 13h because it duplicates the address and bit position of the sleep enable function in the System Controller. (For test purposes, the Bus Controller register can be read and written at indexed location 83h.) The Bus Controller sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems. When activated by the CPU via an I/O write to bit 7 of the sleep register, the DMA subsystem and the AT slot bus subsystems are shut off. The interrupt controllers and the timers continue to operate. When an interrupt occurs due to an external source or internal timer zero, the Bus Controller passes it to the CPU. The CPU then resets bit 7 of the sleep register. This brings both the System Controller and the Bus Controller out of the sleep state.

Setting bit 0 = 0 disables the SYSCLK oscillator (BUSCLK/2) if bit 7 is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If bit 0 = 1, the oscillator is always enabled even in sleep mode.

In operation, bit 0 is set for the desired operational mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of sleep mode during operation.

IN-CIRCUIT TEST LOGIC

During In-Circuit Test (ICT) all of the outputs can be toggled by one or more inputs. This allows for a board level tester to test the solder connections for each signal pin.

The sequence for enabling ICT is as follows:

1) Tester drives –TRI signal to 0.
4) Tester drives D0 to 0 (D7-D1 must all be 0's).
5) Tester pulses –IOR and –IOW low for 100 ns (minimum).
6) Tester drives –TRI signal to 1 (outputs now enabled).

The sequence for disabling ICT is assertion of RESET.

CONFIGURATION REGISTER OPERATIONAL SUMMARY

Table 13 at end of this section shows a mapping of the 82344 ISA Bus Controller indexed configuration registers. These registers are accessed through a single port address as described in the "Index Register" section that follows.

Other configuration register sets exist in the Bus Controller. The DMA controllers, interrupt controllers, and counter/timers have separate I/O registers at the PC/AT-compatible locations.

Index Register (0ECh) (Write-Only)

The value written to this register is the 8-bit address of the data port which is accessed through the data port register at I/O address 0EDh. All subsequent data port reads and writes will access the register at this address until the index register is written with a new 8-bit address. This register is write-only. The index register and data port register, described below, share common addresses with the index and data port registers located in the System Controller. A write to the index register at 0ECh is latched into both the System Controller and Bus Controller. Only the System Controller index register is readable in order to avoid bus collisions.

Data Port Register (I/O Address 0EDh)

Each register accessible through I/O address 0EDh is functionally described next. It is accessed first by writing its address to the index register at I/O address 0ECh, then by accessing the data port at I/O address 0EDh. All data ports in the Bus Controller are located in the range 80h to FFh to avoid contention with data ports located in the System Controller. However, there is one exception. See the section "Sleep Register" for details.

Version (80h) (Read-Only)

D2-D7 will contain a code which indicates that this part is an Intel PC/AT-compatible ISA Bus Controller. D0 and D1 contain the version number of this chip. By using this byte a smart BIOS can compensate for "feature" differences based on the version number. The code F8h is used in the initial version of this chip. By breaking the code in two bit pieces, it is revealed to be "344" Rev. "0."

ROMDMA (81h)

Bits 6 and 7 indicate the number of ROM wait states. These wait states are timed in slot bus cycles. The valid range is 1 to 3.

0X = 1 wait state
10 = 2 wait states
11 = 3 wait states (Default)

Bits 4 and 5 are encoded with the number of 8-bit DMA wait states as follows:

00 = 0 wait states
X1 = 1 wait state (Default)
10 = 2 wait states

Bits 2 and 3 are encoded with the number of 16-bit DMA wait states as follows:

00 = 0 wait states
X1 = 1 wait state (Default)
10 = 2 wait states

Bit 1 = 1 for DMA clock = SYSCLK. Bit 1 = 0 for SYSCLK/2. (Default = 0.)

Bit 0 = 0 delay DMAMEMR# one clock cycle later than XIOR#. Bit 0 = 1 start DMAMEMR# and XIOR# go active concurrently. (Default = 0.)

612AXS (82h)

Bit 7 enables the extended DMA functions when set to 1 by allowing access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. This latter mode is fully compatible with the PC/AT-standard. When bit 7 = 1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. See the bit 0 discussion below for more detail. (Default = 0.)

Bit 6 enables EISA I/O access compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX where XX = the same address as the lower page register byte. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used. (Default = 0.)

Note - When the external 286/–386 pin is not tied to ground, bits 6 and 7 are held low disabling the extended DMA mode. Attempts by software to write logic 1's to these bits has no effect and subsequent reads will return 0. The extended DMA function is not supported when the 82344 ISA Bus Controller is used with the 82343 System Controller in 286- or 386SX-based systems.

Bits 1 through 5 are read-only and will always return logic 1's.

Bit 0 allows access via the same I/O addresses to the lower address bits, A16-A23 of the DMA page register when set to 0 or to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. (Default = 0.)

Sleep (13h) (Write-only)
SLEEP (83h) (Read/Write for Factory or Post Test)
This special case register shadows the sleep register at the same indexed register location as in the System Controller. D7 and D0 are the only active bits in the Bus Controller. In standard operation, a read of indexed register 13h will return the register's contents as last written and latched into the System Controller. For test purposes, the Bus Controller sleep register can be read and written at indexed location 83h. In normal operation, however, all reads and writes should be performed through indexed register 13h.

Bit 7- Power-down enable.
0 = Default setting. Normal PC/AT-compatible operation.
1 = Effect of sleep on bus controller TBD.

This bit is reset to zero and normal operation resumes when rewritten or when a hardware reset of the Bus Controller occurs.

Bits 1 thtrough 6 are read-only and return logic 1's when a read of indexed register 83h is performed.

Bit 0 can be used to disable the SYSCLK signal to the slot bus. When set to 0 and bit 7 is set to 1, the SYSCLK signal is shutdown until bit 7 is reset to 0. If bit 0 = 1, SYSCLK is enabled to the slot bus regardless of the state of bit 7. (Default = 1.)

BUSCTL (84H)
Bit 7, when set to a logic1, allows the 386DX or 386SX NA# pin to be tied low for pipeline control rather than dynamically controlling NA# in real time via the System Controller's NA# output pin. More pipeline mode timing margin results. When set to logic 0, pipeline mode must be dynamically controlled via the System Controller's NA# pin with bit 4 of the System Controller's RAMSET register set to 1. (Default = 0.)

Bit 6 allows the internal RTC to be disabled if use of an external RTC is prefered. Bit 6 = 1 disables the internal RTC and redefines the PS/–RCLR pin to IRQ8 in. (Default = 0.)

Bit 5 controls internal I/O decode. When bit 5 = 0, full 16-bit decode is performed. When bit 5 = 1, 10-bit decode is performed. (Default = 0.)

Bit 4 is are read-only and always return logic 1's.

Bit 3 allows addition of one extra command delay for 8- and 16-bit I/O cycles and for 8-bit memory cycles. (Default = 0, no added command delays.)

Bit 2 determines whether to use the PC/AT-compatible zero command delays on 16-bit memory cycles or whether to add one. (Default = 0, no command delays on 16-bit memory cycles.)

Bit 1 determines whether to use zero or one wait states for 16-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible zero wait states are used. When set to 1, one wait state is used to allow robust operation of add-in cards at faster slot speeds. (Default = 0, zero wait states on 16 slot bus accesses.)

Bit 0 determines whether to use four or five wait states for 8-bit slot bus accesses. When bit 1 = 0, the PC/AT-compatible four wait states are used. When set to 1, five wait states are used to allow robust operation of add-in cards at faster slot speeds. (Default = 0: four wait states on 8-bit slot bus accesses.)

TABLE 13. ISA BUS CONTROLLER CONFIGURATION REGISTER MAP

Index Port	D7	D6	D5	D4	D3	D2	D1	D0
0ECh (W-O)	A7	A6	A5	A4	A3	A2	A1	A0

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
VER (R-O)	1	1	1	1	1	0	0	0
ROMDA	ROM Wait States		8-Bit DMA Wait States		16-Bit DMA Wait States		DMA Clock	MEMR Time
612AXS	Enable FF	4XX Enable	1	1	1	1	1	FF PTR
SLEEP	Enable	1	1	1	1	1	1	SYSCLK
BUSCTL	NACtrl	RTC Ctrl	10/16 IO	1	ADDLY	RLX Timing	16 WS	8 WS

Note: A 1 indicates reserved register bits that read back as logic 1.

TABLE 14. CONFIGURATION REGISTER DEFAULTS ON RESET

Data Port 0EDh (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
VER (R-O)	1R	1R	1R	1R	1R	0R	0R	0R
ROMDA	1	1	1	1	1	1	0	0
612AXS	0	0	1R	1R	1R	1R	1R	0
SLEEP	0*	1R	1R	1R	1R	1R	1R	1*
BUSCTL	0	0	0	1R	0	0	0	0

*These two bits are read/write at address 83H and write-only at address 13h. All other sleep register bits are write-only at address 13h and read-only at address 83H.

AC CHARACTERISTICS: TA = 0°C to +70 °C, VDD = 5 V ±5%, VSS = 0V

This section contains a set of preliminary timing diagrams. AC values for these diagrams are not yet available. Additional timing diagrams and AC values will be forthcoming. The following diagrams are shown below:

DMA: 8- and 16-bit DMA waveforms are shown. These are the default waveforms. They can be modified by programming values into the ROMDMA configuration register.

Interrupt Timing

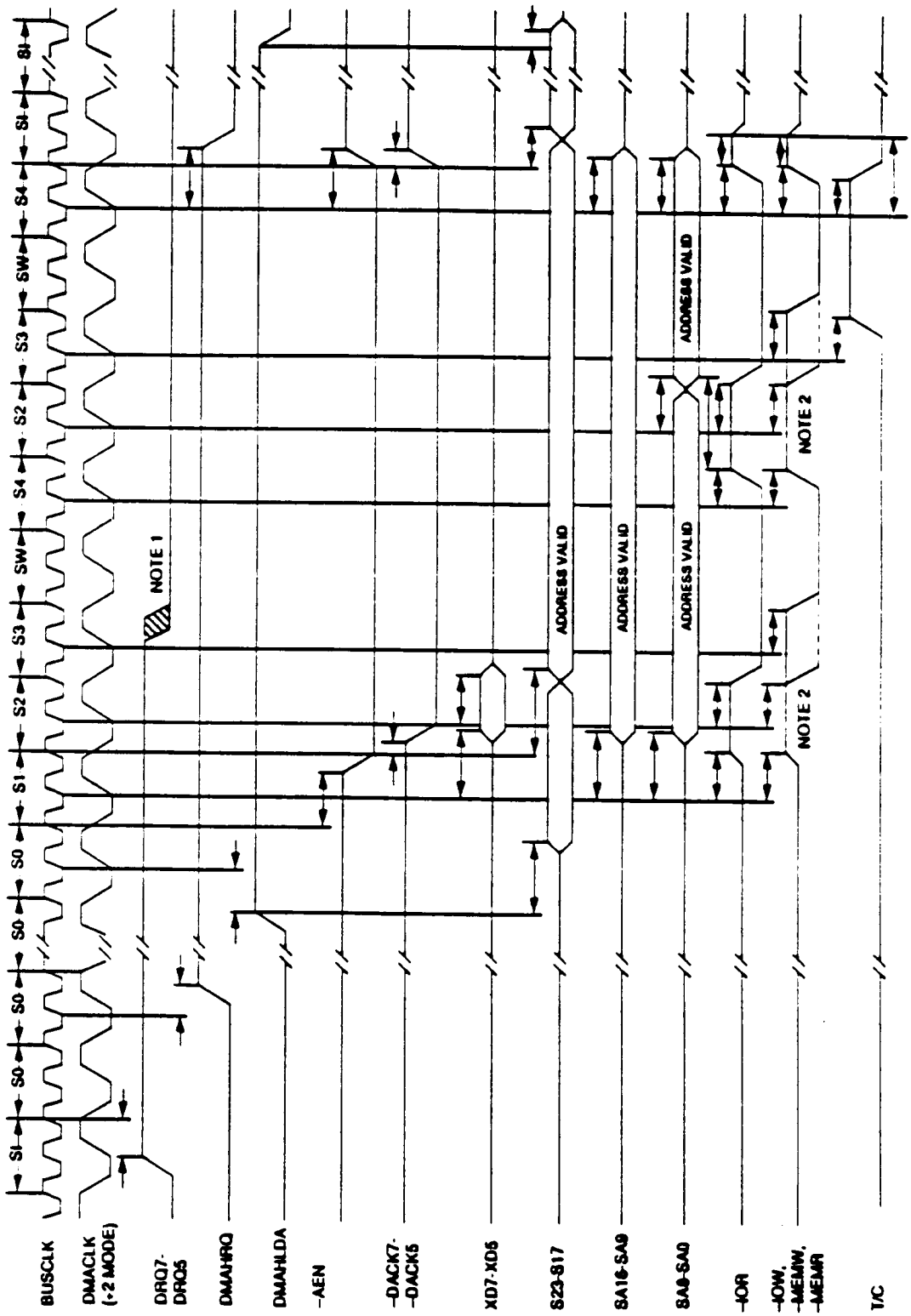
Master Mode

IOCHRDY

Timer/Counter

Bus Conversion: The Bus Controller, via its control of the Data Buffer, performs a large number of data conversions for both memory and I/O cycles. Waveforms for most, but not all, are shown.

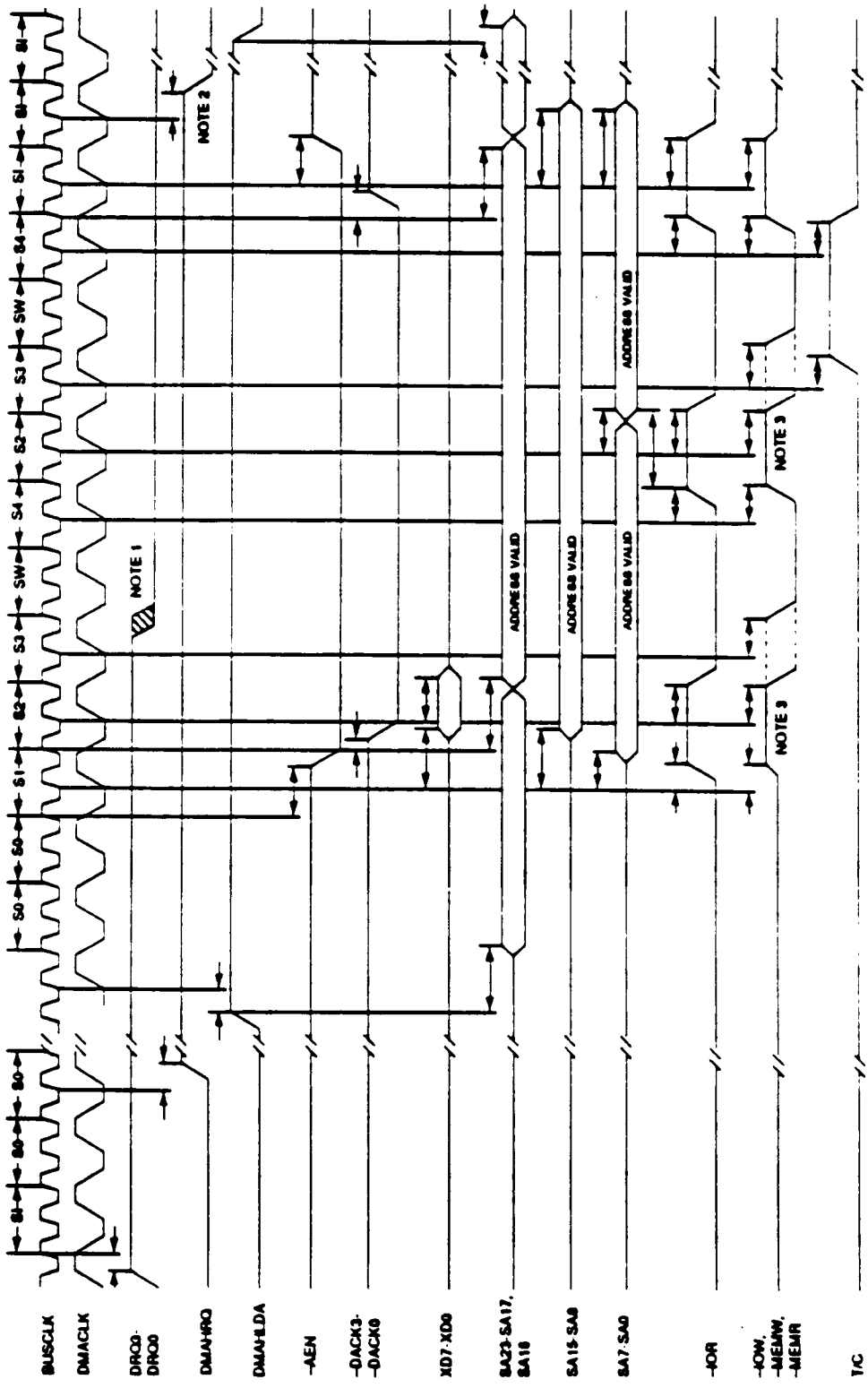
FIGURE 5. 16-BIT DMA TIMING



Notes: 1. DRQ should be held active until –DACK is returned.

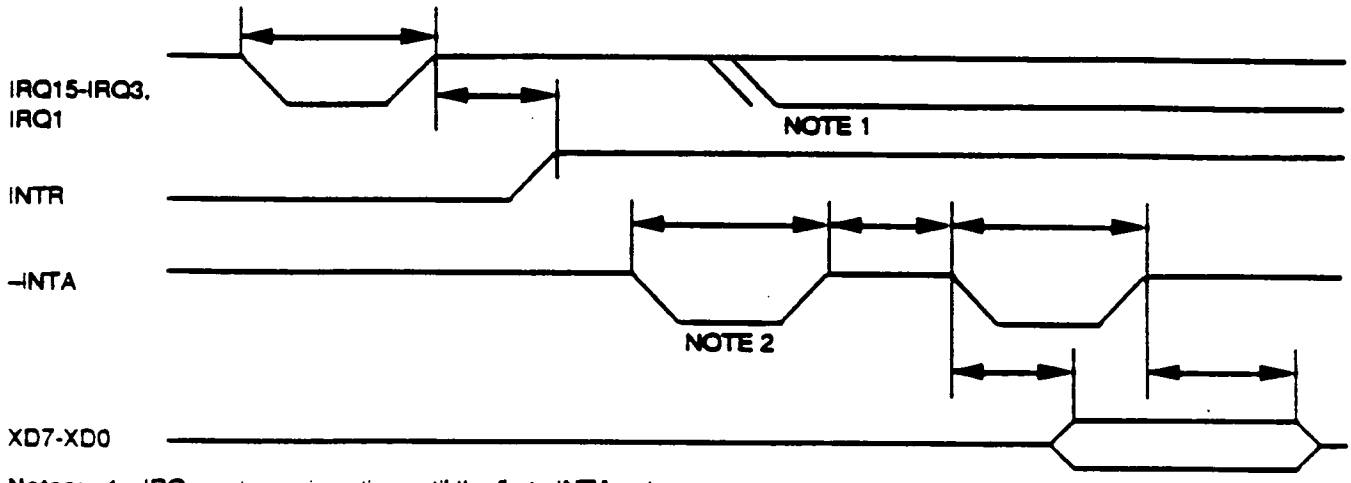
2. The first high to low transistion shown here is extended for –XIOW and –XMEMW. The second high to low transition shown is for –XMEMR and late write on –XIOW and –XMEMW.

FIGURE 6. 8-BIT DMA TIMING



Notes:
1. DRQ should be held active until –DACK is returned.
2. The falling edge of CPUHRQ could occur one clock cycle earlier or later depending on how may bytes are transferred.
3. The first high to low transition shown here is extended for –XIOW and –XMEMW. The second high to low transition shown if for –XMEMR and late write on –XIOW and –XMEMW.

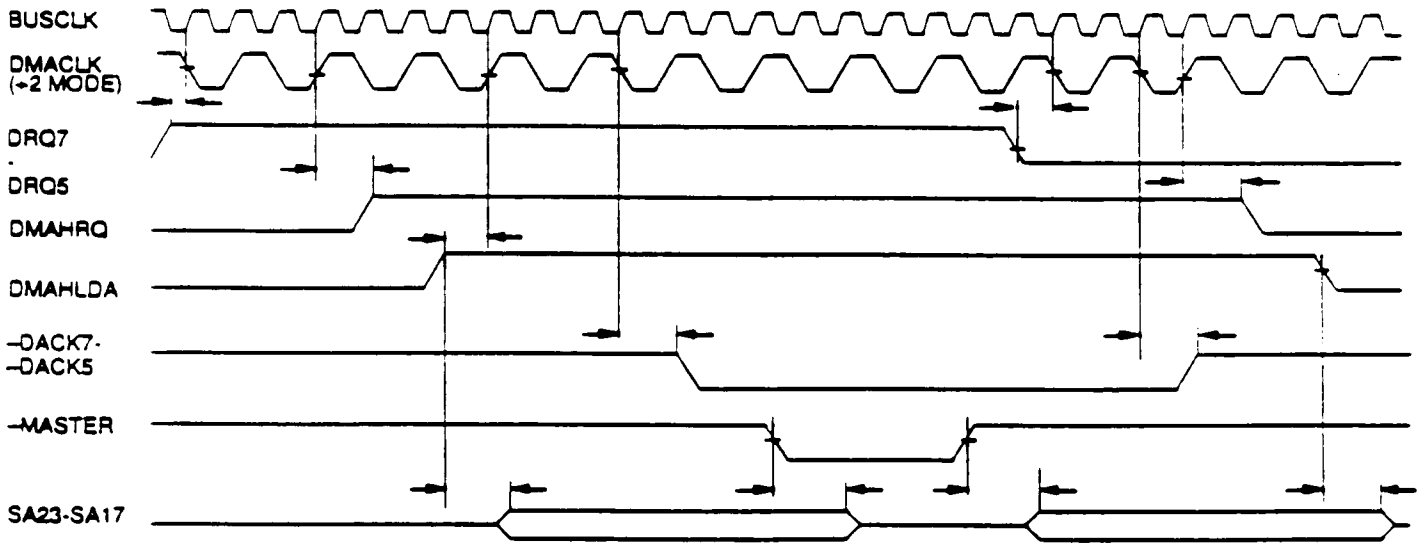
FIGURE 7. INTERRUPT TIMING



Notes: 1. IRQ must remain active until the first –INTA pulse.

2. Cascade priority is resolved on this –INTA cycle.

FIGURE 8. MASTER MODE TIMING



Notes: 1. The DMA channel used for requesting control of the bus by a new bus master must be programmed in cascade mode. The new master should not pull –MASTER low until it has received the corresponding –DACK signal.

2. A 16-bit DMA channel must be used for master cycle operation. 8-bit bus masters are not supported.

FIGURE 9. IOCHRDY TIMING

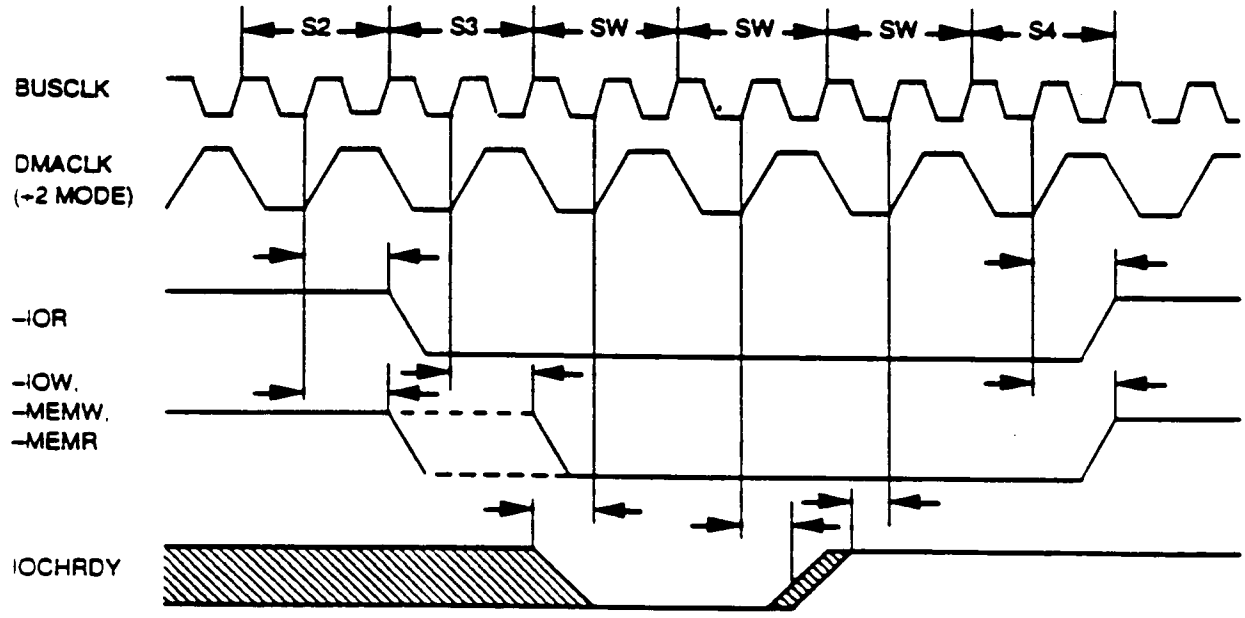


FIGURE 10. TIMER/COUNTER TIMING

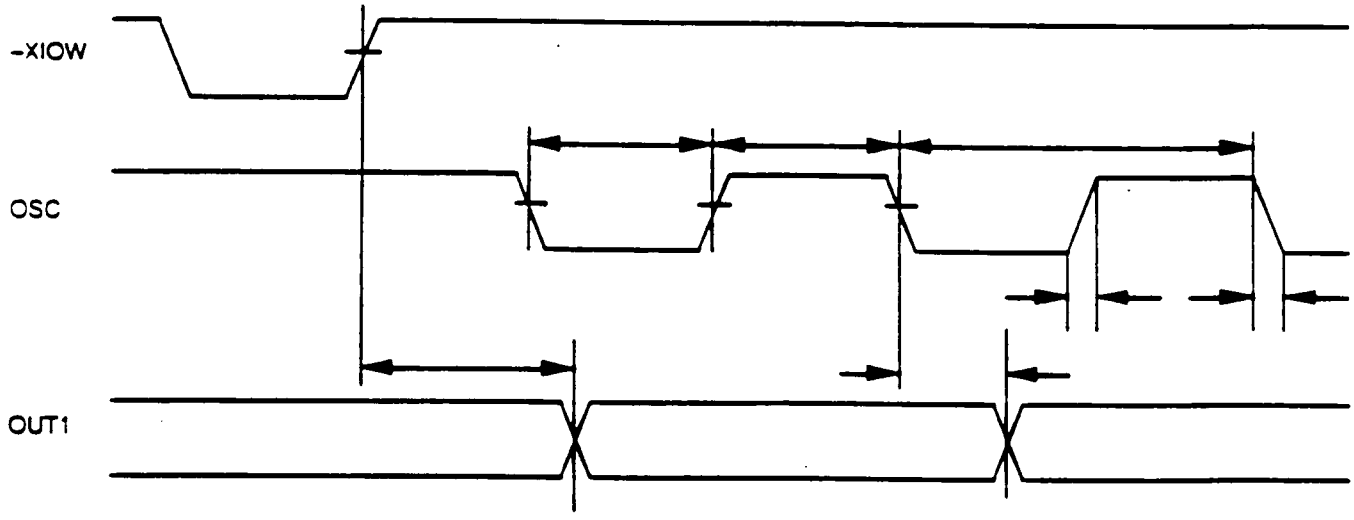


FIGURE 11. 16 TO 8 CONVERSION - I/O READS

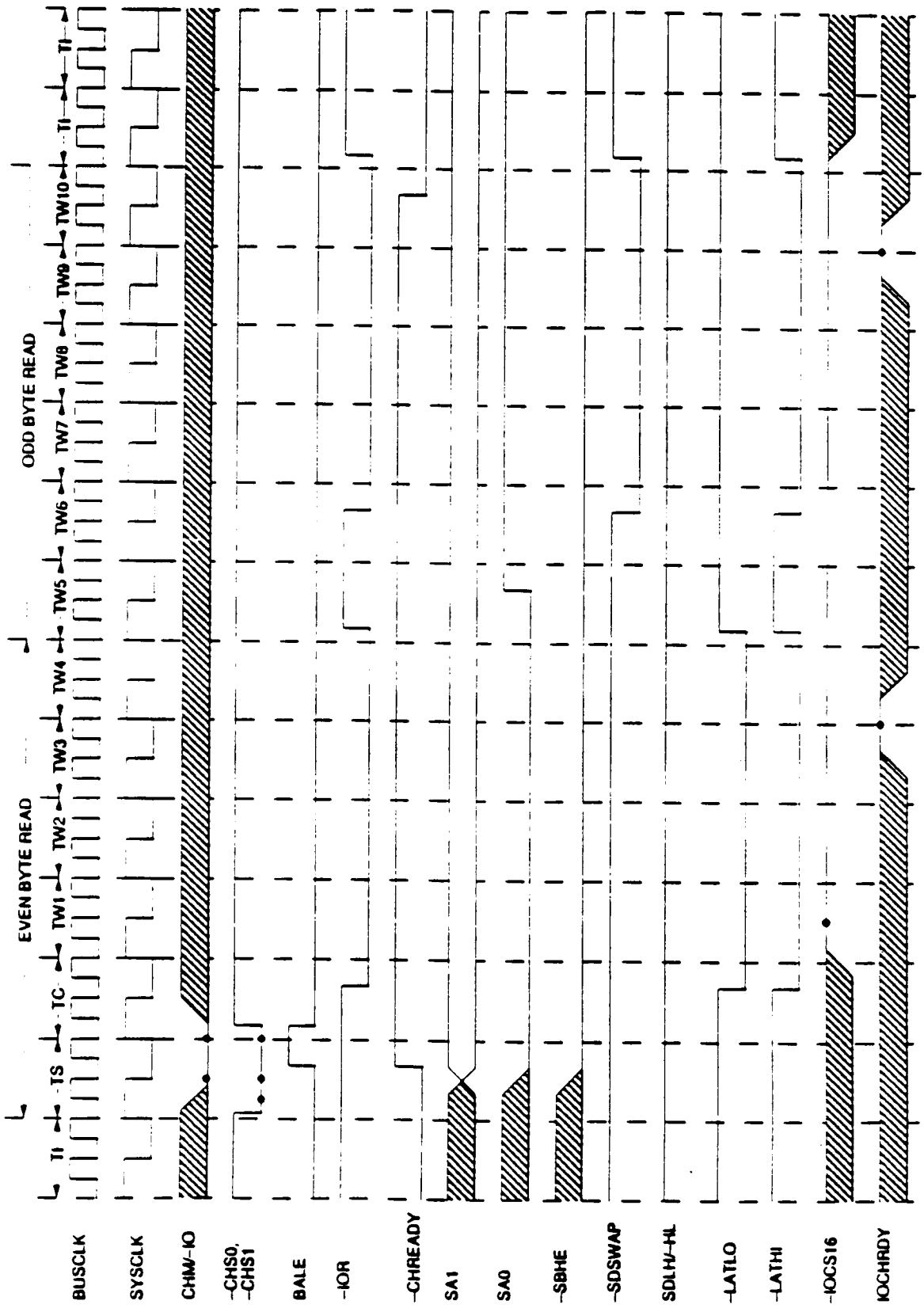


FIGURE 12. 16 TO 8 CONVERSION - I/O WRITES

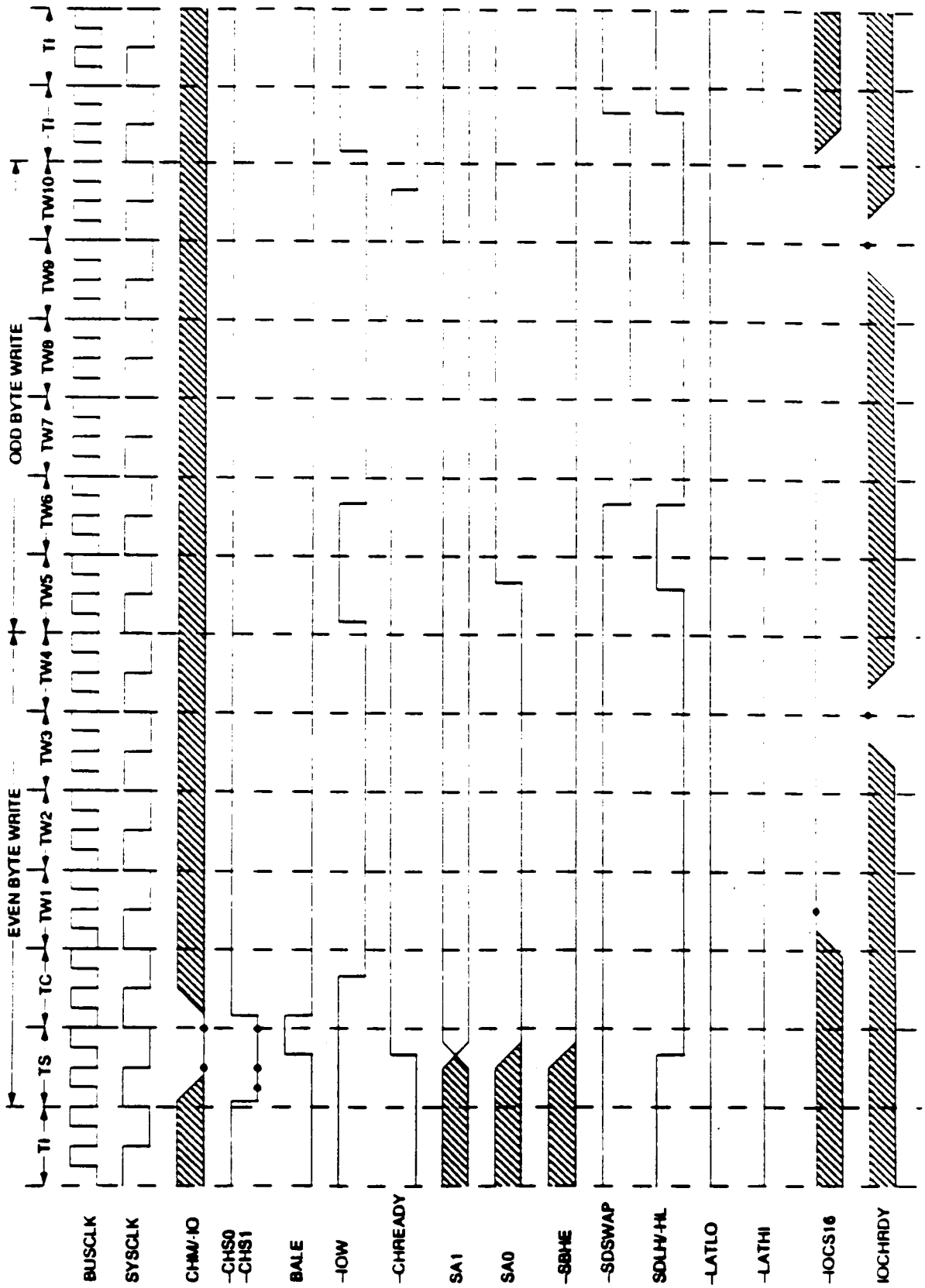


FIGURE 13. 16 TO 8 CONVERSION - MEMORY READS

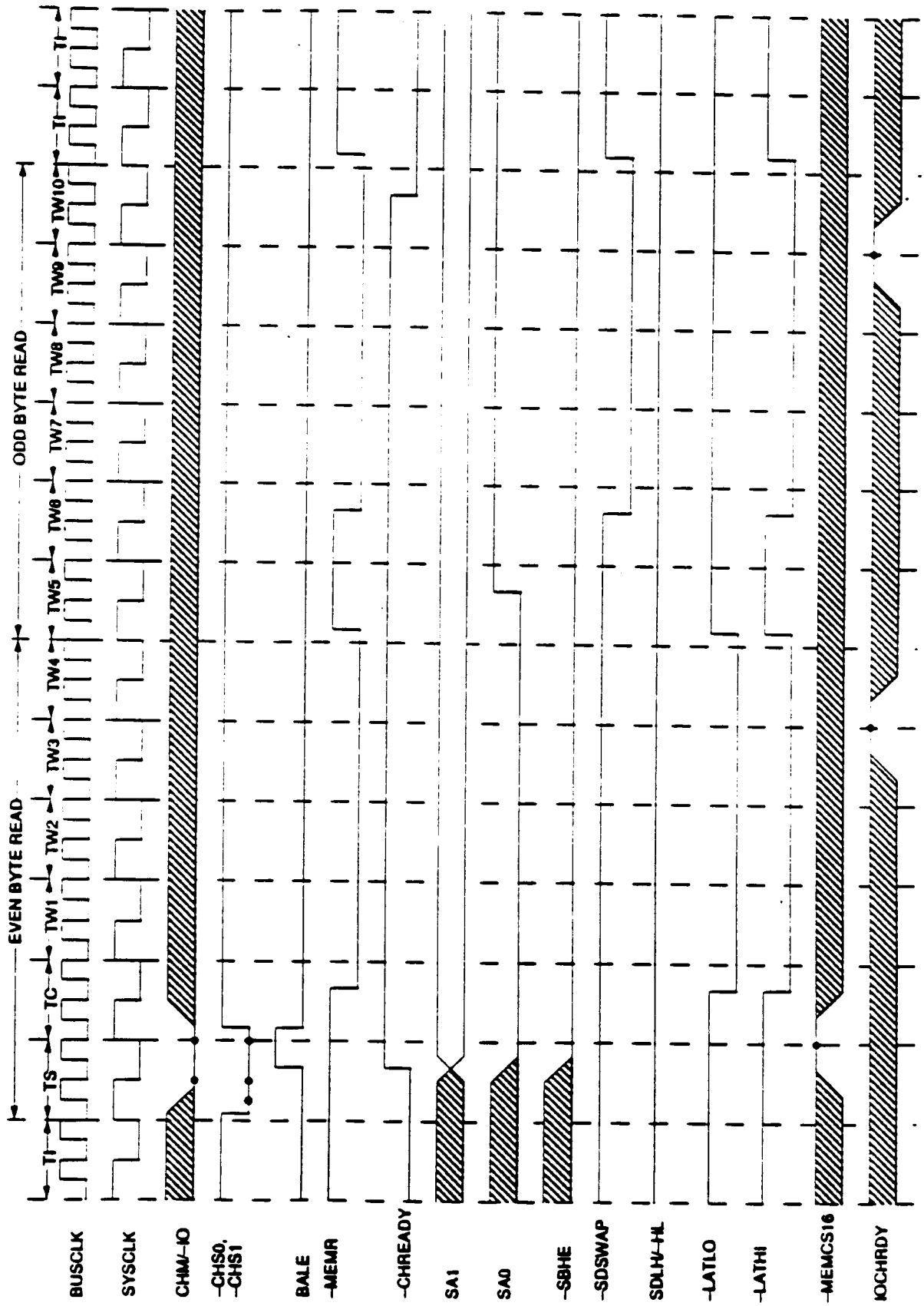


FIGURE 14. 16 TO 8 CONVERSION - MEMORY WRITES

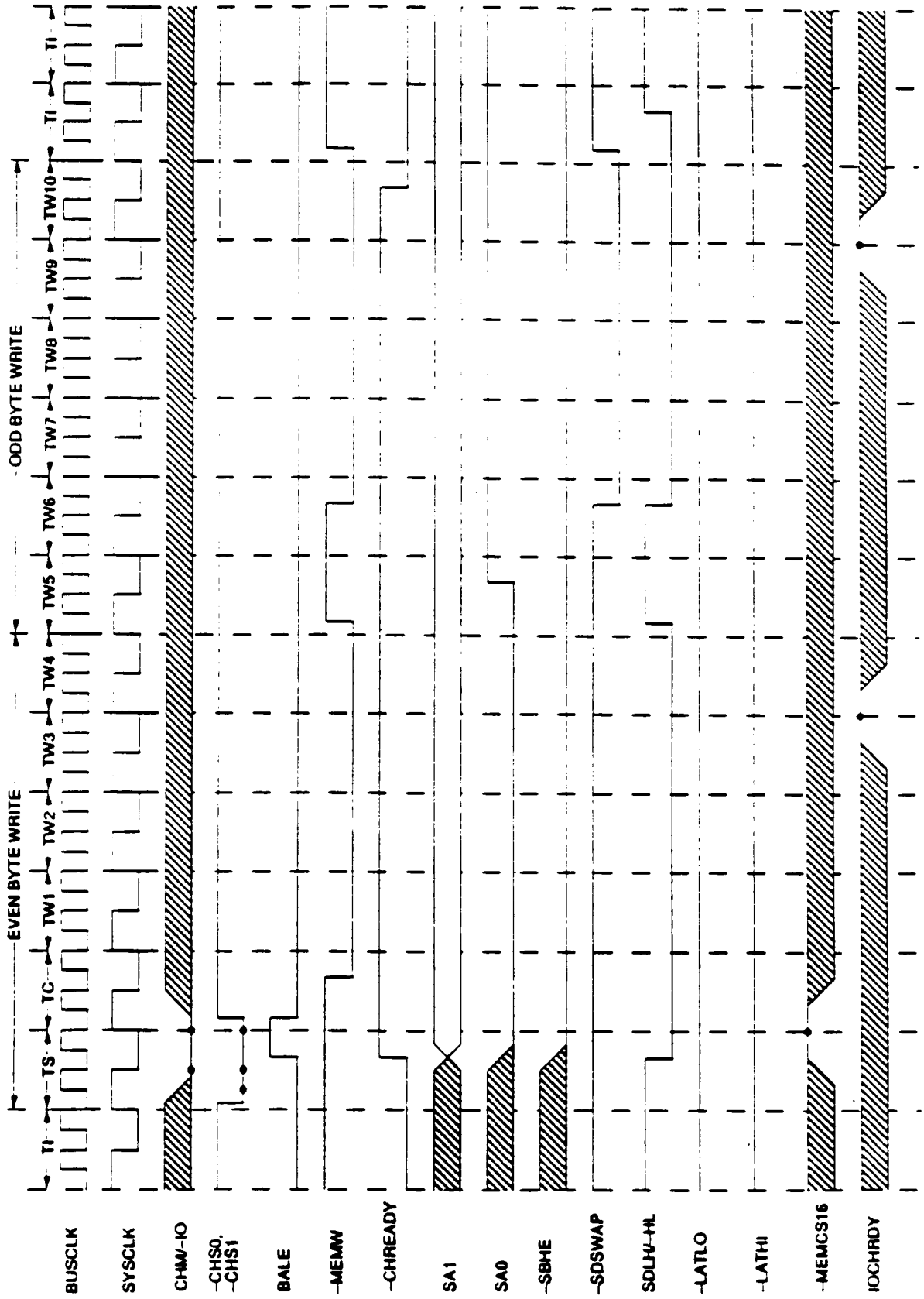


FIGURE 15. 24 TO 8 CONVERSION - I/O READ

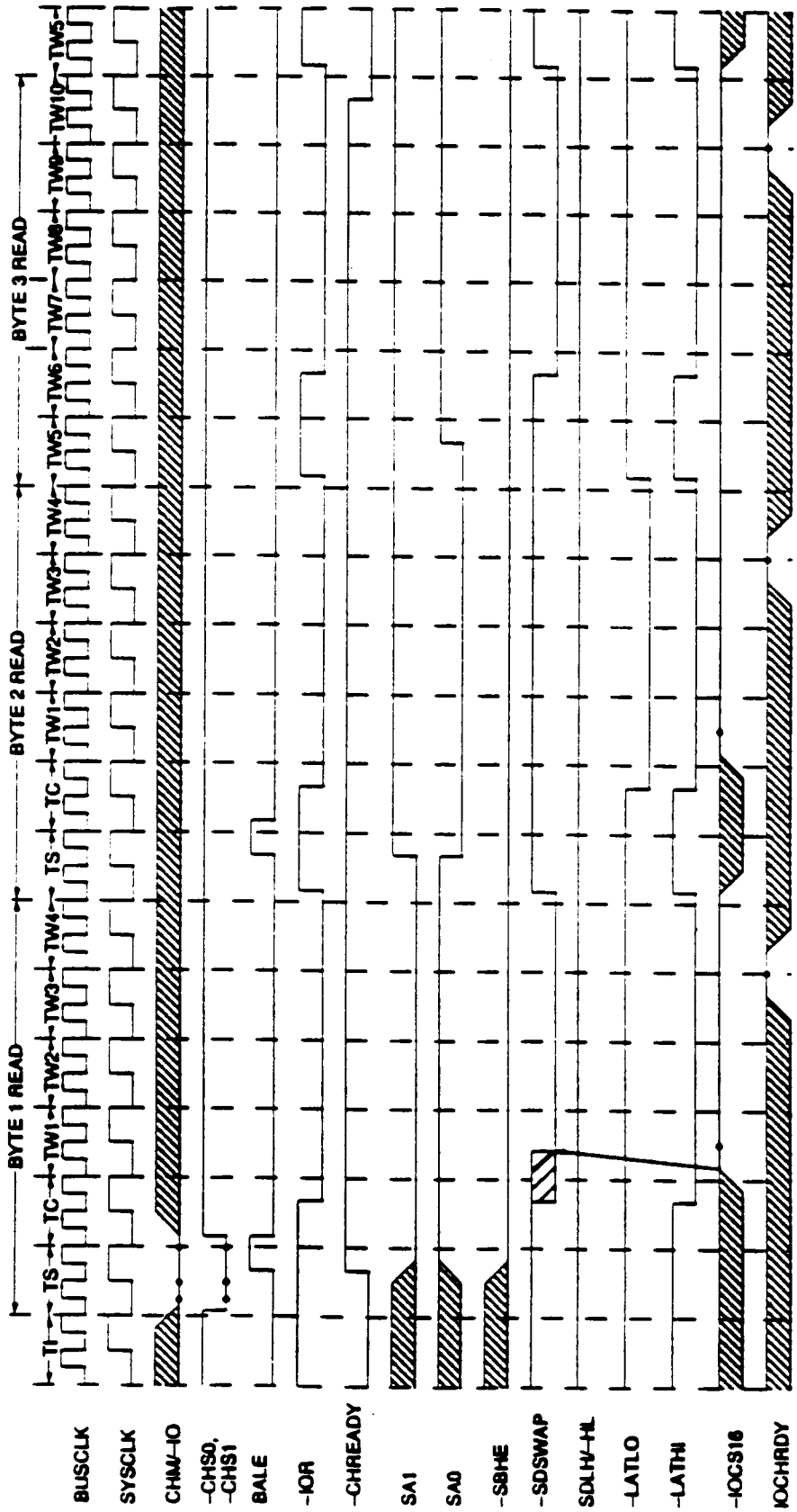


FIGURE 16. 24 TO 8 CONVERSION - I/O WRITE

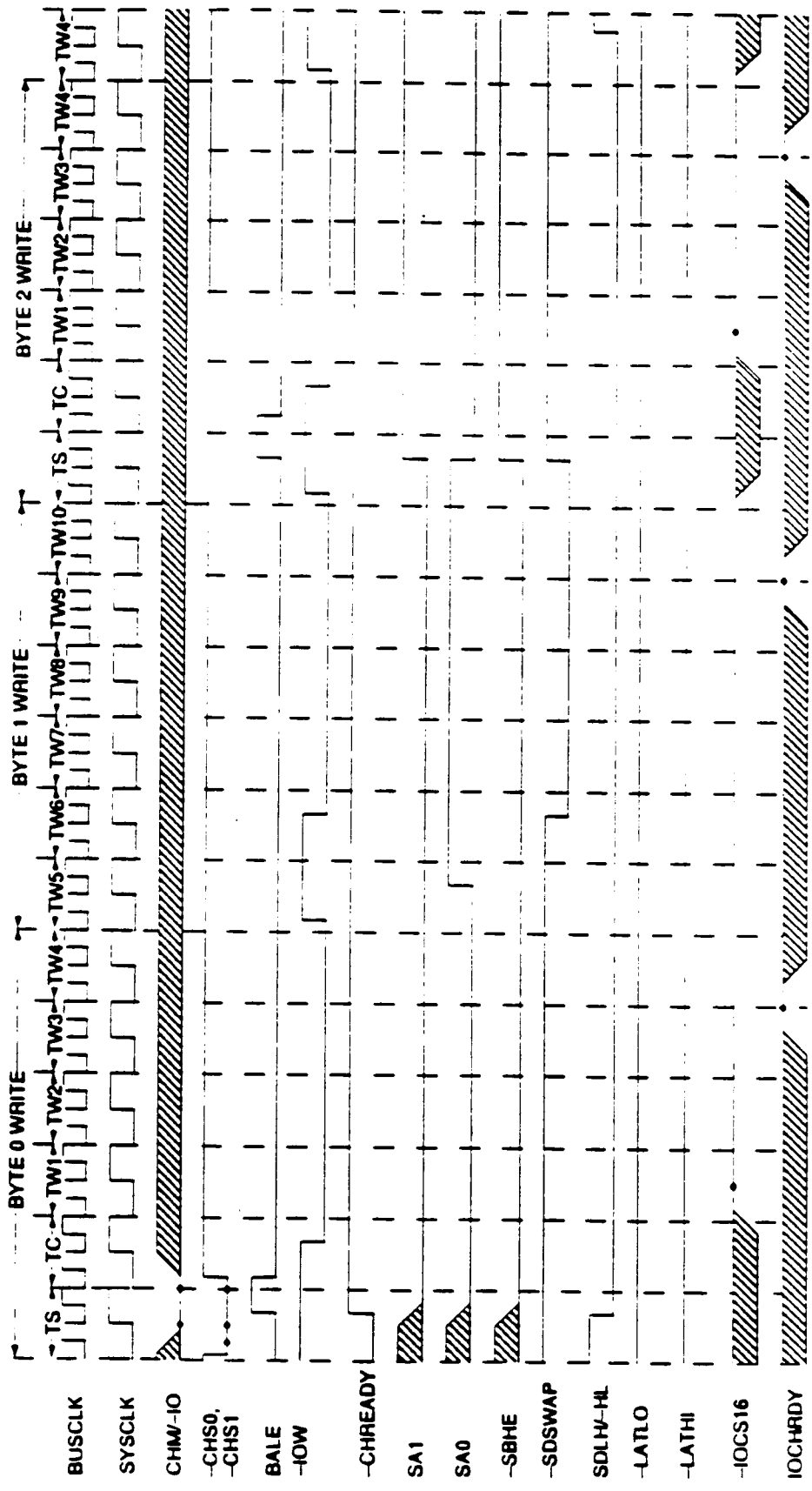


FIGURE 17. 32 TO 8 CONVERSION - MEMORY READ

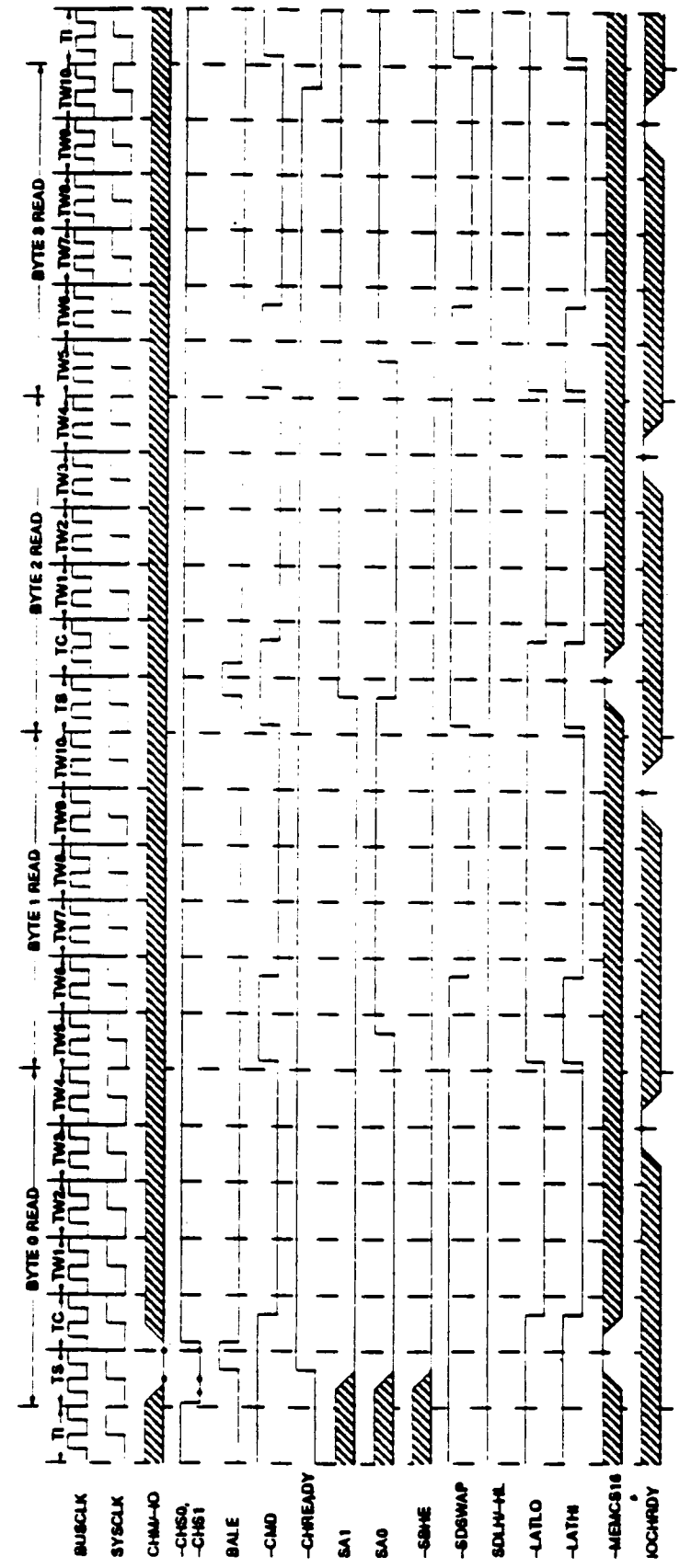


FIGURE 18. 32 TO 8 CONVERSION - MEMORY WRITE

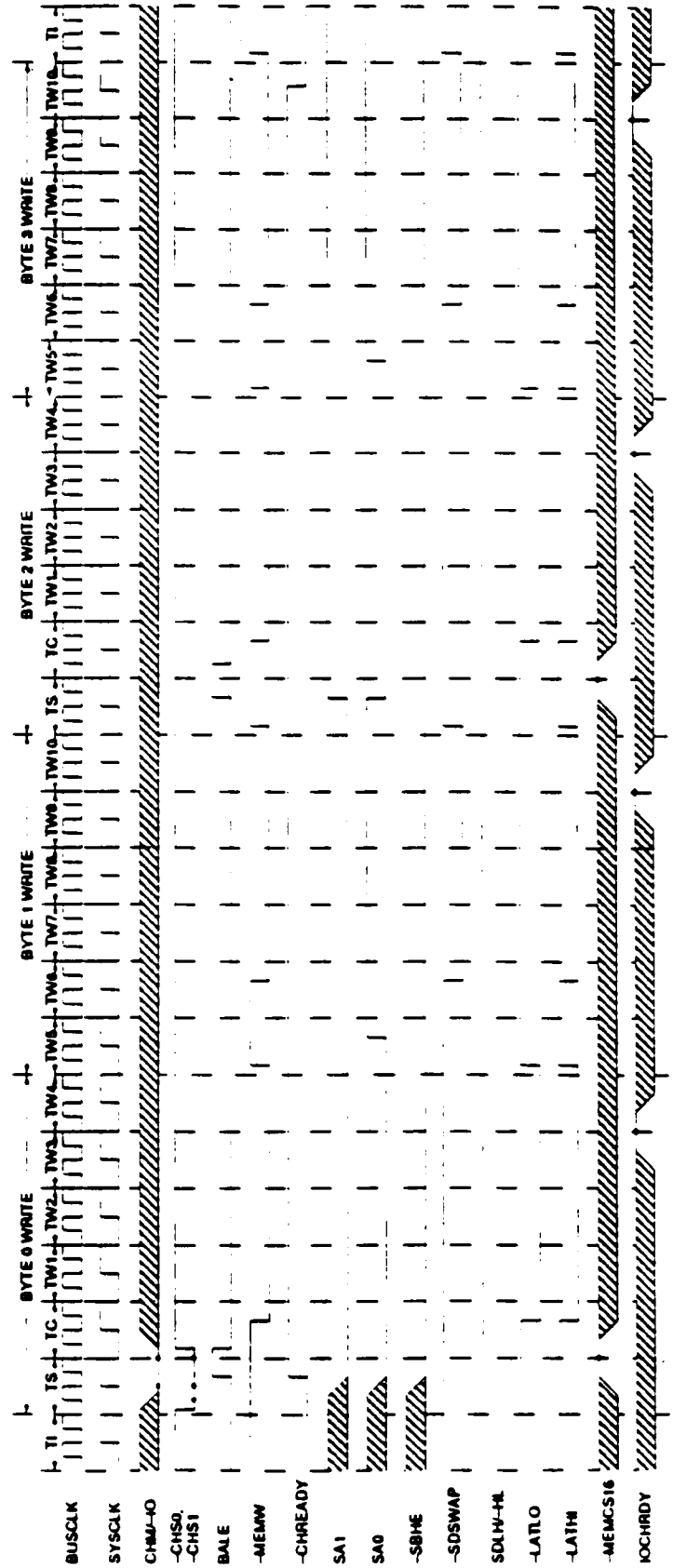


FIGURE 19. 24 TO 16 CONVERSION - MEMORY READS

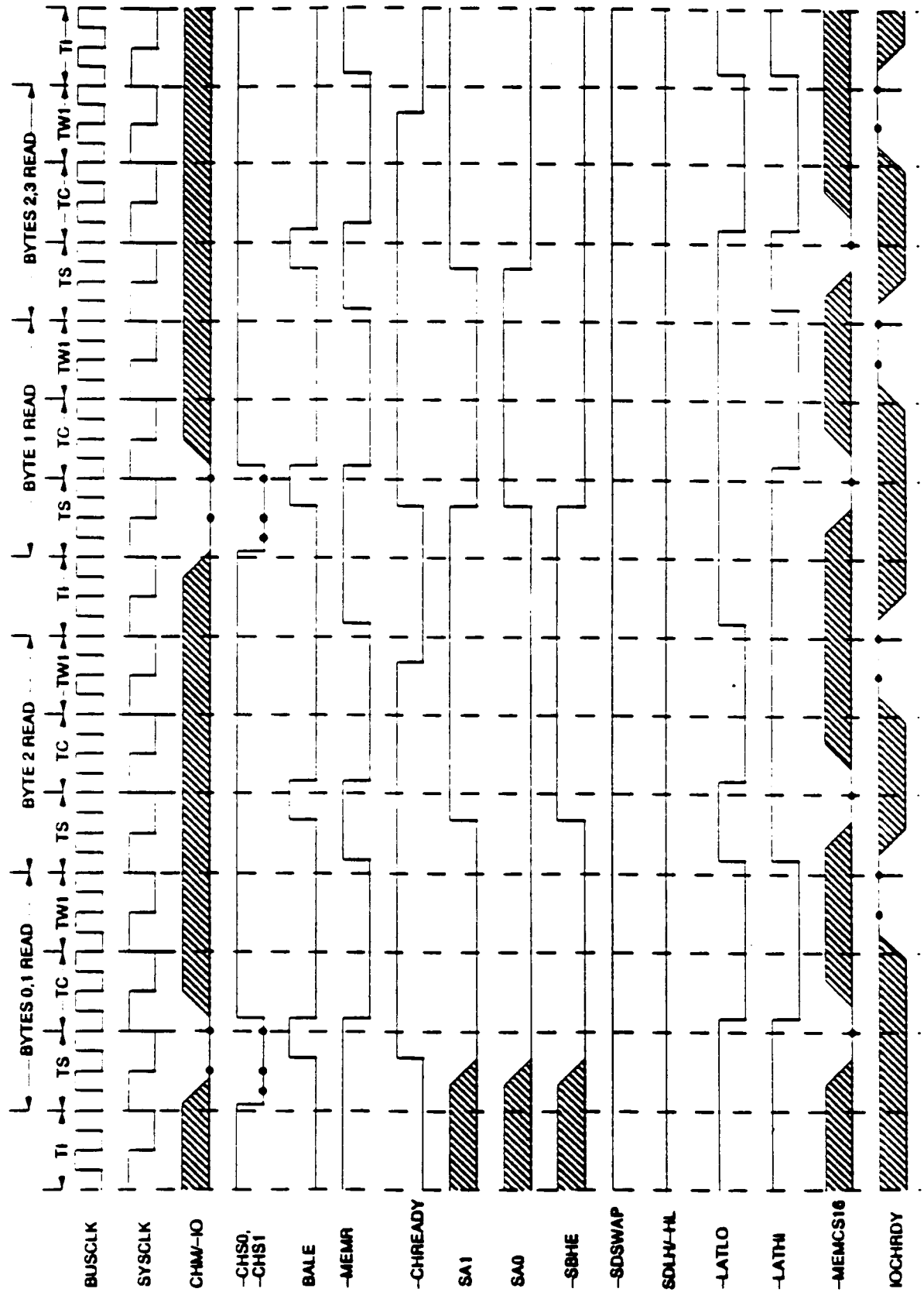


FIGURE 20. 24 TO 16 CONVERSION - MEMORY WRITES

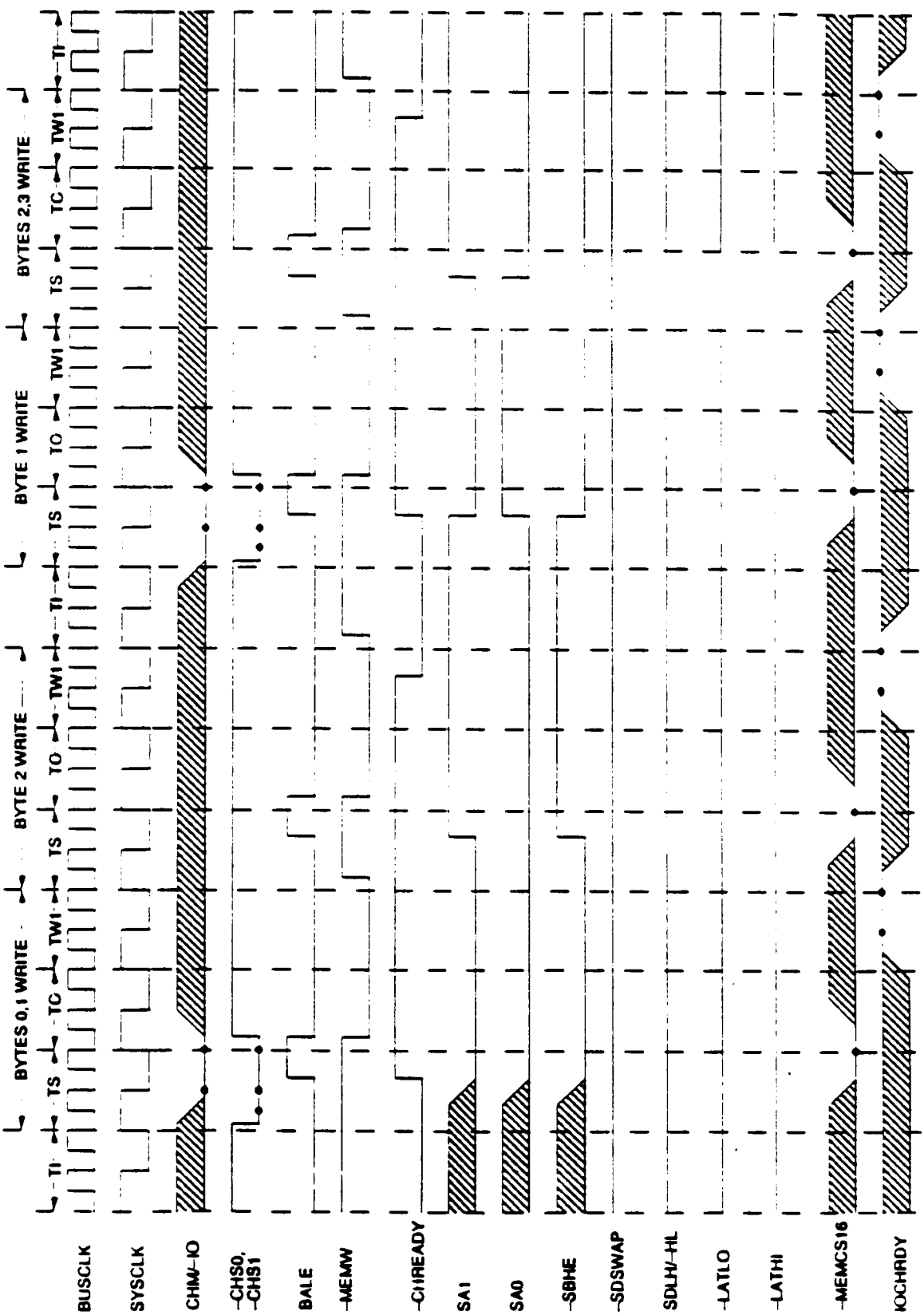


FIGURE 21. 32 TO 16 CONVERSION - MEMORY READS

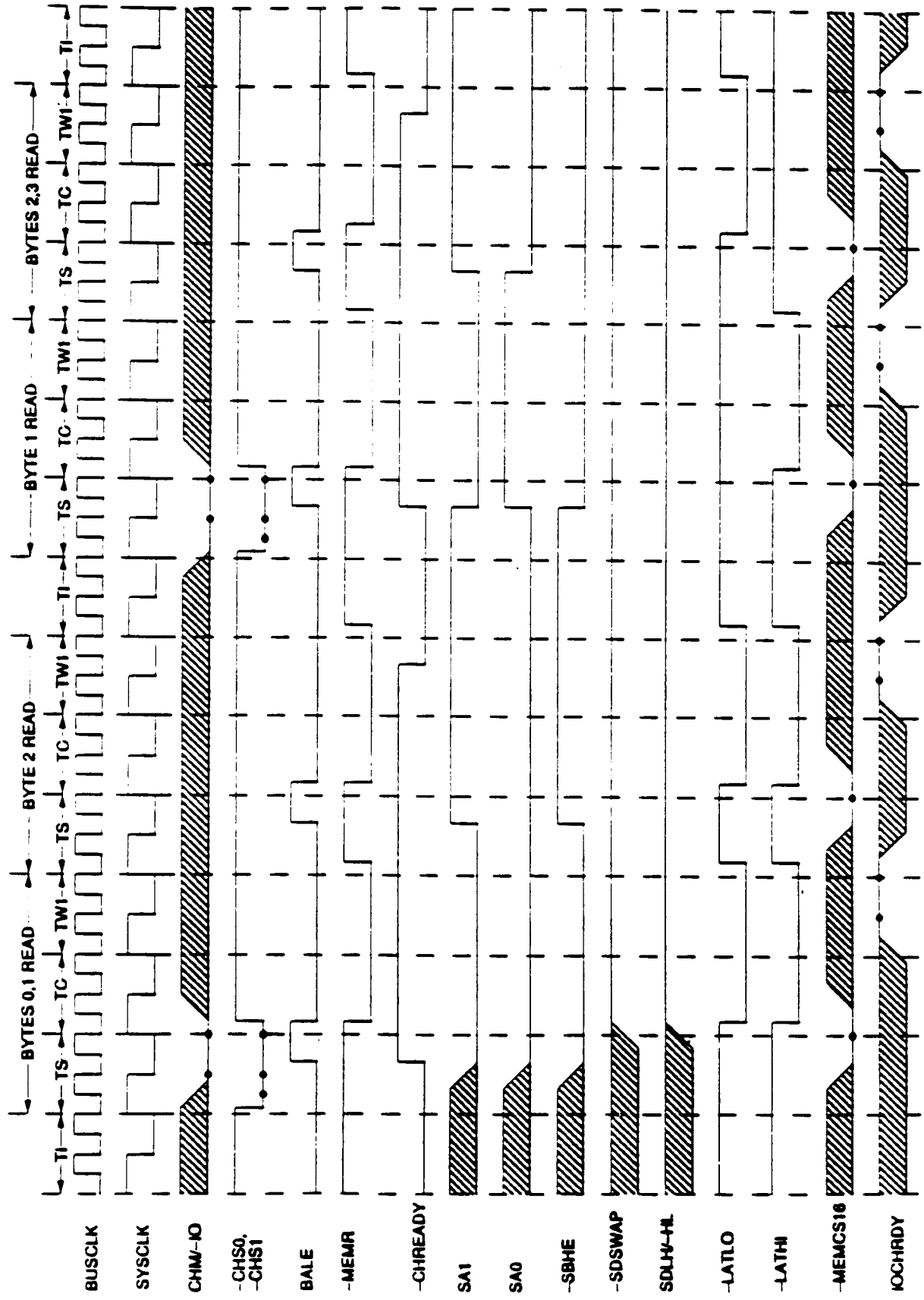


FIGURE 22. 32 TO 16 CONVERSION - MEMORY WRITES

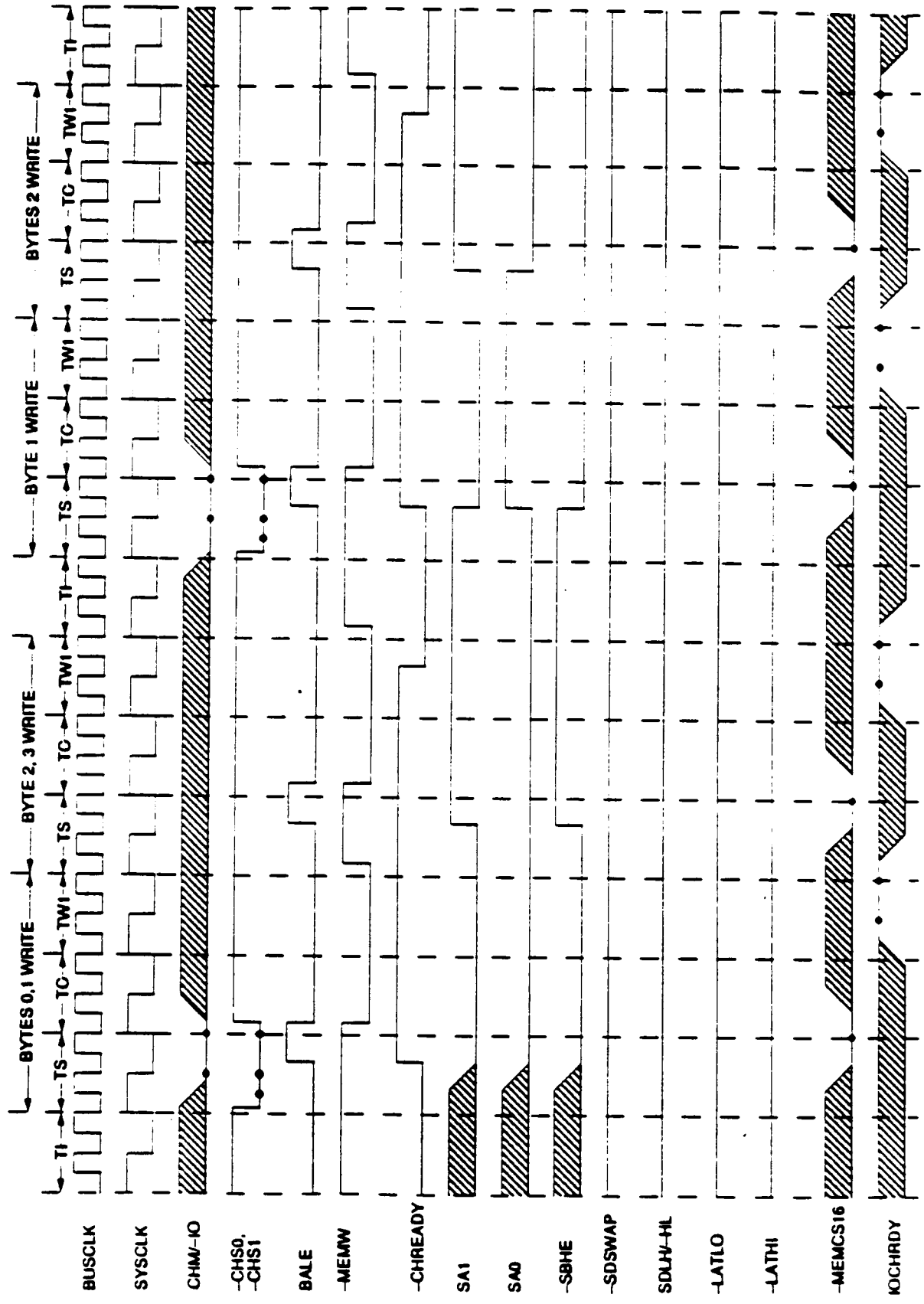


FIGURE 23. 32 TO 16 CONVERSION - I/O READS

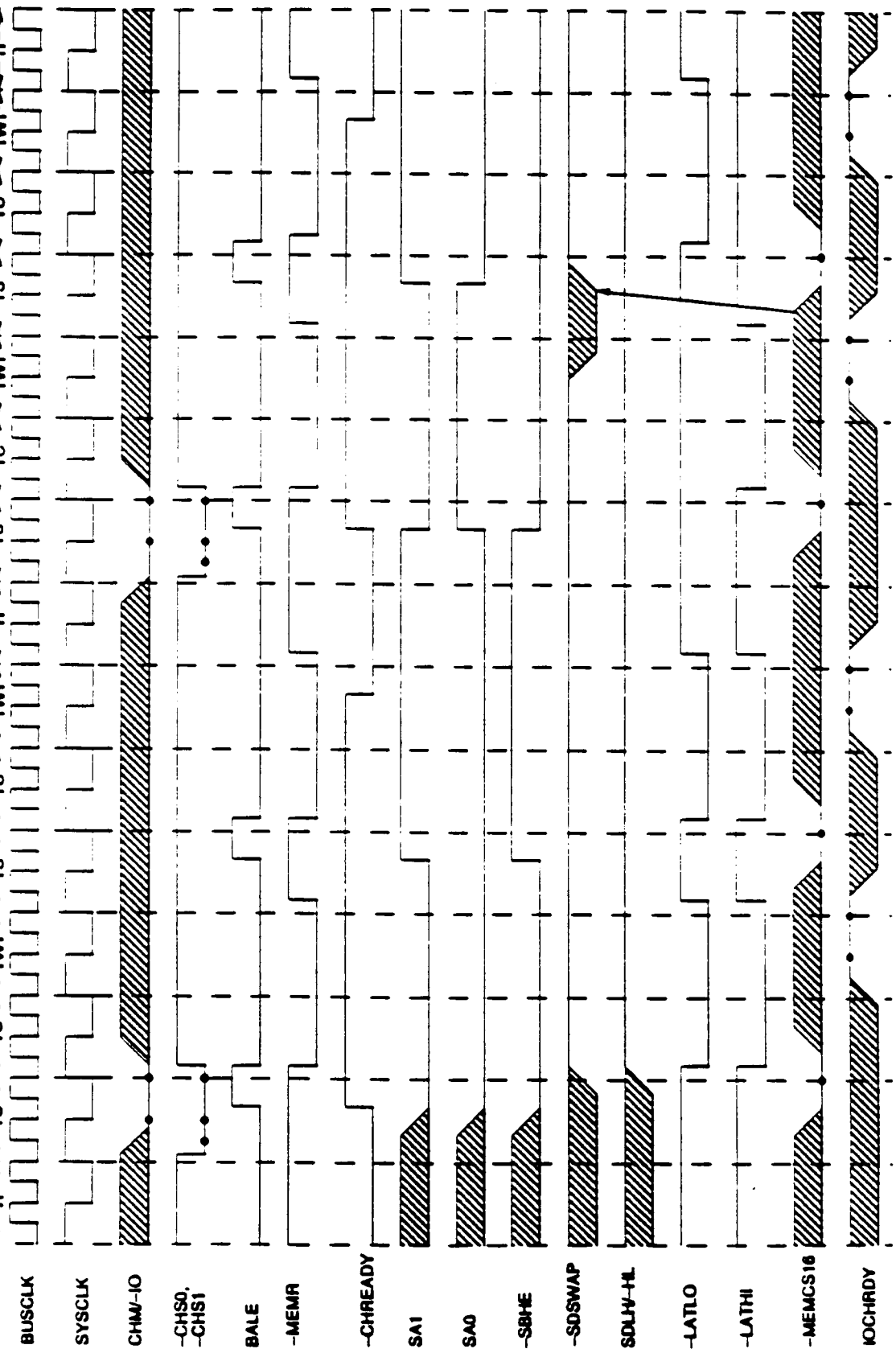
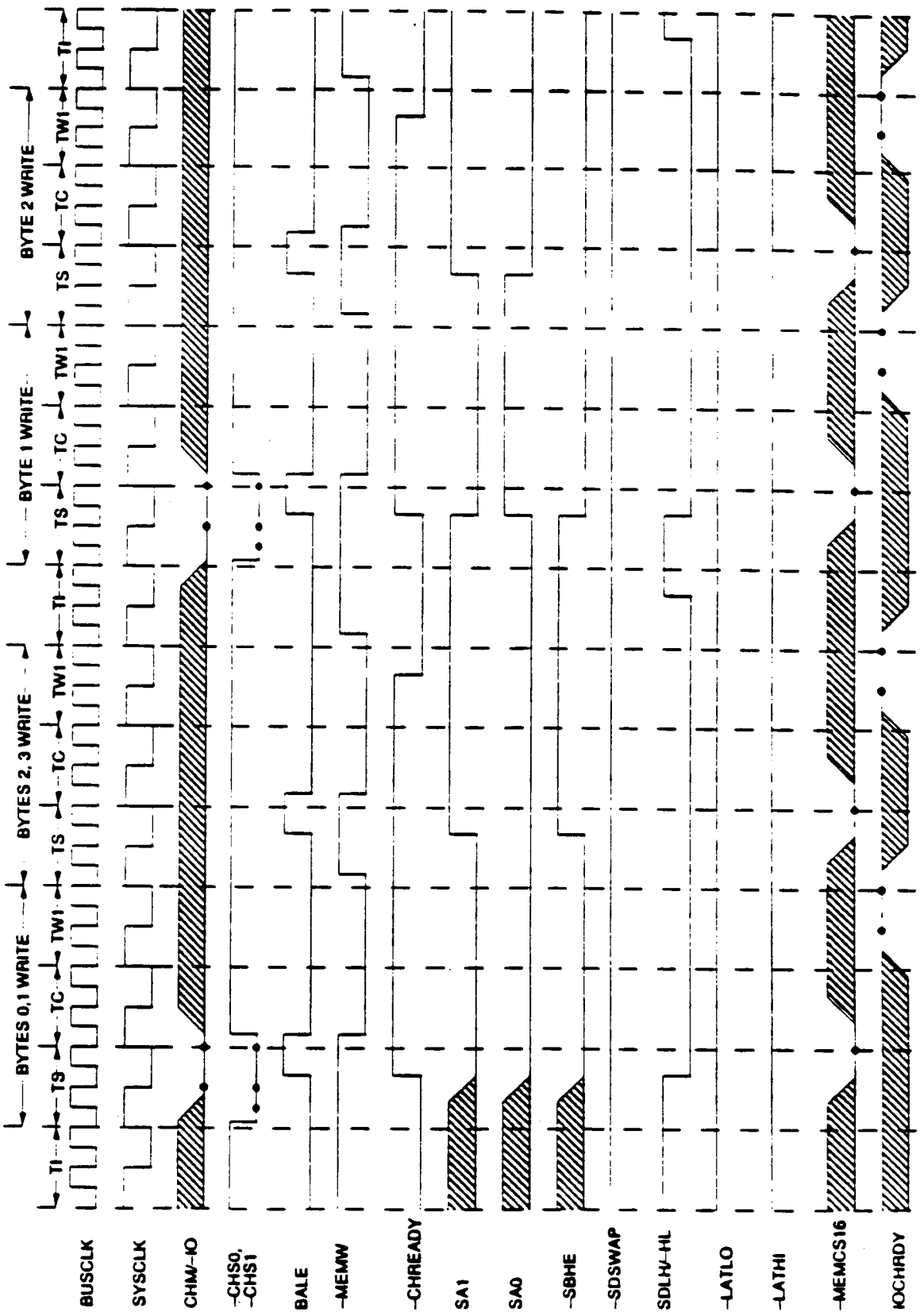


FIGURE 24. 32 TO 16 CONVERSION - I/O WRITES



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground	−0.5 V to VDD + 0.3 V
Applied Output Voltage	−0.5 V to VDD + 0.3 V
Applied Input Voltage	−0.5 V to 7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C TO +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min.	Max.	Unit	Conditions
VILX	Clock Input Low	−0.5	0.8	V	
VIHX	Clock Input High	2.0	VDD	V	
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD	V	
VOL	Output Low Voltage		0.4	V	2 mA
			0.4	V	12 mA
VOH	Output High Voltage	2.4		V	2 mA
		2.4		V	12 mA
VILR	Reset VIL (Schmitt-trigger)		0.8	V	
VOLR	Reset VIH (Schmitt-trigger)	2.0		V	
IDD	Supply Current		50	mA	VDD = 5.25 V
IDD	Dynamic Current		2.5	mA/MHz	VDD = 5.25 V
IIL	Input Leakage		±10	µA	VDD = 5.25 V, VSS = 0 V
ICL	Clock Leakage		±10	µA	VDD = 5.25 V, VSS = 0 V
IOZ	Three-state Leakage		±20	µA	VDD = 5.25 V, VSS = 0 V