# HS-C²MOS™ INTEGRATED CIRCUITS

041948

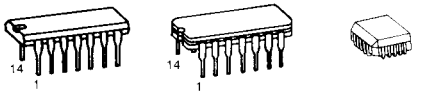
**M54HC113**
**M74HC113**

**PRELIMINARY DATA**

## DUAL J-K FLIP FLOP WITH PRESET

### DESCRIPTION

The M54/74HC113 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This circuit offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



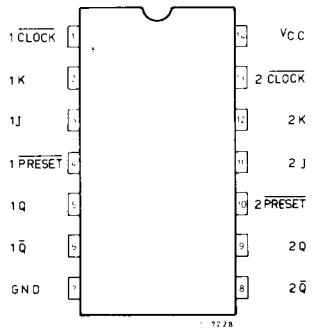

**B1** Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HC113 F1
M74HC113 B1
M74HC113 F1
M74HC113 C1

### FEATURES

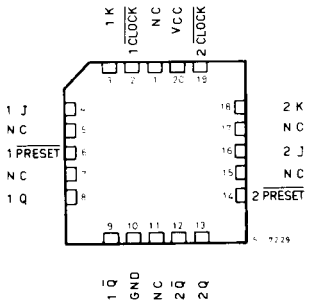
- High Speed
  $f_{MAX}$ = 71 MHz (Typ.) $V_{CC}$ = 5V
- Low Power Dissipation
  $I_{CC}$ = 2 $\mu$A (Max.) at $T_A$ = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  $V_{CC}$ (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS113

### PIN CONNECTIONS
(top view)




Dual in line

### CHIP CARRIER



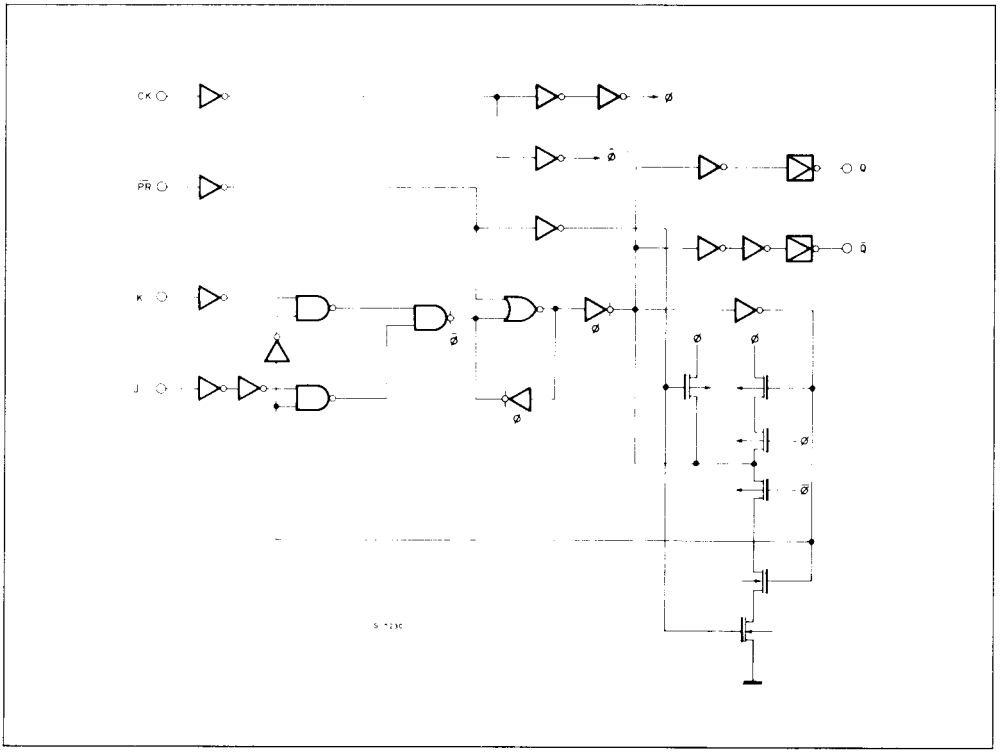

NC = No Internal Connection

### TRUTH TABLE

| INPUTS | | | | OUTPUT | |
|---|---|---|---|---|---|
| PRESET | CLOCK | J | K | Q | Q |
| L | * | * | * | H | L |
| H | ↓ | L | L | No Change | |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | Toggle | |
| H | ↑ | * | * | No Change | |

↑: Transition from Low to High Level ↓: High to Low
*: Don't care

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | − 0.5 to 7 | V |
| $V_I$ | DC Input Voltage | − 0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Source Sink Current Per Output Pin | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | − 65 to 150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limit | | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 to 6 | | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | | V |
| $T_A$ | Operating Temperature 74HC Series<br>54HC Series | − 40 to 85<br>−55 to 125 | | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ 2 V | 0 to 1000 | ns |
| | | $V_{CC}$ 4.5V | 0 to 500 | |
| | | $V_{CC}$ 6 V | 0 to 400 | |

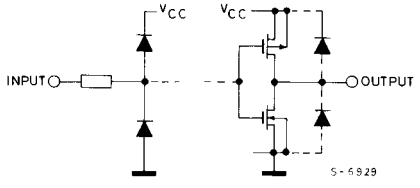
## DC SPECIFICATIONS

| Symbol | Parameter | $V_{CC}$ | Test Condition | | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_I$ | $I_O$ | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | | 1.5 | — | — | 1.5 | — | 1.5 | — | V |
| | | 4.5 | | | 3.15 | — | — | 3.15 | — | 3.15 | — | |
| | | 6.0 | | | 4.2 | — | — | 4.2 | — | 4.2 | — | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | — | — | 0.5 | — | 0.5 | — | 0.5 | V |
| | | 4.5 | | | — | — | 1.35 | — | 1.35 | — | 1.35 | |
| | | 6.0 | | | — | — | 1.8 | — | 1.8 | — | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $V_{IH}$ or $V_{IL}$ | −20 μA | 1.9 | 2.0 | — | 1.9 | — | 1.9 | — | V |
| | | 4.5 | | | 4.4 | 4.5 | — | 4.4 | — | 4.4 | — | |
| | | 6.0 | | | 5.9 | 6.0 | — | 5.9 | — | 5.9 | — | |
| | | 4.5 | | −4.0 mA | 4.18 | 4.31 | — | 4.13 | — | 4.10 | — | |
| | | 6.0 | | −5.2 mA | 5.68 | 5.8 | — | 5.63 | — | 5.60 | — | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $V_{IH}$ or $V_{IL}$ | 20 μA | — | 0 | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 4.5 | | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 6.0 | | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 4.5 | | 4.0 mA | — | 0.17 | 0.26 | — | 0.33 | — | 0.40 | |
| | | 6.0 | | 5.2 mA | — | 0.18 | 0.26 | — | 0.33 | — | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | — | — | ±0.1 | — | ±1 | | ±1 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | — | — | 2 | — | 20 | | 40 | μA |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15pF, Input $t_r = t_f$ = 6ns)

| Symbol | Parameter | 54HC and 74HC | | | Unit |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | | 4 | 8 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{CLOCK}$-Q,Q) | | 14 | 23 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time ($\overline{PRESET}$-Q,Q) | | 17 | 27 | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 40 | 71 | | MHz |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width ($\overline{CLOCK}$) | | 8 | 15 | ns |
| $t_{W(L)}$ | Minimum Pulse Width ($\overline{PRESET}$) | | 8 | 15 | ns |
| $t_s$ | Minimum Set-up Time (J,K) | | 5 | 10 | ns |
| $t_h$ | Minimum Hold Time (J,K) | | — | 0 | ns |
| $t_{REM}$ | Minimum Removal Time ($\overline{PRESET}$) | | — | 0 | ns |

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | — | 22 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | | | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | | |
| $t_{PLH}$ $t_{PHL}$ | Progataion Delay Time ($\overline{CK}$-Q,$\overline{Q}$) | 2.0 | | — | 55 | 135 | — | 165 | | | ns |
| | | 4.5 | | — | 17 | 27 | — | 33 | | | |
| | | 6.0 | | — | 15 | 23 | — | 28 | | | |
| $t_{PLH}$ $t_{PHL}$ | Progataion Delay Time ($\overline{PRESET}$- Q, $\overline{Q}$) | 2.0 | | — | 72 | 160 | — | 195 | | | ns |
| | | 4.5 | | — | 20 | 32 | — | 39 | | | |
| | | 6.0 | | — | 17 | 28 | — | 34 | | | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | | 7 | 16 | — | 5 | — | | | MHz |
| | | 4.5 | | 35 | 58 | — | 29 | — | | | |
| | | 6.0 | | 41 | 68 | — | 34 | — | | | |
| $t_{W(H)}$ $t_{W(L)}$ | Minimum Pulse Width ($\overline{CK}$) | 2.0 | | — | 27 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | | | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | | |
| $t_{W(L)}$ | Minimum Pulse Width ($\overline{PRESET}$) | 2.0 | | — | 34 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | | | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | | |
| $t_s$ | Minimum Set-up Time (J,K) | 2.0 | | — | 25 | 50 | — | 60 | | | ns |
| | | 4.5 | | — | 5 | 10 | — | 12 | | | |
| | | 6.0 | | — | 4 | 9 | — | 11 | | | |
| $t_h$ | Minimum Hold Time (J,K) | 2.0 | | — | — | 0 | — | 0 | | | ns |
| | | 4.5 | | — | — | 0 | — | 0 | | | |
| | | 6.0 | | — | — | 0 | — | 0 | | | |
| $t_{REM}$ | Minimum Removal Time ($\overline{PRESET}$) | 2.0 | | — | — | 0 | — | 0 | | | ns |
| | | 4.5 | | — | — | 0 | — | 0 | | | |
| | | 6.0 | | — | — | 0 | — | 0 | | | |
| $C_{IN}$ | Input Capacitance | | | — | 5 | 10 | — | 10 | | | pF |
| $C_{PD}$ (*) | Power Dissipation Capacitance | | | — | 38 | — | — | — | | | pF |

Note (*) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)