RS8228/M28228

Octal ATM Transmission Convergence PHY Device

The RS8228 Octal ATM Transmission Convergence PHY device dramatically improves performance for switch and access system low-speed ports by integrating all the ATM physical layer processing functions found in the ATM Forum Cell Based Transmission Convergence Sublayer specification (af-phy-0043.000) for eight individual ports. Each port can be independently configured for operation at speeds ranging from 64 kbps to 52 Mbps. There is also a powerdown mode option for each TC port. A UTOPIA Level 2 Multi-PHY interface connects the device to the host switch or terminal system and concentrates the ATM cell traffic onto one interface.

Typical system implementations center around the concentration of ATM cells over standard PDH data rates such as T1/E1 lines, DS3/E3 lines, and multiple Digital Subscriber Line (DSL) formats such as HDSL, ADSL or VDSL*. For each format, external devices perform the appropriate Physical Media Dependent (PMD) layer functions and present the RS8228 with a payload bit stream. The RS8228 then performs all cell alignment functions on that bit stream. This gives system designers a simple, modular, and low-cost architecture for supporting all UNI and NNI ATM interfaces below 52 Mbps. Because the RS8228 performs only the cell-based portion of the protocol stack, designers can select the most integrated framer and Line Interface Unit (LIU) available or reuse existing devices and software.

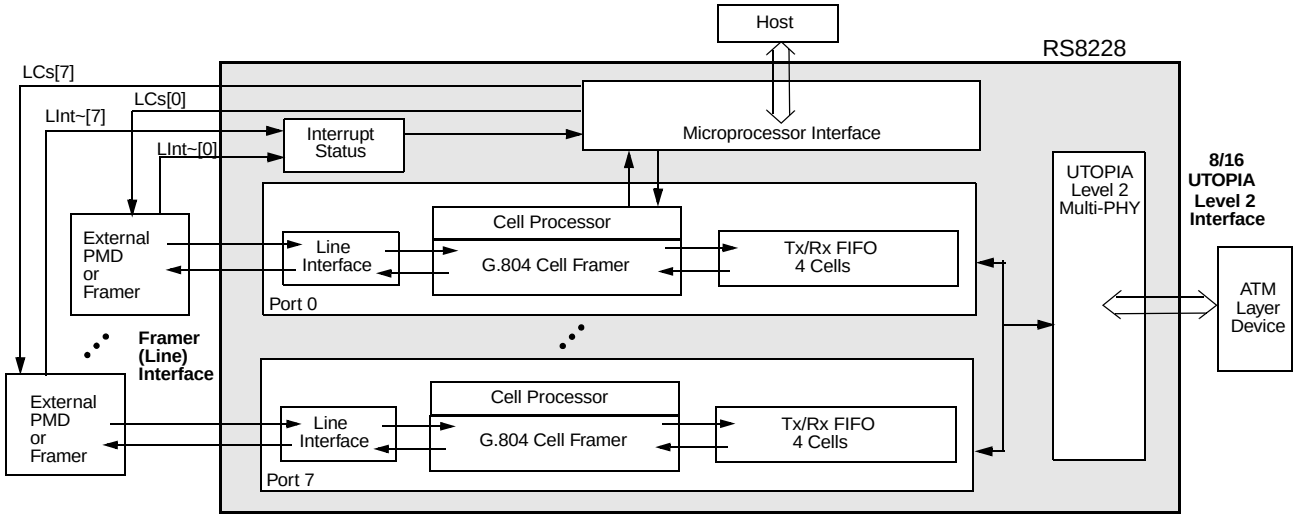
The RS8228 can also be used in combination with a Conexant Segmentation and Reassembly (SAR) device. The RS8228 gluelessly connects to the SAR via the UTOPIA and microprocessor interfaces. The device can be configured and controlled optionally through a generic microprocessor interface. The RS8228's chip-select feature allows the microprocessor to select any of the framers through the PHY. The RS8228's eight interrupt inputs provide an internal mechanism for registering and controlling generated interrupts.

* The term xDSL is used throughout this document to refer to the various DSL formats as a group.

Distinguishing Features

- 8 cell-based TC Ports
- UTOPIA interface
  - Level 2
  - 8/16 bit modes
  - Multi-PHY
  - Redundant channel
- Glueless interface to Conexant's:
  - T1/E1 framers
  - T3/E3 framers
  - HDSL/SDSL devices
  - SAR devices
- Software reference material provided
- 8 chip selects for external framers
- 8 interrupt inputs for external framers
- Octet- and bit-level cell delineation
- ITU I.432-compliant
- Available in either 27 mm or 17 mm BGA packages

Functional Block Diagram



Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
RS8228EBG	28228-11	A	272-ball, 27 mm BGA	–40 °C to 85 °C
RS8228EBGB	28228-12	B	272-ball, 27 mm BGA	–40 °C to 85 °C
M28228	28228-21	A	256-ball, 17 mm BGA	–40 °C to 85 °C

Revision History

Revision	Level	Date	Description
C	—	April 2005	Corrected 0x05—IOMODE (Input/Output Mode Control Register), bits 5 and 3.
B	—	November 2003	Placed registers in numerical order.
A	—	November 2001	This version has the 17 mm BGA information included. Note that this document was previously released under the document numbers 100064A and 100064B.

Framer (Line) Interface Section

- Programmable bit or byte synchronous serial interface
- Direct connection to external Conexant components for:
  - T1/E1
  - DS3
  - E3
  - J2
  - xDSL
  - General purpose mode
  - Interrupt and chip select signals for each external framer

Cell Alignment Framing Section

- Supports ATM cell interface for:
  - Circuit-based physical layer
  - Cell-based physical layer
- Passes or rejects idle cells or selected cells based on header register configuration
- Recovers cell alignment from Header Error Correction (HEC)
- Performs single-bit HEC correction and single- or multiple-bit detection
- Generates cell status bits, cell counts, and error counts
- Inserts headers and generates HEC
- Inserts idle cells when no traffic is ready

UTOPIA Level 2 Interface

- PHY cell to UTOPIA interface
- 50 MHz maximum clock rate
- 8/16-bit data path interface
- Multi-PHY capability

Control and Status

Microprocessor Interface

- Asynchronous SRAM-like interface mode
- Synchronous, glueless Bt8233/RS8234 SAR interface mode
- 8-bit data bus
- Open-drain interrupt output
- Open-drain ready output
- 8–50 MHz operation
- All control registers are read/write
- Four programmable status indicator signals per port

Counters/Status Register Section

- Summary interrupt indications
- Configuration of interrupt enables
- One-second counter latching
- Counters for:
  - LOCD events
  - Corrected HEC errors
  - Uncorrected HEC errors
  - Transmitted cells
  - Matching received cells
  - Non-matching received cells

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1.0 Product Description

The RS8228 Octal ATM Transmission Convergence (TC) PHY device dramatically increases the level of integration for switches and access systems. The RS8228 integrates all the ATM Layer processing functions found in the ATM Forum Cell Based Transmission Convergence Sublayer specification (af-phy-0043.000) in each of eight individual ports.

A UTOPIA Level 2 Multi-PHY interface connects the device to the host switch or terminal system and concentrates the ATM cell traffic onto one bus interface. Because the RS8228 performs only the cell-based portion of the protocol stack, designers may choose the line formatter. Each port may be configured for operation at speeds from 64 kbps to 52 Mbps, allowing a maximum aggregate bandwidth of 416 Mbps for all active ports.

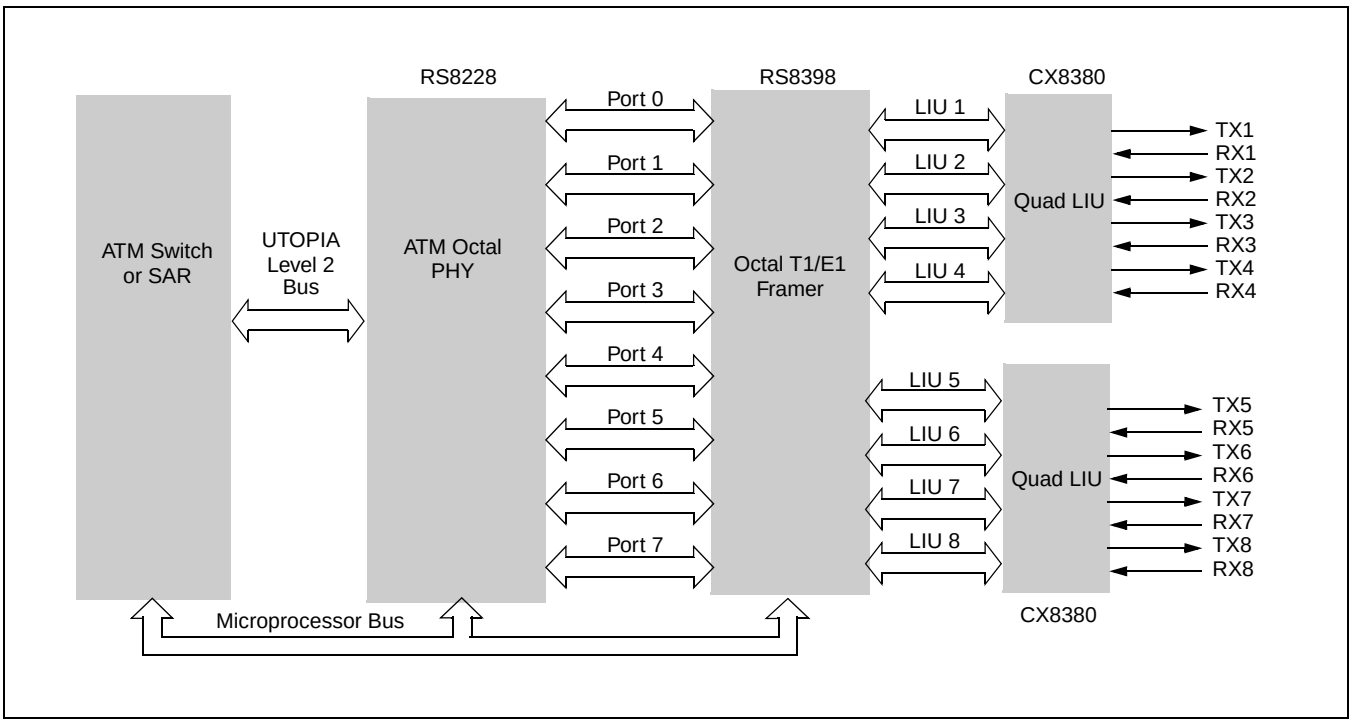
Typical system implementations center around the concentration of multiple standard data rates such as T1 and E1 lines, DS3 and E3 lines, and multiple Digital Subscriber Line (DSL) formats such as HDSL, ADSL or VDSL. For each specific format, external devices perform the appropriate PMDlayer functions and present the RS8228 with a payload bit stream. The RS8228 then performs all cell alignment functions on that bit stream. This gives system designers a simple, modular, and low-cost architecture for supporting all ATM interfaces below 52 Mbps. It also enables them to select the most integrated framer and LIU available, or reuse existing devices and software. The RS8228 device provides a low-cost ATM interface architecture for UNI or NNI interfaces.

NOTE: Both the 27 mm and 17 mm packages use the same silicon die. All references to the RS8228 apply to the M28228.

1.1 Application Overview

The RS8228 is typically used with line framer devices like the RS8398 T1/E1 octal transceiver, the Bt8970 Zip Wire or the Bt8953 HDLC Framer. It provides a chip-select feature that allows the microprocessor to select any framer connected to it. The RS8228 also has eight interrupt inputs so interrupts from the framers can be registered and controlled in the PHY. Figure 1-1 illustrates a typical application.

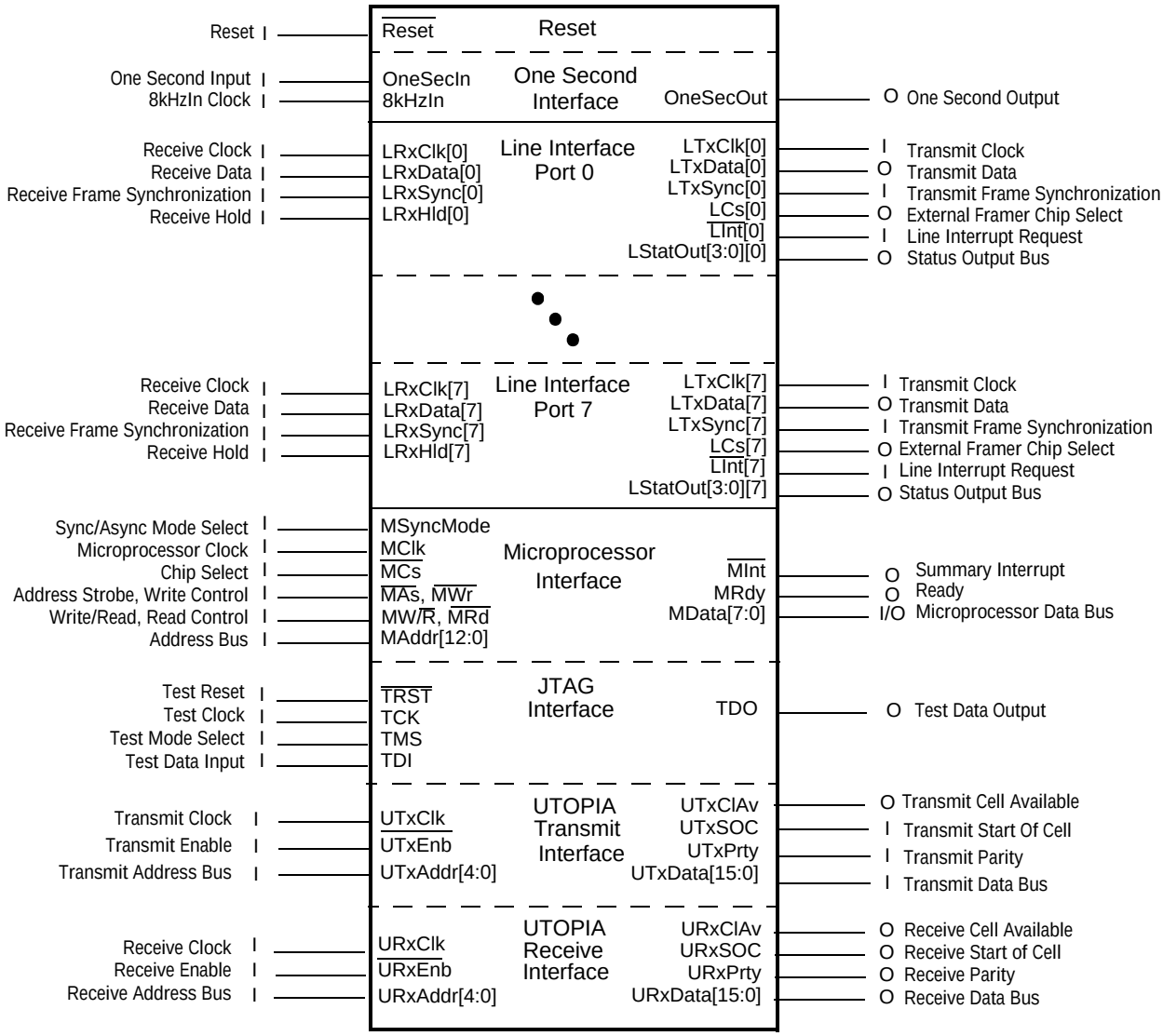
Figure 1-1. RS8228 Connected to a RS8398 Transceiver



1.2 Logic Diagram

Figure 1-2 illustrates a logic diagram of the RS8228's functional modules. Pin descriptions are listed in Table 1-1.

Figure 1-2. RS8228 Logic Diagram



NOTE(S): The overscore on inverted signals in this diagram equates to the "~" in the text of the document.

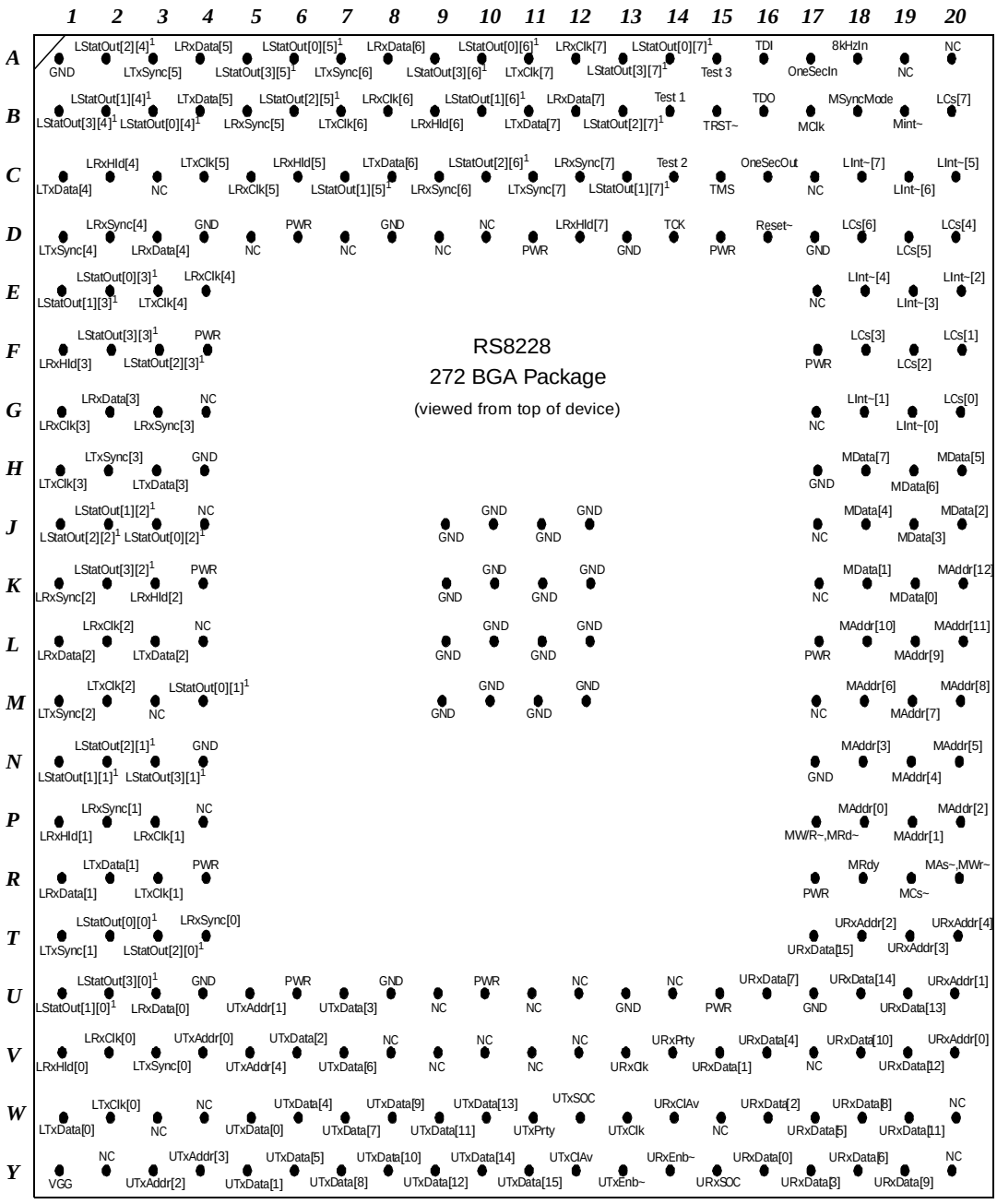
1.3 27 mm Pin Diagram and Definitions

Figure 1-3 illustrates a pinout diagram for the RS8228. It is a single CMOS integrated circuit packaged in a 272-pin BGA. All unused input pins should be connected to ground or power. Unused outputs should be left unconnected.

NOTE: The port numbers following the pin names in the Port Interface section represent each of the eight ports as follows:

LTxSync[0]—Line transmit sync for port 0.
LStatOut[3][0]—Line status output bit number 3 for port 0.

Figure 1-3. RS8228 27 mm Pinout Diagram (Top View)



NOTE(S): The LStatOut pin names list the signal index first [3:0], then the port number [7:0].

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***Table 1-1. RS8228 27 mm Pin Descriptions** (1 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Reset	Reset~	Device Reset	D16	TTL	—	I	When asserted low, resets the device.
One Second Interface	OneSecIn	One-Second Input	A17	TTL	—	I	When asserted high, the device may latch and hold its status, provided either EnStatLat (bit 5) or EnCntLat (bit 4) in the MODE register (0x0202) are written to a logic 1. This pin is typically strobed at one-second intervals. It is typically driven by OneSecOut (pin C16) but can also be driven by an external one-second source.
	OneSecOut	One-Second Output	C16	TTL	4 mA	O	When active high, indicates that 8000 periods of the 8kHzIn input (pin A18) have passed. Typically active at one second intervals. Remains active for one period of the 8kHzIn pin. It typically drives OneSecIn.
	8kHzIn	One-Second Reference Clock Input	A18	TTL	—	I	A clock input used to derive OneSecOut (pin C16). Typically operates at a frequency of 8 kHz).

Table 1-1. RS8228 27 mm Pin Descriptions *(2 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Framer (Line) Interfaces (ports 0–7)	LTxClk[0] LTxClk[1] LTxClk[2] LTxClk[3] LTxClk[4] LTxClk[5] LTxClk[6] LTxClk[7]	Line Transmit Clock Input (ports 0–7)	W2 R3 M2 H1 E3 C4 B7 A11	TTL	—	I	Used for the framer (line) transmit timing source. The polarity is set by TxClkPol (bit 3) in the IOMODE register (0x05).
	LTxData[0] LTxData[1] LTxData[2] LTxData[3] LTxData[4] LTxData[5] LTxData[6] LTxData[7]	Line Transmit Data Output (ports 0–7)	W1 R2 L3 H3 C1 B4 C8 B11	TTL	4 mA	O	Used for serial transmit output data.
	LTxSync[0] LTxSync[1] LTxSync[2] LTxSync[3] LTxSync[4] LTxSync[5] LTxSync[6] LTxSync[7]	Line Transmit Frame Synchronization (ports 0–7)	V3 T1 M1 H2 D1 A3 A7 C11	TTL	—	I	When transferring framed data, must be connected to the framer's start-of-frame output. In general purpose mode, this pin is ignored. The polarity is set by TxMrkPol (bit 4) in the IOMODE register (0x05).
	LRxClk[0] LRxClk[1] LRxClk[2] LRxClk[3] LRxClk[4] LRxClk[5] LRxClk[6] LRxClk[7]	Line Receive Clock Input (ports 0–7)	V2 P3 L2 G1 E4 C5 B8 A12	TTL	—	I	Used for the framer (line) receive timing source. The polarity is set by RxClkPol (bit 5) in the IOMODE register (0x05).
	LRxData[0] LRxData[1] LRxData[2] LRxData[3] LRxData[4] LRxData[5] LRxData[6] LRxData[7]	Line Receive Data Input (ports 0–7)	U3 R1 L1 G2 D3 A4 A8 B12	TTL	—	I	Used for serial receive input data.

***Table 1-1. RS8228 27 mm Pin Descriptions** (3 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Framer (Line) Interfaces (ports 0-7) (Continued)	LRxSync[0] LRxSync[1] LRxSync[2] LRxSync[3] LRxSync[4] LRxSync[5] LRxSync[6] LRxSync[7]	Line Receive Frame Synchronization (ports 0-7)	T4 P2 K1 G3 D2 B5 C9 C12	TTL	—	I	When transferring framed data, must be connected to the framer's start-of-frame output. In general purpose mode, this pin is ignored. The polarity is set by RxSyncPol (bit 4) in the IOMODE register (0x05).
	LRxHld[0] LRxHld[1] LRxHld[2] LRxHld[3] LRxHld[4] LRxHld[5] LRxHld[6] LRxHld[7]	Line Receiver Hold Input (ports 0-7)	V1 P1 K3 F1 C2 C6 B9 D12	TTL	—	I	Stops receive cell processing when asserted. The polarity is set by RxHldPol (bit 7) in the IOMODE register (0x05). When asserted, all receiver state machines are held in reset. Tie to 3.3 V for normal operation.
	LCs[0] LCs[1] LCs[2] LCs[3] LCs[4] LCs[5] LCs[6] LCs[7]	Line External Framer Chip Select (ports 0-7)	G20 F20 F19 F18 D20 D19 D18 B20	TTL	4 mA	O	When asserted, the corresponding external framer will be selected. The polarity is set by CsPol (bit 2) in the IOMODE register (0x05).
	LInt~[0] LInt~[1] LInt~[2] LInt~[3] LInt~[4] LInt~[5] LInt~[6] LInt~[7]	Line Interrupt Request (ports 0-7)	G19 G18 E20 E19 E18 C20 C19 C18	TTL	—	I	When asserted low, the corresponding framer needs servicing. The RS8228 may be used to transfer the interrupt request to the microprocessor via MInt~ (pin B19) if it is enabled. These pins have pull-up resistors.
	LStatOut[3][0] LStatOut[3][1] LStatOut[3][2] LStatOut[3][3] LStatOut[3][4] LStatOut[3][5] LStatOut[3][6] LStatOut[3][7]	Line Status Output 3 (ports 0-7)	U2 N3 K2 F2 B1 A5 A9 A13	TTL	4 mA	O	Reflects port signals based on the value of StatSel (bits 0 and 1) in the IOMODE register (0x05): LStatOut — StatSelect RcvrHld[7:0] — 00 NonMatch[7:0] — 01 RxOvfl[7:0] — 10 OutStat[3][7:0](0x07, bit 3) — 11 Eight RcvrHld, NonMatch, and RxOvfl signals (0–7) have numbers that correspond to the eight ports.

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Table 1-1. RS8228 27 mm Pin Descriptions *(4 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Framer (Line) Interfaces (port 0-7) (Continued)	LStatOut[2][0] LStatOut[2][1] LStatOut[2][2] LStatOut[2][3] LStatOut[2][4] LStatOut[2][5] LStatOut[2][6] LStatOut[2][7]	Line Status Output 2 (ports 0-7)	T3 N2 J1 F3 A2 B6 C10 B13	TTL	4 mA	O	Reflects various port signals based on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect HECCorr[7:0] — 00 IdleRcvd[7:0] — 01 TxOvfl[7:0] — 10 OutStat[2][7:0](0x07, bit 2) — 11 Eight HECCorr, IDlRcvd, and TxOvfl signals (0–7) have numbers that correspond to the eight ports.
	LStatOut[1][0] LStatOut[1][1] LStatOut[1][2] LStatOut[1][3] LStatOut[1][4] LStatOut[1][5] LStatOut[1][6] LStatOut[1][7]	Line Status Output 1 (ports 0-7)	U1 N1 J2 E1 B2 C7 B10 C13	TTL	4 mA	O	This pin reflects various port signals depending on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect HECDet[7:0] — 00 CellRcvd[7:0] — 01 SOCErr[7:0] — 10 OutStat[1][7:0](0x07, bit 1) — 11 Eight HECDet, CellRcvd, and SOCErr signals (0–7) have numbers that correspond to the eight ports.
	LStatOut[0][0] LStatOut[0][1] LStatOut[0][2] LStatOut[0][3] LStatOut[0][4] LStatOut[0][5] LStatOut[0][6] LStatOut[0][7]	Line Status Output 0 (ports 0-7)	T2 M4 J3 E2 B3 A6 A10 A14	TTL	4 mA	O	This pin reflects various port signals depending on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect LOCD[7:0] — 00 CellSent[7:0] — 01 ParErr[7:0] — 10 OutStat[0][7:0](0x07, bit 0) — 11 Eight LOCD, CellSent, and ParErr signals (0–7) have numbers that correspond to the eight ports.

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Table 1-1. RS8228 27 mm Pin Descriptions *(5 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface	MClk	Microprocessor Clock	B17	TTL	—	I	An 8–50 MHz clock signal input. The RS8228 samples the microprocessor interface pins (MCs~, MW/R~, MAs~, MAddr[6:0], and MData[7:0]) on the rising edge of this signal. The microprocessor interface output pins (MData[7:0], MInt~) are clocked on the rising edge of MClk.
	MSyncMode	Microprocessor Synchronous/ Asynchronous Bus Mode Select	B18	TTL	—	I	Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R~,MRd~ (pin P17) and MAs~,MWr~ (pin R20). A logic 1 selects the synchronous bus mode, compatible with Bt8230 and Bt8233. In this mode, these pins are defined as follows: MW/R~ (P17) and MAs~ (R20). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd~ (P17) and MWr~ (R20).
	MCs~	Microprocessor Chip Select	R19	TTL	—	I	When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MClk, MW/R~, MRd~, or MAs~, MWr~. Additionally, when MCs~ is asserted high, the MData[7:0] pins are in a high-impedance state but the MInt~ pin remains operational. ***NOTE(S):*** MCs~ must be asserted when using the LCs pins to select external framers.

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Table 1-1. RS8228 27 mm Pin Descriptions *(6 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface (Continued)	MW/R~ or MRd~	Microprocessor Write/ Read or Read Control	P17	TTL	—	I	When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R~ is asserted high, a write access is enabled and the MData[7:0] pin values will be written to the memory location indicated by the MAddr[6:0] pins. Also, when MW/R~ is asserted low in this mode, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read. Its value is placed on the MData[7:0] pins. Both read and write accesses assume the device is chip selected (MCs~ = 0), the address is valid (MAs~ = 0), and the device is not being reset (Reset~ = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd~ is asserted low, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read. Its value is placed on the MData[7:0] pins. The read access assumes the device is chip selected (MCs~ = 0), a write access is not being requested (MWr~ = 1), and the device is not being reset (Reset~ = 1).
	MAs~ or MWr~	Microprocessor Address Strobe or Write Control	R20	TTL	—	I	When MSyncMode is asserted high, this pin is an address strobe pin. When the MAs~ pin is asserted low, it indicates a valid address, MAddr[6:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr~ is asserted low, a write access is enabled and the MData[7:0] pin values will be written to the memory location indicated by the MAddr[6:0] pins. The write access assumes the device is chip selected (MCs~ = 0), a read access is not being requested (MRd~ = 1), and the device is not being reset (Reset~ = 1).

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***Table 1-1. RS8228 27 mm Pin Descriptions** (7 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface (Continued)	MAddr[12]	Microprocessor Address Bus	K20	TTL	—	I	These 13 bits are an address input for identifying the register to access. Registers are mapped into the address space 0000–1FFF.
	MAddr[11]		L20	TTL		I	
	MAddr[10]		L18	TTL		I	
	MAddr[9]		L19	TTL		I	
	MAddr[8]		M20	TTL		I	
	MAddr[7]		M19	TTL		I	
	MAddr[6]		M18	TTL		I	
	MAddr[5]		N20	TTL		I	
	MAddr[4]		N19	TTL		I	
	MAddr[3]		N18	TTL		I	
	MAddr[2]		P20	TTL		I	
	MAddr[1]		P19	TTL		I	
	MAddr[0]		P18	TTL		I	
	MData[7]	Microprocessor Data Bus	H18	TTL	8 mA	I/O	A bidirectional data bus for transferring read and write data.
	MData[6]		H19	TTL	8 mA	I/O	
	MData[5]		H20	TTL	8 mA	I/O	
	MData[4]		J18	TTL	8 mA	I/O	
	MData[3]		J19	TTL	8 mA	I/O	
	MData[2]		J20	TTL	8 mA	I/O	
	MData[1]		K18	TTL	8 mA	I/O	
	MData[0]		K19	TTL	8 mA	I/O	
	MRdy	Microprocessor Ready	R18	TTL	4 mA	O	When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.
	MInt~	Microprocessor Interrupt Request	B19	TTL	2 mA	O	When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an external wired OR logic implementation. See Section 2.4.6. An external pull-up resistor is required for this pin.

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Table 1-1. RS8228 27 mm Pin Descriptions *(8 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
JTAG (see IEEE 1149.1a-1993)	TRST~	Test Reset	B15	TTL	—	I	When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. Do not assert this reset unless a clock is provided on TCK.
	TCK	Test Clock	D14	TTL	—	I	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations.
	TMS	Test Mode Select	C15	TTL	—	I	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
	TDI	Test Data Input	A16	TTL	—	I	The serial test data input. This pin has a pull-up resistor.
	TDO	Test Data Output	B16	TTL	4 mA	O	The serial test data output.
UTOPIA Transmit	UTxClk	UTOPIA Transmit Clock	W13	TTL	—	I	A clock input used to synchronize transmitted data.
	UTxEnb~	Transmit Enable	Y13	TTL	—	I	Enables data transmission when asserted low.
	UTxAddr[0]	LSB	V4	TTL	—	I	The address of the PHY device being selected for transmission. Address 11111 (31 decimal) indicates a null PHY port.
	UTxAddr[1]		U5	TTL		I	
	UTxAddr[2]	UTOPIA Transmit Address	Y3	TTL		I	
	UTxAddr[3]		Y4	TTL		I	
	UTxAddr[4]	MSB	V5	TTL		I	

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***Table 1-1. RS8228 27 mm Pin Descriptions** (9 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
UTOPIA Transmit (Continued)	UTxData[0]	LSB	W5	TTL	—	I	Transmit data from the ATM layer.
	UTxData[1]		Y5	TTL		I	
	UTxData[2]		V6	TTL		I	
	UTxData[3]	UTOPIA Transmit Data	U7	TTL		I	
	UTxData[4]		W6	TTL		I	
	UTxData[5]		Y6	TTL		I	
	UTxData[6]		V7	TTL		I	
	UTxData[7]		W7	TTL		I	
	UTxData[8]		Y7	TTL		I	
	UTxData[9]		W8	TTL		I	
	UTxData[10]		Y8	TTL		I	
	UTxData[11]		W9	TTL		I	
	UTxData[12]		Y9	TTL		I	
	UTxData[13]		W10	TTL		I	
	UTxData[14]		Y10	TTL		I	
	UTxData[15]	MSB	Y11	TTL		I	
	UTxPrty	UTOPIA Transmit Parity Input	W11	TTL	—	I	The parity calculated over the UTxData bus. BusWidth (bit 0) in the IOMODE register (0x0202) determines whether parity is checked over UTxData[7:0] or UTxData[15:0]. OddEven (bit 2) in the UTOP1 register (0x0D) determines whether this pin represents even or odd parity.
	UTxSOC	UTOPIA Transmit Start of Cell	W12	TTL	—	I	Indicates the first byte of valid cell data transmitted when asserted high.
	UTxClAv	UTOPIA Transmit Cell Available	Y12	TTL	8 mA	O	Indicates a FIFO full condition or Cell Available condition, depending upon UTOPIA HandShake (bit 1) in the MODE register (0x0202). An external pull-down resistor is required for this pin.
UTOPIA Receive	URxClk	UTOPIA Receive Clock	V13	TTL	—	I	A clock input used to synchronize received data.
	URxEnb~	Receive Enable	Y14	TTL	—	I	Enables data reception when asserted low.
	URxAddr[0]	LSB	V20	TTL	—	I	The address of the PHY device being selected for reception. The address range is 0–30. Address 11111 (31 decimal) indicates a null PHY port.
	URxAddr[1]		U20	TTL		I	
	URxAddr[2]	UTOPIA Receive Address	T18	TTL		I	
	URxAddr[3]		T19	TTL		I	
	URxAddr[4]	MSB	T20	TTL		I	

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Table 1-1. RS8228 27 mm Pin Descriptions *(10 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
UTOPIA Receive (Continued)	URxData[0]	LSB	Y16	TTL	8 mA	O	Output the received data to the ATM layer.
	URxData[1]		V15	TTL	8 mA	O	
	URxData[2]		W16	TTL	8 mA	O	
	URxData[3]	UTOPIA Receive Data Bus	Y17	TTL	8 mA	O	
	URxData[4]		V16	TTL	8 mA	O	
	URxData[5]		W17	TTL	8 mA	O	
	URxData[6]		Y18	TTL	8 mA	O	
	URxData[7]		U16	TTL	8 mA	O	
	URxData[8]		W18	TTL	8 mA	O	
	URxData[9]		Y19	TTL	8 mA	O	
	URxData[10]		V18	TTL	8 mA	O	
	URxData[11]		W19	TTL	8 mA	O	
	URxData[12]		V19	TTL	8 mA	O	
	URxData[13]		U19	TTL	8 mA	O	
	URxData[14]		U18	TTL	8 mA	O	
	URxData[15]	MSB	T17	TTL	8 mA	O	
	URxPrty	UTOPIA Receive Parity	V14	TTL	8 mA	O	The parity calculated over the URxData bus. BusWidth (bit 0) in the IOMODE register (0x0202) determines whether parity is calculated over URxData[7:0] or URxData[15:0]. OddEven (bit 2) in the UTOP1 register (0x0D) determines whether this pin represents even or odd parity.
	URxSOC	Receive Start of Cell	Y15	TTL	8 mA	O	When active high, indicates the first byte of valid cell data received. An external pull-down resistor is required for this pin.
	URxClAv	UTOPIA Receive Cell Available	W14	TTL	8 mA	O	Indicates FIFO empty or Cell Buffer Available, depending upon HandShake (bit 1) in the MODE register (0x0202). An external pull-down resistor is required for this pin.

Table 1-1. RS8228 27 mm Pin Descriptions *(11 of 11)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Supply Voltage	PWR	Supply Voltage	D6 D11 D15 F4 F17 K4 L17 R4 R17 U6 U10 U15	—	—	—	Power supply connections.
	GND	Ground	A1 D4 D8 D13 D17 H4 H17 J9 J10 J11 J12 K9 K10 K11 K12 L9 L10 L11 L12 M9 M10 M11 M12 N4 N17 U4 U8 U13 U17	—	—	—	Ground connections.
	VGG	Electrostatic Discharge (ESD) Supply Voltage	Y1	—	—	—	Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, leave this pin unconnected.
Testing	Test 1	Manufacturing Test 1	B14	TTL	—	I	Reserved, connect to ground.
	Test 2	Manufacturing Test 2	C14	TTL	—	I	Reserved, connect to ground.
	Test 3	Manufacturing Test 3	A15	TTL	—	I	Reserved, connect to ground.

NOTE(S): All input and bi-directional pins have hysteresis.

1.4 17 mm Pin Diagram and Definitions

Figure 1-3 illustrates a pinout diagram for the M28228. It is a single CMOS integrated circuit packaged in a 256-pin BGA. All unused input pins should be connected to ground or power. Unused outputs should be left unconnected.

NOTE: The port numbers following the pin names in the Port Interface section represent each of the eight ports as follows:

LTxSync[0]—Line transmit sync for port 0.
LStatOut[3][0]—Line status output bit number 3 for port 0.

Figure 1-4. M28228 17 mm Pinout Diagram (Top View)

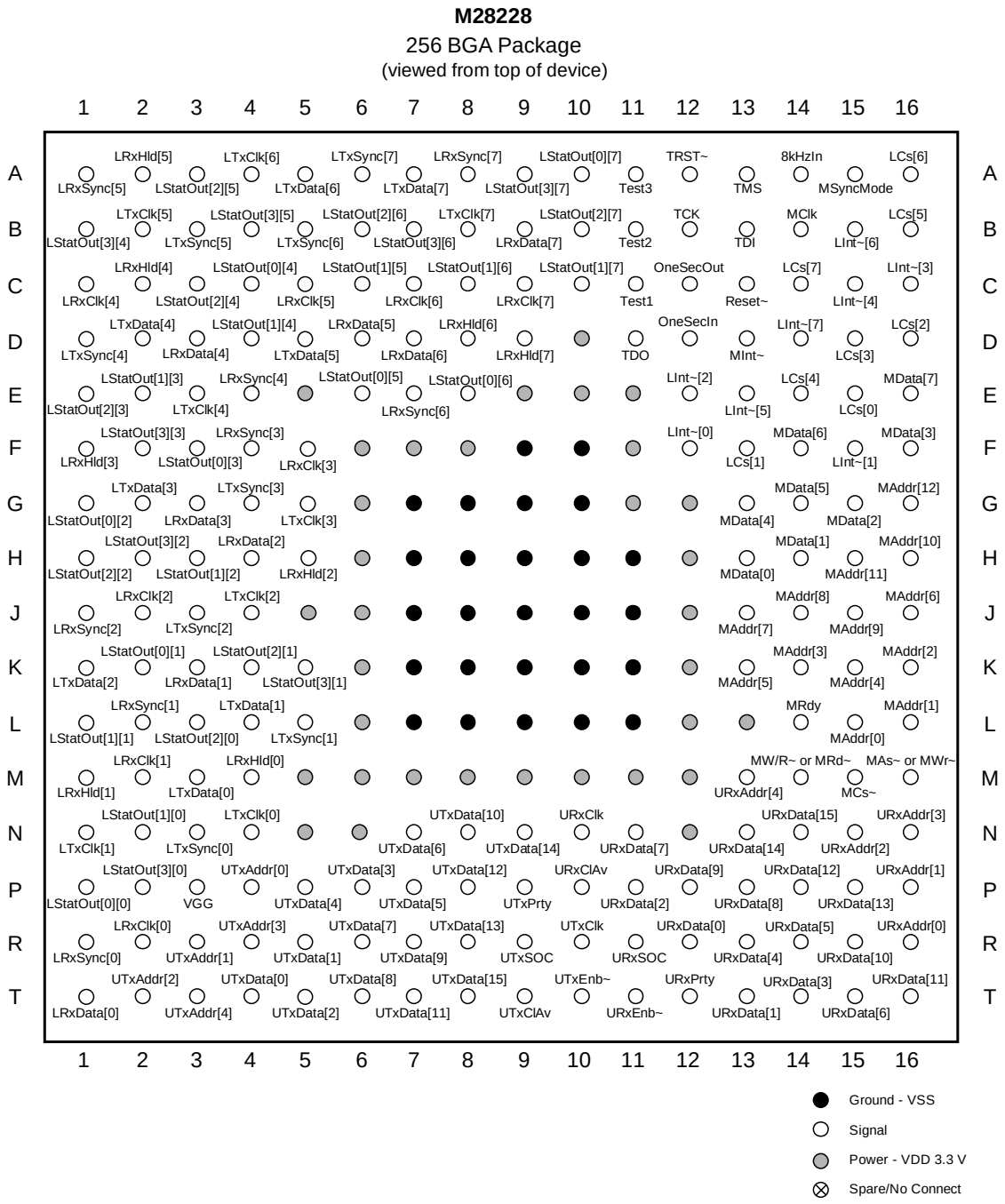

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***Table 1-2. RS8228 17 mm Pin Descriptions** (1 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Reset	Reset*	Device Reset	C13	TTL	—	I	When asserted low, resets the device.
One Second Interface	OneSecIn	One-Second Input	D12	TTL	—	I	When asserted high, the device may latch and hold its status, provided either EnStatLat (bit 5) or EnCntLat (bit 4) in the MODE register (0x0202) are written to a logic 1. This pin is typically strobed at one-second intervals. It is typically driven by OneSecOut (pin C16) but can also be driven by an external one-second source.
	OneSecOut	One-Second Output	C12	TTL	4 mA	O	When active high, indicates that 8000 periods of the 8kHzIn input (pin A18) have passed. Typically active at one second intervals. Remains active for one period of the 8kHzIn pin. It typically drives OneSecIn.
	8kHzIn	One-Second Reference Clock Input	A14	TTL	—	I	A clock input used to derive OneSecOut (pin C16). Typically operates at a frequency of 8 kHz).
Framer (Line) Interfaces (ports 0–7)	LTxClk[0] LTxClk[1] LTxClk[2] LTxClk[3] LTxClk[4] LTxClk[5] LTxClk[6] LTxClk[7]	Line Transmit Clock Input (ports 0–7)	N4 N1 J4 G5 E3 B2 A4 B8	TTL	—	I	Used for the framer (line) transmit timing source. The polarity is set by TxClkPol (bit 3) in the IOMODE register (0x05).
	LTxData[0] LTxData[1] LTxData[2] LTxData[3] LTxData[4] LTxData[5] LTxData[6] LTxData[7]	Line Transmit Data Output (ports 0–7)	M3 L4 K1 G2 D2 D5 A5 A7	TTL	4 mA	O	Used for serial transmit output data.
	LTxSync[0] LTxSync[1] LTxSync[2] LTxSync[3] LTxSync[4] LTxSync[5] LTxSync[6] LTxSync[7]	Line Transmit Frame Synchronization (ports 0–7)	N3 L5 J3 G4 D1 B3 B5 A6	TTL	—	I	When transferring framed data, must be connected to the framer's start-of-frame output. In general purpose mode, this pin is ignored. The polarity is set by TxMrkPol (bit 4) in the IOMODE register (0x05).
	LRxClk[0] LRxClk[1] LRxClk[2] LRxClk[3] LRxClk[4] LRxClk[5] LRxClk[6] LRxClk[7]	Line Receive Clock Input (ports 0–7)	R2 M2 J2 F5 C1 C5 C7 C9	TTL	—	I	Used for the framer (line) receive timing source. The polarity is set by RxClkPol (bit 5) in the IOMODE register (0x05).

Table 1-2. RS8228 17 mm Pin Descriptions *(2 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Framer (Line) Interfaces (ports 0-7) (Continued)	LRxData[0] LRxData[1] LRxData[2] LRxData[3] LRxData[4] LRxData[5] LRxData[6] LRxData[7]	Line Receive Data Input (ports 0–7)	T1 K3 H4 G3 D3 D6 D7 B9	TTL	—	I	Used for serial receive input data.
	LRxSync[0] LRxSync[1] LRxSync[2] LRxSync[3] LRxSync[4] LRxSync[5] LRxSync[6] LRxSync[7]	Line Receive Frame Synchronization (ports 0-7)	R1 L2 J1 F4 E4 A1 E7 A8	TTL	—	I	When transferring framed data, must be connected to the framer's start-of-frame output. In general purpose mode, this pin is ignored. The polarity is set by RxSyncPol (bit 4) in the IOMODE register (0x05).
	LRxHld[0] LRxHld[1] LRxHld[2] LRxHld[3] LRxHld[4] LRxHld[5] LRxHld[6] LRxHld[7]	Line Receiver Hold Input (ports 0-7)	M4 M1 H5 F1 C2 A2 D8 D9	TTL	—	I	Stops receive cell processing when asserted. The polarity is set by RxHldPol (bit 7) in the IOMODE register (0x05). When asserted, all receiver state machines are held in reset. Tie to V_{SS} for normal operation.
	LCs[0] LCs[1] LCs[2] LCs[3] LCs[4] LCs[5] LCs[6] LCs[7]	Line External Framer Chip Select (ports 0-7)	E15 F13 D16 D15 E14 B16 A16 C14	TTL	4 mA	O	When asserted, the corresponding external framer will be selected. The polarity is set by CsPol (bit 2) in the IOMODE register (0x05).
	LInt*[0] LInt*[1] LInt*[2] LInt*[3] LInt*[4] LInt*[5] LInt*[6] LInt*[7]	Line Interrupt Request (ports 0-7)	F12 F15 E12 C16 C15 E13 B15 D14	TTL	—	I	When asserted low, the corresponding framer needs servicing. The RS8228 may be used to transfer the interrupt request to the microprocessor via MInt* (pin B19) if it is enabled. These pins have pull-up resistors.

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***Table 1-2. RS8228 17 mm Pin Descriptions** (3 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Framer (Line) Interfaces (ports 0-7) (Continued)	LStatOut[3][0] LStatOut[3][1] LStatOut[3][2] LStatOut[3][3] LStatOut[3][4] LStatOut[3][5] LStatOut[3][6] LStatOut[3][7]	Line Status Output 3 (ports 0-7)	P2 K5 H2 F2 B1 B4 B7 A9	TTL	4 mA	O	Reflects port signals based on the value of StatSel (bits 0 and 1) in the IOMODE register (0x05): LStatOut — StatSelect RcvrHld[7:0] — 00 NonMatch[7:0] — 01 RxOvfl[7:0] — 10 OutStat[3][7:0](0x07, bit 3) — 11 Eight RcvrHld, NonMatch, and RxOvfl signals (0–7) have numbers that correspond to the eight ports.
	LStatOut[2][0] LStatOut[2][1] LStatOut[2][2] LStatOut[2][3] LStatOut[2][4] LStatOut[2][5] LStatOut[2][6] LStatOut[2][7]	Line Status Output 2 (ports 0-7)	L3 K4 H1 E1 C3 A3 B6 B10	TTL	4 mA	O	Reflects various port signals based on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect HECCorr[7:0] — 00 IdleRcvd[7:0] — 01 TxOvfl[7:0] — 10 OutStat[2][7:0](0x07, bit 2) — 11 Eight HECCorr, IDlRcvd, and TxOvfl signals (0–7) have numbers that correspond to the eight ports.
	LStatOut[1][0] LStatOut[1][1] LStatOut[1][2] LStatOut[1][3] LStatOut[1][4] LStatOut[1][5] LStatOut[1][6] LStatOut[1][7]	Line Status Output 1 (ports 0-7)	N2 L1 H3 E2 D4 C6 C8 C10	TTL	4 mA	O	This pin reflects various port signals depending on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect HECDet[7:0] — 00 CellRcvd[7:0] — 01 SOCErr[7:0] — 10 OutStat[1][7:0](0x07, bit 1) — 11 Eight HECDet, CellRcvd, and SOCErr signals (0–7) have numbers that correspond to the eight ports.
	LStatOut[0][0] LStatOut[0][1] LStatOut[0][2] LStatOut[0][3] LStatOut[0][4] LStatOut[0][5] LStatOut[0][6] LStatOut[0][7]	Line Status Output 0 (ports 0-7)	P1 K2 G1 F3 C4 E6 E8 A10	TTL	4 mA	O	This pin reflects various port signals depending on the value of StatSel (0x05, bits 0 and 1): LStatOut[3] — StatSelect LOCD[7:0] — 00 CellSent[7:0] — 01 ParErr[7:0] — 10 OutStat[0][7:0](0x07, bit 0) — 11 Eight LOCD, CellSent, and ParErr signals (0–7) have numbers that correspond to the eight ports.

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Table 1-2. RS8228 17 mm Pin Descriptions *(4 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface	MClk	Microprocessor Clock	B14	TTL	—	I	An 8–50 MHz clock signal input. The RS8228 samples the microprocessor interface pins (MCs*, MW/R*, MAs*, MAddr[6:0], and MData[7:0]) on the rising edge of this signal. The microprocessor interface output pins (MData[7:0], MInt*) are clocked on the rising edge of MClk.
	MSyncMode	Microprocessor Synchronous/ Asynchronous Bus Mode Select	A15	TTL	—	I	Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R*,MRd* (pin P17) and MAs*,MWr* (pin R20). A logic 1 selects the synchronous bus mode, compatible with Bt8230 and Bt8233. In this mode, these pins are defined as follows: MW/R* (P17) and MAs* (R20). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd* (P17) and MWr* (R20).
	MCs*	Microprocessor Chip Select	M15	TTL	—	I	When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MClk, MW/R*, MRd*, or MAs*, MWr*. Additionally, when MCs* is asserted high, the MData[7:0] pins are in a high-impedance state but the MInt* pin remains operational. ***NOTE(S):*** MCs* must be asserted when using the LCs pins to select external framers.

***Table 1-2. RS8228 17 mm Pin Descriptions** (5 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface (Continued)	MW/R* or MRd*	Microprocessor Write/ Read or Read Control	M14	TTL	—	I	When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R* is asserted high, a write access is enabled and the MData[7:0] pin values will be written to the memory location indicated by the MAddr[6:0] pins. Also, when MW/R* is asserted low in this mode, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read. Its value is placed on the MData[7:0] pins. Both read and write accesses assume the device is chip selected (MCs* = 0), the address is valid (MAs* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd* is asserted low, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read. Its value is placed on the MData[7:0] pins. The read access assumes the device is chip selected (MCs* = 0), a write access is not being requested (MWr* = 1), and the device is not being reset (Reset* = 1).
	MAs* or MWr*	Microprocessor Address Strobe or Write Control	M16	TTL	—	I	When MSyncMode is asserted high, this pin is an address strobe pin. When the MAs* pin is asserted low, it indicates a valid address, MAddr[6:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr* is asserted low, a write access is enabled and the MData[7:0] pin values will be written to the memory location indicated by the MAddr[6:0] pins. The write access assumes the device is chip selected (MCs* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).

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Table 1-2. RS8228 17 mm Pin Descriptions *(6 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Microprocessor Interface (Continued)	MAddr[12] MAddr[11] MAddr[10] MAddr[9] MAddr[8] MAddr[7] MAddr[6] MAddr[5] MAddr[4] MAddr[3] MAddr[2] MAddr[1] MAddr[0]	Microprocessor Address Bus	G16 H15 H16 J15 J14 J13 J16 K13 K15 K14 K16 L16 L15	TTL	—	I	These 13 bits are an address input for identifying the register to access. Registers are mapped into the address space 0000–1FFF.
	MData[7] MData[6] MData[5] MData[4] MData[3] MData[2] MData[1] MData[0]	Microprocessor Data Bus	E16 F14 G14 G13 F16 G15 H14 H13	TTL	8 mA	I/O	A bidirectional data bus for transferring read and write data.
	MRdy	Microprocessor Ready	L14	TTL	4 mA	O	When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.
	MInt*	Microprocessor Interrupt Request	D13	TTL	2 mA	O	When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an external wired OR logic implementation. See Section 2.4.6. An external pull-up resistor is required for this pin.
JTAG (see IEEE 1149.1a-1993)	TRST*	Test Reset	A12	TTL	—	I	When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. Do not assert this reset unless a clock is provided on TCK.
	TCK	Test Clock	B12	TTL	—	I	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations.
	TMS	Test Mode Select	A13	TTL	—	I	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
	TDI	Test Data Input	B13	TTL	—	I	The serial test data input. This pin has a pull-up resistor.
	TDO	Test Data Output	D11	TTL	4 mA	O	The serial test data output.

***Table 1-2. RS8228 17 mm Pin Descriptions** (7 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
UTOPIA Transmit	UTxClk	UTOPIA Transmit Clock	R10	TTL	—	I	A clock input used to synchronize transmitted data.
	UTxEnb*	Transmit Enable	T10	TTL	—	I	Enables data transmission when asserted low.
	UTxAddr[0]	LSB	P4	TTL	—	I	The address of the PHY device being selected for transmission. Address 11111 (31 decimal) indicates a null PHY port.
	UTxAddr[1]		R3	TTL		I	
	UTxAddr[2]	UTOPIA Transmit Address	T2	TTL		I	
	UTxAddr[3]		R4	TTL		I	
	UTxAddr[4]	MSB	T3	TTL		I	
UTOPIA Transmit (Continued)	UTxData[0]	LSB	T4	TTL	—	I	Transmit data from the ATM layer.
	UTxData[1]		R5	TTL		I	
	UTxData[2]		T5	TTL		I	
	UTxData[3]	UTOPIA Transmit Data	P6	TTL		I	
	UTxData[4]		P5	TTL		I	
	UTxData[5]		P7	TTL		I	
	UTxData[6]		N7	TTL		I	
	UTxData[7]		R6	TTL		I	
	UTxData[8]		T6	TTL		I	
	UTxData[9]		R7	TTL		I	
	UTxData[10]		N8	TTL		I	
	UTxData[11]		T7	TTL		I	
	UTxData[12]		P8	TTL		I	
	UTxData[13]		R8	TTL		I	
	UTxData[14]		N9	TTL		I	
	UTxData[15]	MSB	T8	TTL		I	
	UTxPrty	UTOPIA Transmit Parity Input	P9	TTL	—	I	The parity calculated over the UTxData bus. BusWidth (bit 0) in the IOMODE register (0x0202) determines whether parity is checked over UTxData[7:0] or UTxData[15:0]. OddEven (bit 2) in the UTOP1 register (0x0D) determines whether this pin represents even or odd parity.
	UTxSOC	UTOPIA Transmit Start of Cell	R9	TTL	—	I	Indicates the first byte of valid cell data transmitted when asserted high.
	UTxClAv	UTOPIA Transmit Cell Available	T9	TTL	8 mA	O	Indicates a FIFO full condition or Cell Available condition, depending upon UTOPIA HandShake (bit 1) in the MODE register (0x0202). An external pull-down resistor is required for this pin.

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Table 1-2. RS8228 17 mm Pin Descriptions *(8 of 10)*

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
UTOPIA Receive	URxClk	UTOPIA Receive Clock	N10	TTL	—	I	A clock input used to synchronize received data.
	URxEnb*	Receive Enable	T11	TTL	—	I	Enables data reception when asserted low.
	URxAddr[0]	LSB	R16	TTL	—	I	The address of the PHY device being selected for reception. The address range is 0–30. Address 11111 (31 decimal) indicates a null PHY port.
	URxAddr[1]		P16	TTL		I	
	URxAddr[2]	UTOPIA Receive Address	N15	TTL		I	
	URxAddr[3]		N16	TTL		I	
	URxAddr[4]	MSB	M13	TTL		I	
UTOPIA Receive (Continued)	URxData[0]	LSB	R12	TTL	8 mA	O	Output the received data to the ATM layer.
	URxData[1]		T13	TTL	8 mA	O	
	URxData[2]		P11	TTL	8 mA	O	
	URxData[3]	UTOPIA Receive Data Bus	T14	TTL	8 mA	O	
	URxData[4]		R13	TTL	8 mA	O	
	URxData[5]		R14	TTL	8 mA	O	
	URxData[6]		T15	TTL	8 mA	O	
	URxData[7]		N11	TTL	8 mA	O	
	URxData[8]		P13	TTL	8 mA	O	
	URxData[9]		P12	TTL	8 mA	O	
	URxData[10]		R15	TTL	8 mA	O	
	URxData[11]		T16	TTL	8 mA	O	
	URxData[12]		P14	TTL	8 mA	O	
	URxData[13]		P15	TTL	8 mA	O	
	URxData[14]		N13	TTL	8 mA	O	
	URxData[15]	MSB	N14	TTL	8 mA	O	
	URxPrty	UTOPIA Receive Parity	T12	TTL	8 mA	O	The parity calculated over the URxData bus. BusWidth (bit 0) in the IOMODE register (0x0202) determines whether parity is calculated over URxData[7:0] or URxData[15:0]. OddEven (bit 2) in the UTOP1 register (0x0D) determines whether this pin represents even or odd parity.
	URxSOC	Receive Start of Cell	R11	TTL	8 mA	O	When active high, indicates the first byte of valid cell data received. An external pull-down resistor is required for this pin.
	URxClAv	UTOPIA Receive Cell Available	P10	TTL	8 mA	O	Indicates FIFO empty or Cell Buffer Available, depending upon HandShake (bit 1) in the MODE register (0x0202). An external pull-down resistor is required for this pin.

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Table 1-2. RS8228 17 mm Pin Descriptions (9 of 10)

	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Supply Voltage	PWR	Supply Voltage	D10 E5 E9 E10 E11 F6 F7 F8 F11 G6 G11 G12 H6 H12 J5 J6 J12 K6 K12 L6 L12 L13 M5 M6 M7 M8 M9 M10 M11 M12 N5 N6 N12	—	—	—	Power supply connections.

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Table 1-2. RS8228 17 mm Pin Descriptions *(10 of 10)*

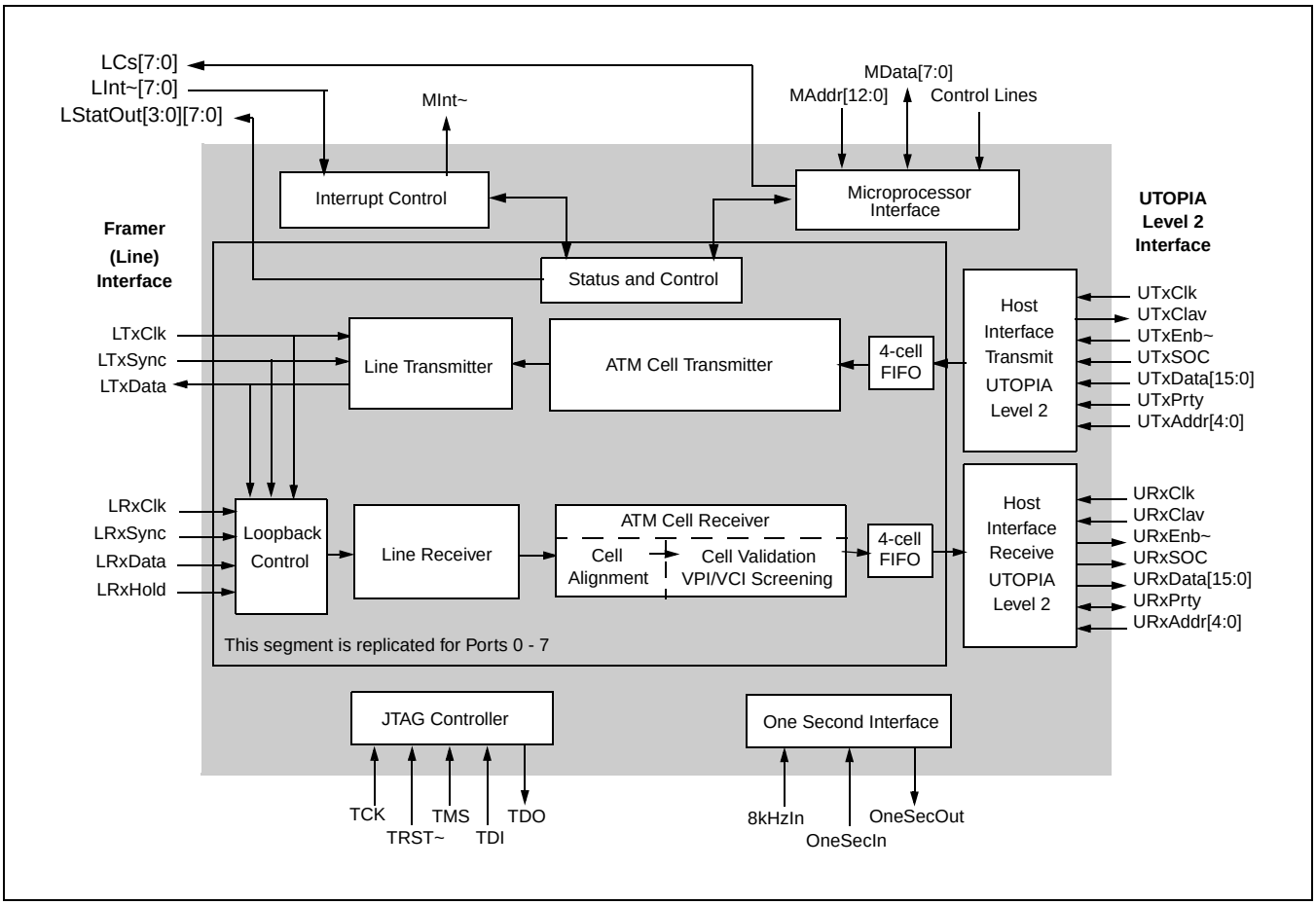
	Pin Label	Signal Name	No.	Type	Driver Strength	I/O	Description
Supply Voltage	GND	Ground	F9 F10 G7 G8 G9 G10 H7 H8 H9 H10 H11 J7 J8 J9 J10 J11 K7 K8 K9 K10 K11 L7 L8 L9 L10 L11	—	—	—	Ground connections.
	VGG	Electrostatic Discharge (ESD) Supply Voltage	P3	—	—	—	Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, leave this pin unconnected.
Testing	Test 1	Manufacturing Test 1	C11	TTL	—	I	Reserved, connect to ground.
	Test 2	Manufacturing Test 2	B11	TTL	—	I	Reserved, connect to ground.
	Test 3	Manufacturing Test 3	A11	TTL	—	I	Reserved, connect to ground.

NOTE(S): All input and bi-directional pins have hysteresis.

1.5 Block Diagram and Descriptions

Figure 1-5 illustrates a detailed block diagram of the RS8228/M28228 device. Traffic is transmitted from the ATM layer device via the UTOPIA bus, in either an 8- or 16-bit format. The ATM cells are then formatted for serial-line transmission by one of the RS8228 transmit ports. In the receive direction, serial network data is packed into octets by the receive port and passed to the ATM cell receiver module. Octet data is then delineated into ATM cells, checked, and sent to the UTOPIA port. The UTOPIA interface communicates with the next layer of ATM processing.

Figure 1-5. RS8228 Block Diagram



2.0 Functional Description

This chapter describes the primary functions of the RS8228, including the ATM cell processor, the UTOPIA interface, and the microprocessor interface.

2.1 ATM Cell Processor

The RS8228's ATM cell receiver block is responsible for recovering cell alignment using the HEC octet, performing detection/correction, and descrambling the payload octets. The resulting ATM cells are then passed to the ATM layer via the UTOPIA interface. Simultaneously, the ATM transmitter block is receiving data from the ATM layer, optionally inserting header fields, optionally calculating the HEC, and sending the cells to the framers. If no data is being received from the ATM layer, the cell processor generates idle cells based on the data programmed into the associated registers.

The RS8228 has all counters needed for capturing ATM error events and performs payload CRC calculations as required by the AAL formats. It generates cell status events, cell counts, and error counts.

2.1.1 ATM Cell Transmitter

The ATM cell transmitter controls the generation and formatting of 53-octet ATM cells that are sent to the Framer (Line) Transmit Ports. This block formats an octet stream containing ATM data cells from the ATM layer device when those cells are available. All 53 octets of the data cells may be obtained from the external data source and formatted into the outgoing octet stream.

This block calculates the HEC octet in the outgoing cell from the header field. The calculated HEC octet can be inserted in place of the incoming data octet by writing DisHEC (bit 7) in the CGEN register (0x08) to a logic 0. For testing purposes, this HEC octet can be corrupted by XORing the calculated value with a specific error pattern input set in the ERRPAT register (0x0B). This HEC error is achieved by writing ErrHEC (bit 4) in the CGEN register (0x08) to a logic 1. The remaining 48-octet payload field of the outgoing cell is obtained from the external data source. The payload can be scrambled.

When there is no data from the ATM layer device, the RS8228 inserts idle cells automatically in the outgoing octet stream. The 4-octet header field for these idle cells comes from the TXIDL1–4 registers (0x14–17). The HEC octet is calculated and inserted automatically. The payload field is filled with the octet contained in the IDLPAY register (0x0A).

In normal operation, the 4-octet header field in the outgoing cell is passed on from the ATM layer device. Header patterns can be modified in the TXHDR1–4 registers (0x10–13) and inserted into outgoing cells in place of header bytes received from the ATM layer. Whether the original header cells or replacement cells are sent is controlled by bits 0–4 in the HDRFIELD (0x09) register.

2.1.1.1 HEC Generation

In normal operation, the RS8228 calculates the HEC for the four header bytes of each cell coming from the ATM layer. It then adds the HEC coset (55 hex, by ATM standards) and inserts the result in octet 5 of the outgoing cell. HEC calculation can be disabled by setting bit 7 of CGEN (0x08) to a 1. When HEC is disabled, the RS8228 leaves the contents of the HEC field unchanged and transmits whatever data is placed in that field by the ATM layer.

The HEC coset is used to maintain a value other than zero in the HEC field. If the first four bytes in the header are zero, the HEC derived from these bytes is also zero. When this occurs and there are strings of zeros in the data, the receiver cannot determine cell boundaries. Therefore, it is recommended that the value 55 hex be added to the HEC before transmission. To enable the HEC coset on the transmit side, set bit 6 in register CGEN (0x08) to one. To enable the receive HEC coset, set bit 5 in register CVAL (0x0C) to one.

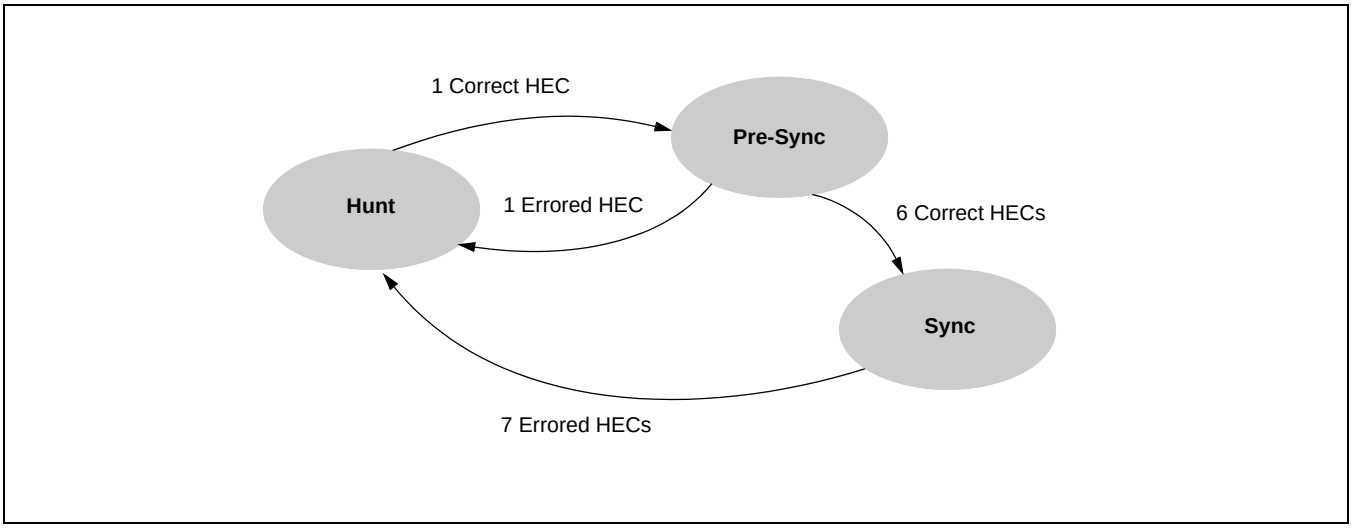
2.1.2 ATM Cell Receiver

The ATM cell receiver performs cell delineation on incoming data cells by searching for the position of a valid HEC field within the cell. The HEC coset can be either active or inactive; this is determined in bit 5 in the CVAL (0x0C) register.

2.0.0.1 Cell Delineation

The ATM block receives octets from the framers and recovers ATM cells by means of cell delineation. Cell delineation is achieved by aligning ATM cell boundaries using the HEC algorithm. Four consecutive bytes are chosen and the HEC value is calculated. The result is compared with the value of the following byte. This “hunt” is continued by shifting this four-byte window, one byte at a time, until the calculated HEC value equals the received HEC value. When this occurs, a pre-sync state is declared and the next 48 bytes are assumed to be payload. The ATM block calculates HEC on the four bytes following this payload, assuming that a new cell has begun. If seven consecutive header blocks are found, synchronization is declared. If any HEC calculation fails in the pre-sync state, the process begins again (see Figure 2-1). Synchronization will be held until seven consecutive incorrect HECs are received. At this time, the “hunt” state is reinitiated.

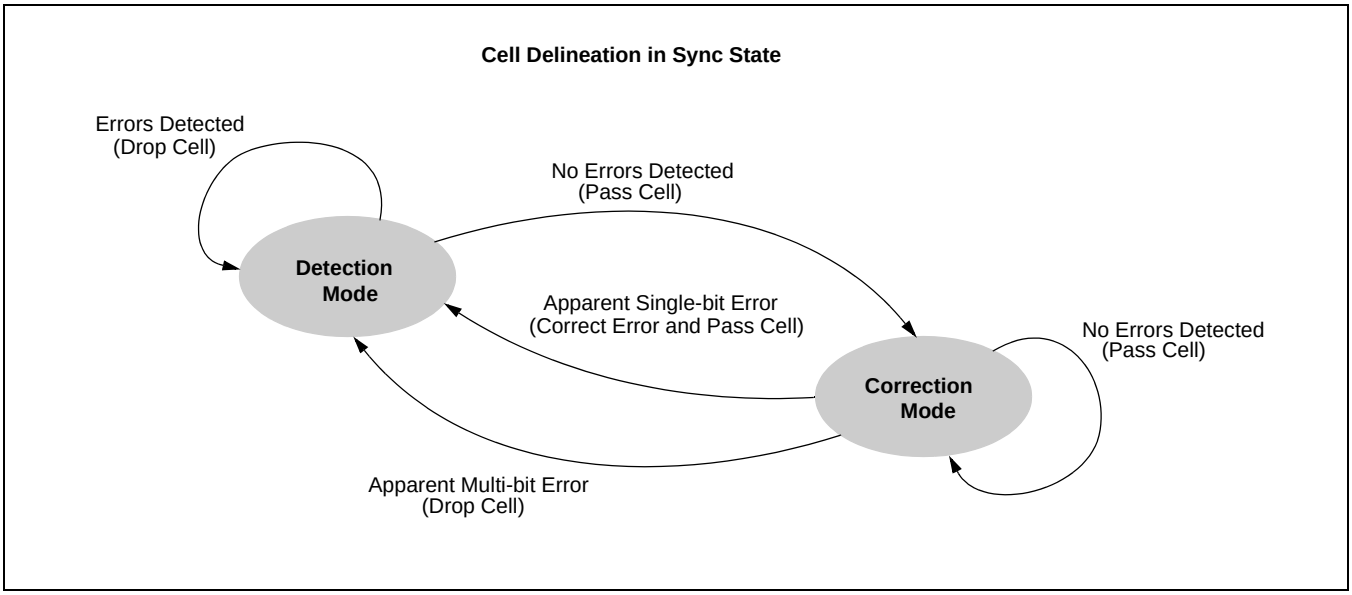
Figure 2-1. Cell Delineation Process



During the sync state of cell delineation, cells are passed to the UTOPIA interface if the HEC is valid. If a single-bit error in the header is detected, the error is corrected (optionally), and the cell is passed to the UTOPIA interface. If HEC checking is enabled and HEC correcting is disabled (bit 3 in the CVAL register [0x0C]), cells with single-bit HEC errors are discarded. If a multi-bit error is detected, the cell is dropped. Once either type of error is noted, all subsequent errored cells are dropped until a valid cell is received. This rule applies even for single-bit errors that could be corrected. Once a valid cell is detected, the process begins again. (See Figure 2-2.)

When LOCD occurs, an interrupt is generated and the RS8228 automatically enters the “hunt” mode. However, the cell is still being scrambled by the far-end transmitter, leaving only the headers (or just the HEC byte in Distributed Sample Scrambler [DSS]) unscrambled. This means that the only repetitive byte patterns in the data stream that meet the cell delineation criteria are valid headers (or just the HEC bytes in DSS).

Figure 2-2. Header Error Check Process



When the RS8228 is in general purpose mode, a synchronization pulse from the framer interface is not always available. In this mode, the RS8228 performs a bit serial search to find byte and cell alignment. The RS8228 selects a starting window of 32 sequential bits and calculates the HEC over this window. This HEC is then compared to the next eight incoming bits. If they do not match, the RS8228 shifts the 32-bit window by 1 bit and recalculates the HEC until a valid HEC position is found. Once byte-alignment is achieved, cell delineation is performed.

2.0.0.2 Cell Screening

The RS8228 provides two optional types of cell screening. The first type, idle cell rejection, prevents idle cells from being passed on. The second type, user traffic screening, compares incoming bits to the values in the receive cell header registers. Cells are rejected or accepted based on the bit patterns of their headers.

Idle cell rejection is enabled in bit 6 of the CVAL register (0x0C). If this bit is set to 1, all incoming cells that match the contents of the Receive Idle Cell Header Control Registers, RXIDL1–4 (0x20–23), are rejected. Individual bits in the Receive Idle Cell Mask Control Registers, IDLMSK1–4 (0x24–27), can be set to 1 or Don’t Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their value. If idle cell rejection is disabled, cells pass directly to user traffic screening.

User traffic cell screening is similar to idle cell screening in that the incoming cells are compared to the Receive Cell Header Control Registers, RXHDR1–4 (0x18–1B). Individual bits in the Receive Cell Mask Control Registers, RXMSK1–4 (0x1C–1F), can be set to 1 or Don't Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their values. The RejHdr bit (bit 7) in the CVAL register (0x0C) determines whether matching cells are rejected or accepted. If it is set to 0, matching cells are accepted. If it is set to 1, matching cells are rejected. See Table 2-1 and Table 2-2.

Table 2-1. Cell Screening—Matching

Receive Cell Mask Bit	Receive Cell Header Bit	Incoming Bit	Result
0	0	0	Match
0	0	1	Fail
0	1	0	Fail
0	1	1	Match
1	x	x	Match

Table 2-2. Cell Screening—Accept/Reject Cell

Cell	Reject Header	Result
Match	0	Accept Cell
Match	1	Reject Cell
Fail	0	Reject Cell
Fail	1	Accept Cell

2.1.3 Cell Scrambler

The ATM standard requires cell scrambling to ensure that only valid headers are found in the cell delineation process. Scrambling randomizes any repeated patterns or other data strings that could be mistaken for valid headers. The RS8228 supports two types of scrambling as defined by ITU-T I.432:

1. Self Synchronizing Scrambler (SSS)
2. Distributed Sample Scrambler (DSS). Typically, SSS is used and is, therefore, the RS8228's default method. However, xDSL in asynchronous format generally use DSS.

NOTE: *If both SSS and DSS are enabled, SSS overrides DSS.*

2.0.0.1 SSS Scrambling

SSS scrambling uses the polynomial $\times^{43} + 1$ to scramble the payload, leaving the five header bytes untouched. It can be enabled in EnTxCellScr, bit 5, of the CGEN register (0x08).

Descrambling uses the same polynomial to recover the 48-byte cell payload. It can be enabled in EnRxCellScr, bit 4, of the CVAL register (0x0C). SSS scrambling runs at up to 45 Mbps.

2.0.0.2 DSS Scrambling

DSS scrambling uses the $\times^{31} + \times^{28} + 1$ polynomial to scramble the entire cell, except the HEC byte. HEC is calculated after the first four bytes of the header have been scrambled. DSS scrambling is enabled in EnTxDSSScr, bit 1, of the CGEN register (0x08).

Descrambling uses the first six bits of the HEC for alignment. Once alignment is found, all eight bits of the HEC are sampled. Descrambling uses the same polynomial to recover the 48-byte cell payload. It is enabled in EnRxDSSScr, bit 0, of the CGEN register (0x08). If DSS descrambling fails, the RS8228 defaults to unscrambled mode.

2.2 Framing Modes

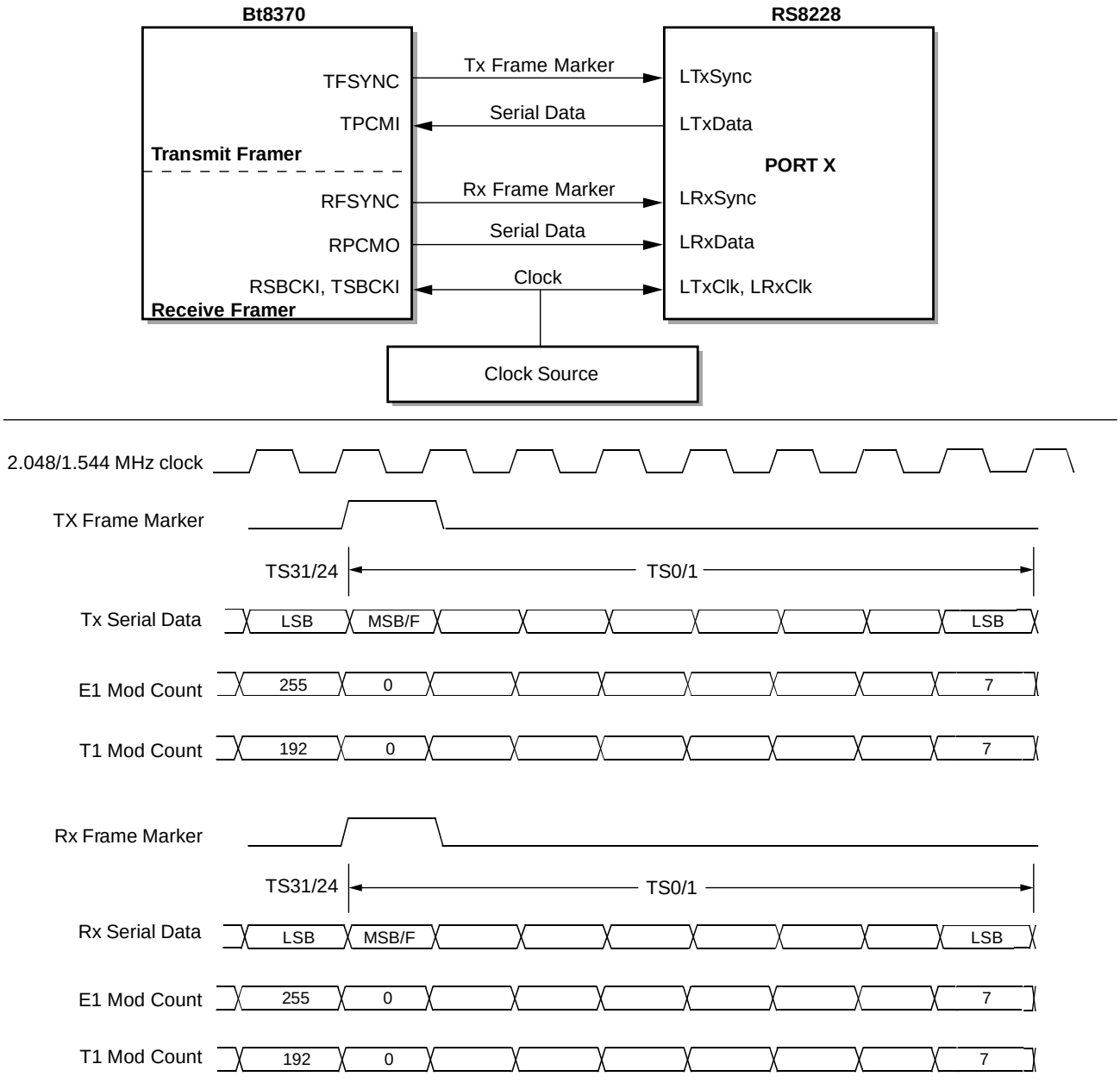
The RS8228's eight ports can be individually configured for the major framing modes to a maximum of 52 Mbps: T1/E1, DS3, E3/G.832, and J2. A general purpose framing mode provides an interface to customized framers at a maximum of 52 Mbps. Each of the eight ports can be configured for a different mode.

2.2.1 T1/E1 Timing for the CX28229

This describes the timing requirements of the RS8228 when operating in T1 or E1 mode. Connection to a Bt8370 T1/E1 framer is used as an example, as illustrated in Figure 2-3. The RS8228 receives a T1/E1 data stream from the external framer, ignores the T1/E1 overhead, extracts the ATM cells, and passes the ATM cells to the ATM layer device. In the transmit direction, the RS8228 inserts 0's in the overhead bit locations and fills the rest of the frame with ATM cells from the UTOPIA bus.

For the E1 mode, the ATM cells are mapped into time slots 1–15 and 17–31 as described in *Recommendation G.704*. For the T1 mode, the ATM cells are mapped into time slots 1–24.

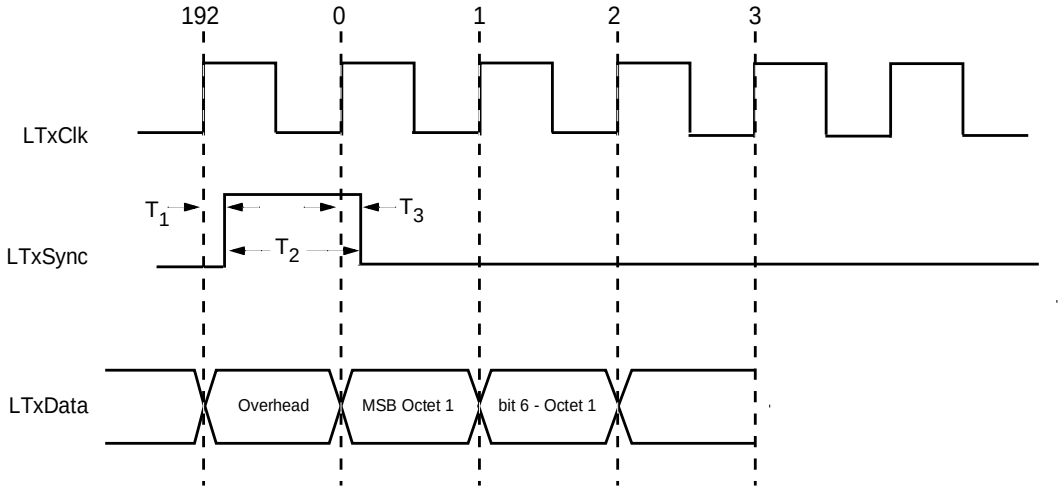
Figure 2-3. Bt8370 Interface Diagram



NOTE(S):

In E1 mode, ATM cells are mapped into time slots 1–15 and 17–31 as described in Recommendation G.704.
In T1 mode, ATM cells are mapped into time slots 1–24.

Figure 2-4. Transmit Waveforms



NOTE(S):

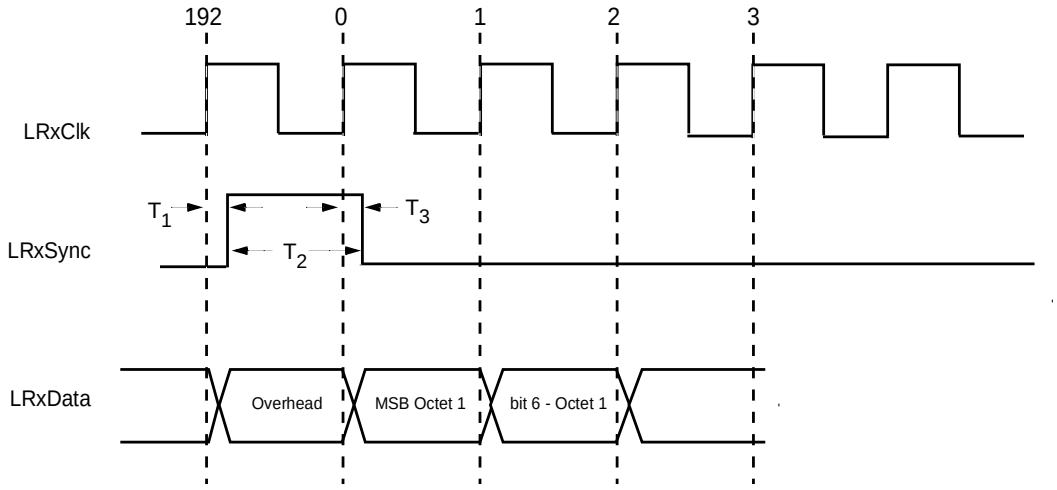
The diagram shows the RS8228 programmed to sample on the rising edge of the clock.

For T_1, LTxSync must occur at least 10 ns *after* the rising edge of the 193rd clock.

T_2 must have a minimum of 1 clock period.

For T_3, the hold time is 10 ns after the rising edge of the clock.

Figure 2-5. Receive Waveforms



NOTE(S):

The diagram shows the RS8228 programmed to sample on the rising edge of the clock.

The Overhead bit is sampled on the clock edge 0.

For T_1, LRxSync must occur at least 10 ns *after* the rising edge of the 193rd clock.

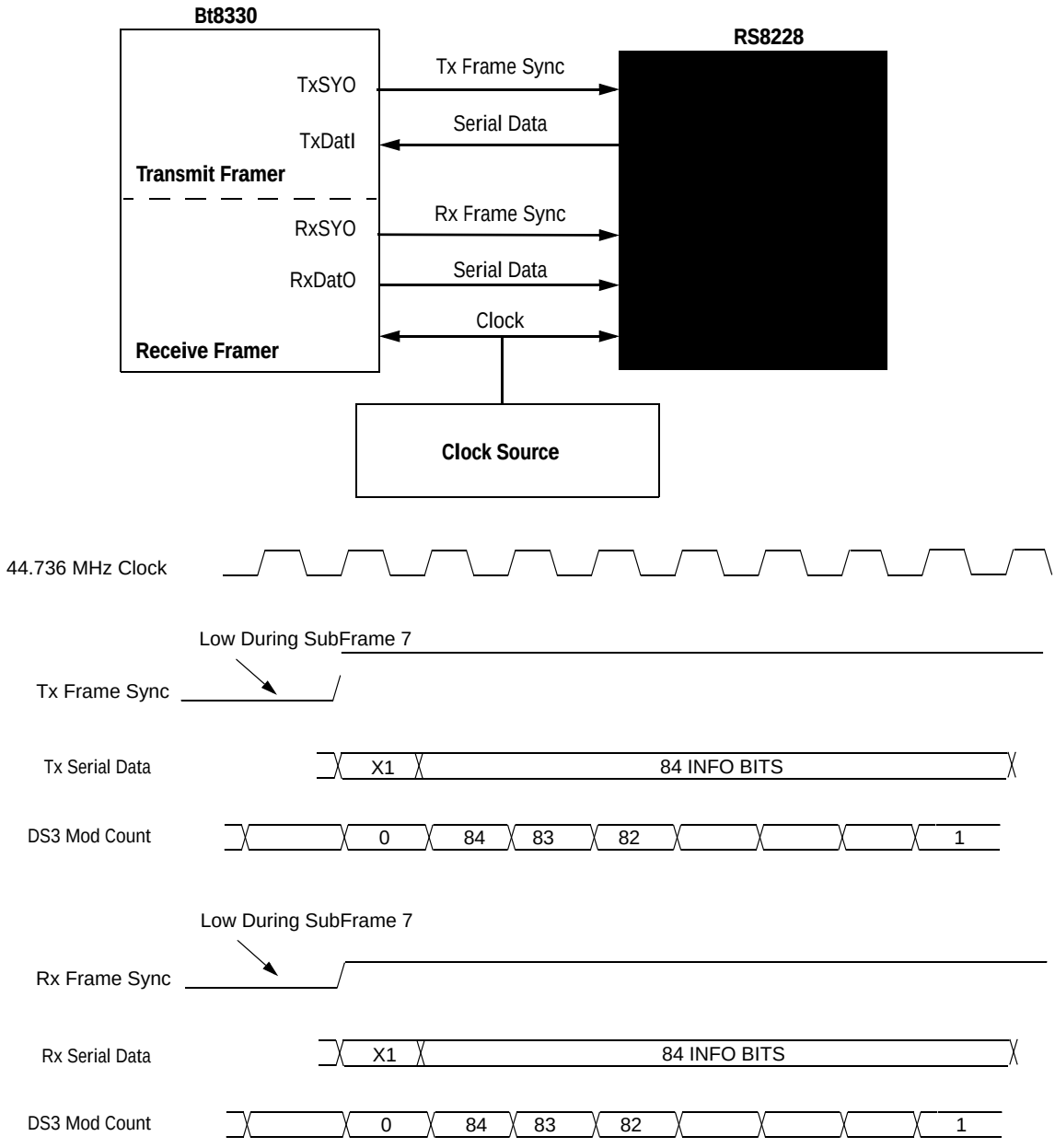
T_2 must have a minimum of 1 clock period.

For T_3, the hold time is 10 ns after the rising edge of the clock.

2.2.2 DS3 Interface

The RS8228 interfaces directly to the Bt8330 DS3 framer, as shown in Figure 2-6. The RS8228 receives a DS3 data stream from the external framer, extracts the ATM cells, ignores the DS3 overhead, and passes the ATM cells to the ATM layer device. The RS8228 performs the inverse process on transmitted data.

Figure 2-6. Bt8330 Interface Diagram

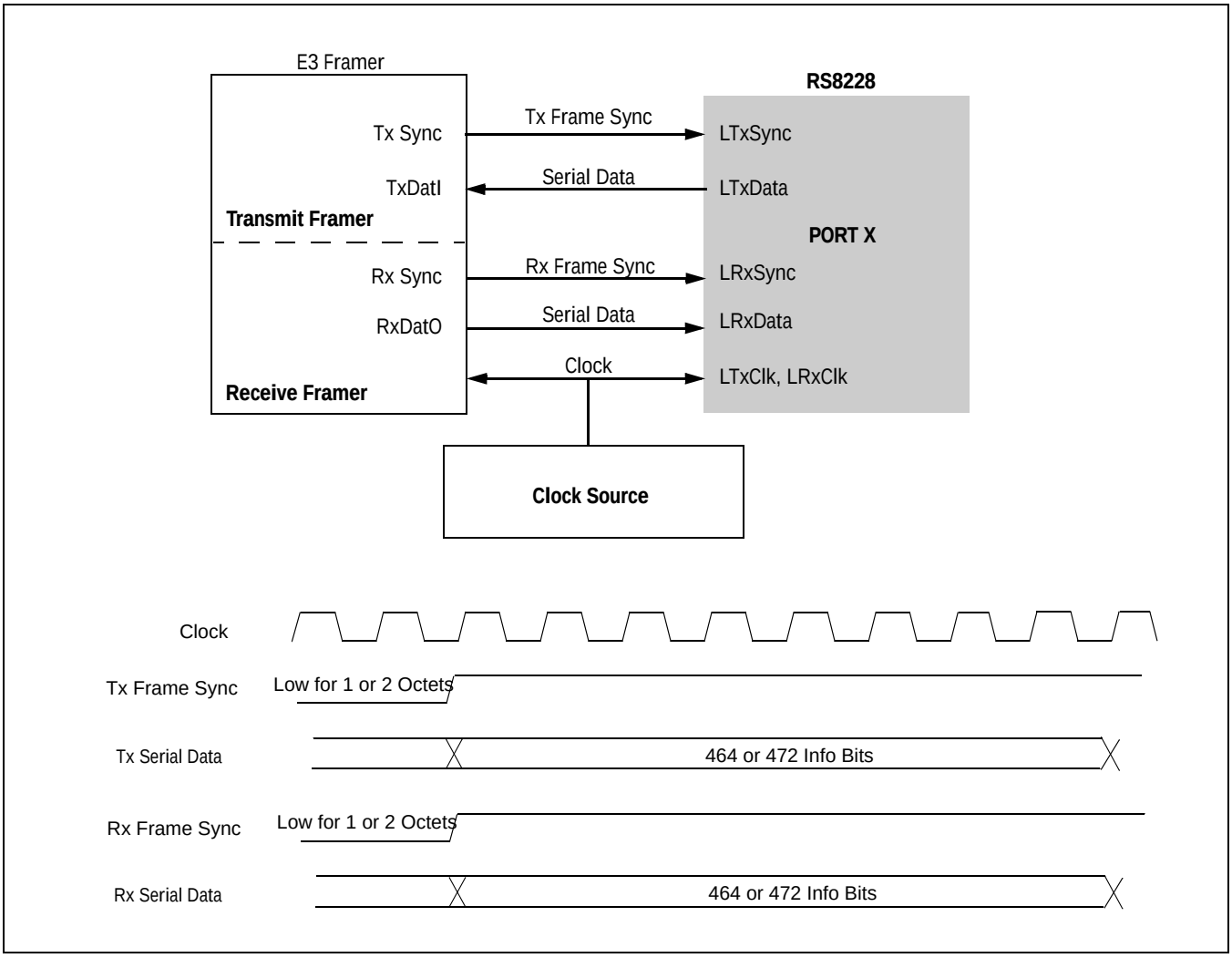


NOTE(S): In DS3 mode, ATM cells are mapped into the 84 information bits (subframe). There are seven subframes per multiframe, which is equal to 4760 bits – 56 overhead bits.

2.2.3 E3/G.832 34.368 Mbps Interface

The RS8228 interfaces directly to an E3 framer, as illustrated in Figure 2-7. The RS8228 receives a data stream from the external framer, extracts the ATM cells, ignores the overhead bytes, and passes the ATM cells to the ATM layer device. The RS8228 performs the inverse process on transmitted data.

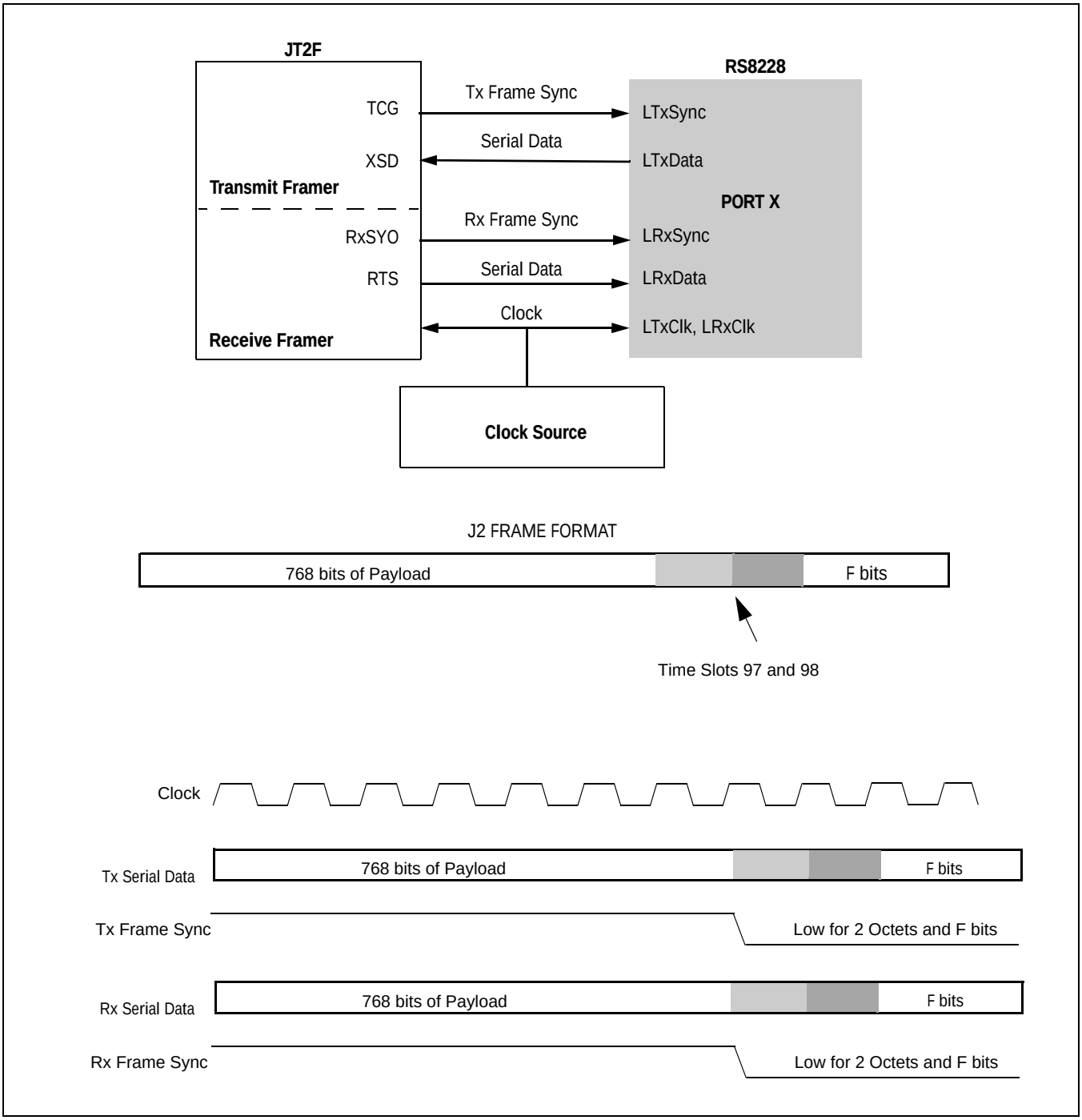
Figure 2-7. E3/G.832 36,368 kbps Diagram



2.2.4 J2 6.312 Mbps Interface

The RS8228 interfaces directly to a J2 framer, as illustrated in Figure 2-8. The RS8228 receives a data stream from the external framer, extracts the ATM cells, ignores the overhead bytes, and passes the ATM cells to the ATM layer device. The RS8228 performs the inverse process on transmitted data. The ATM cell is mapped into bits 1–768 (time slots 1–96) of the 6312 kbps frame.

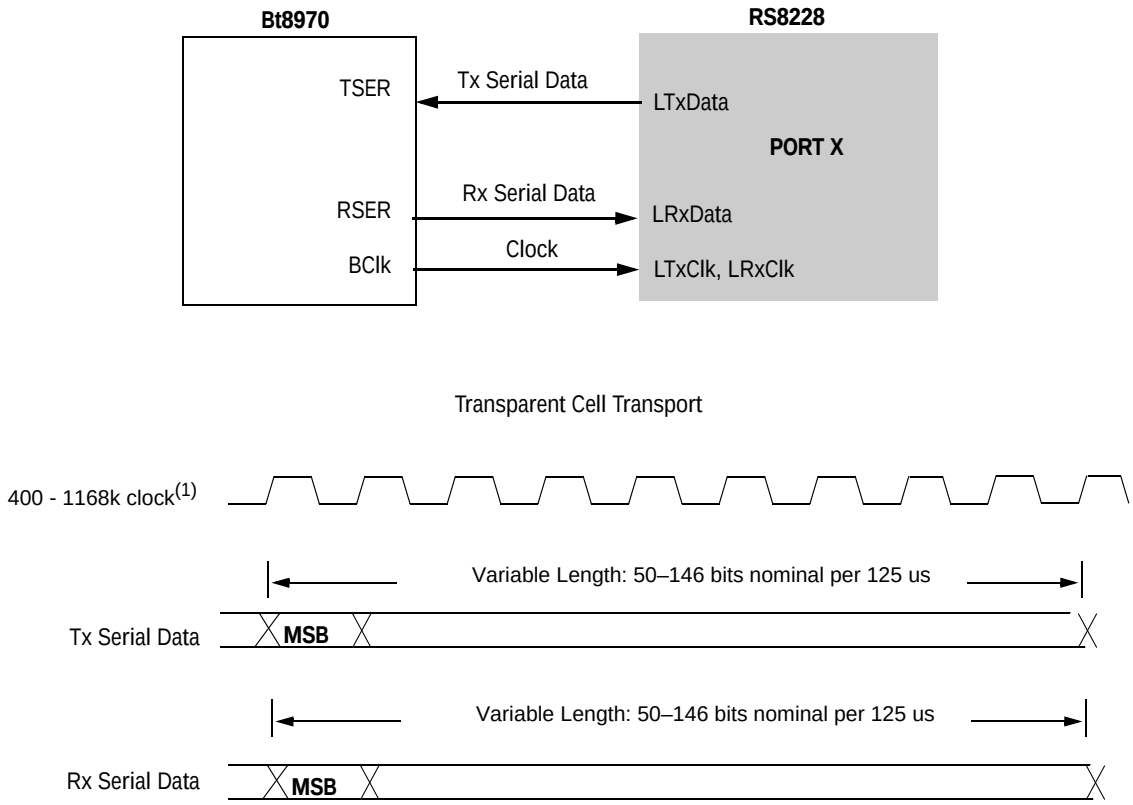
Figure 2-8. J2 6312 kbps Diagram



2.2.5 General Purpose Mode Interface

The RS8228 has a general purpose mode interface as illustrated in Figure 2-9. This mode allows connection with framers that do not provide frame
synchronization. The RS8228 receives a data stream from the external framer, performs byte-alignment and cell delineation, and passes the ATM cells to the ATM layer device. The RS8228 performs the inverse process on transmitted data. In this mode, the framer must ensure that only ATM cells are present in the data stream.

Figure 2-9. General Purpose Mode



NOTE(S):

(1) The 1168 kbps limit is imposed by the Bt8970; the RS8228 operates at data rates from 2400 bps to 51 Mbps.

(2) LRxSync and LTxSync must be tied to the appropriate voltage level as determined by the value of RxMrkPol and TxMrkPol, bits 6 and 4, in the IOMODE register (0x05).

2.3 UTOPIA Interface

The RS8228 uses the ATM Forum's UTOPIA interface as its host interface to communicate with the ATM layer device. This interface is UTOPIA Level 2-compliant and UTOPIA Level 1-compatible. In brief, these two specifications are described as follows:

UTOPIA Level 1: This is an 8- or 16-bit interface designed for data rates up to 200 Mbps. Both octet-level and cell-level handshaking are supported at a clock rate of 25 MHz. Octet-level handshaking requires the PHY to guarantee the acceptance of at least 4 bytes before it asserts the TxFull control line. In cell-level, it must guarantee the transfer of at least one entire 53-byte cell.

UTOPIA Level 2: This interface provides all the features of Level 1, plus several enhancements. Level 2 defines multi-PHY functionality, allowing up to 31 PHYs to interface to one ATM layer device. This interface uses either 8-bit or 16-bit wide data buses and cell-level handshaking. The 16-bit mode, which can run at 50 MHz, supports data rates up to 800 Mbps.

2.3.1 UTOPIA Transmit and Receive FIFOs

The RS8228's UTOPIA block has two sections, transmit and receive, each of which has a 4-cell FIFO buffer. ATM cell data is placed in the transmit FIFOs where it can then be passed to the ATM cell processing block. On the receive side of the UTOPIA interface, incoming cells are placed in the receive FIFO until sent.

NOTE: *By convention, data being transferred from the PHY to the ATM layer is labelled received data, while data from the ATM layer to the PHY is called transmitted data.*

2.3.2 UTOPIA 8-bit and 16-bit Bus Widths

The RS8228 has two bus width options, 8-bit or 16-bit, which are selected in BusWidth, bit 2, of the MODE register (0x0202). The protocols and timing are the same in both modes, except that 8-bit mode uses only the lower half of the data bus (TxData[7:0] and RxData[7:0]) and parity is only generated or checked over those bits.

In 8-bit mode, each ATM cell consists of 53 bytes, as listed in Table 2-3. The first five bytes are used for header information. The remaining bytes are used for payload.

Table 2-3. Cell Format for 8-bit Mode

Bit 7	…	Bit 0
Header 1		
Header 2		
Header 3		
Header 4		
UDF1 (HEC) (byte 5)		
Payload 1		
⋮		
Payload 48		

In 16-bit mode, the cells consists of 54 bytes, as listed in Table 2-4. The first five bytes contain header information. The sixth byte, UDF2, is required to maintain alignment but is not read by the RS8228. The remaining bytes are used for payload.

Table 2-4. Cell Format for 16-bit Mode

Bit 15 … Bit 8	Bit7 … Bit 0
Header 1	Header 2
Header 3	Header 4
UDF1 (HEC) (byte 5)	UDF2 (0) (byte 6)
Payload 1	Payload 2
⋮	⋮
Payload 47	Payload 48

NOTE: *Normally, the HEC is calculated by the PHY and put in byte 5, UDF1. However, setting bit 7 of the CGEN register (0x08) to 1 will disable HEC calculation. In this case, data inserted by the ATM layer into byte 5 is transmitted by the PHY.*

2.3.3 UTOPIA Parity

The RS8228 supports even and odd parity, which is selected by OddEven, bit 2, in the UTOP1 register (0x0D). The parity on received data is generated for either eight bits or 16 bits, according to the selected bus width in bit 0 of the MODE register (0x0202). The result is output on URxPrty (pin V14).

Likewise, the parity on transmitted data is checked for either eight bits or 16 bits, according to the selected bus width. The calculated result should match the bit present on UTxPrty (pin W11). If it does not match, a parity error has occurred. This error can be observed either in the ParErr bit (bit 7) in the TXCELL register (0x2E) or in the ParErrInt bit (bit 7) in the TXCELLINT register (0x2C). Systems that do not use parity should disable the generation of interrupts caused by parity errors by writing bit 7 of the ENCELLT register (0x28) to 0.

2.3.4 UTOPIA Multi-PHY Operation

The RS8228 supports multi-PHY operation as described in the UTOPIA Level specification (af-phy-0039.000, see http://www.atmforum.com). Three primary functions are involved in this operation: polling, selection, and data transfer. These functions are basically the same for both the transmit and receive sides of the UTOPIA bus. The following example describes the transmit functions.

The ATM layer UTOPIA controller polls the connected PHY ports by transmitting the port addresses on the UTxAddr lines. If a port is ready to transfer data, it asserts UTxClAv. The controller determines which port is to transfer data and selects that port by transmitting its address. The controller then asserts UTxEnb~ to allow the PHY to transfer data on the UTxData lines. UTxEnb~ is deasserted when the transfer is completed. Polling can continue during the data transfer process but not during port selection. It operates independently of the state of UTxEnb~.

To pause the data transfer, UTxEnb~ can be deasserted. To continue the transfer, the controller must reselect the port by transmitting its address one clock cycle before asserting UTxEnb~. The controller must ensure that the cell transfer from this port has been completed, to avoid a start-of-cell error.

The RS8228 has a UTOPIA receiver output disable feature which allows the user to set up redundant or back-up PHYs with the same UTOPIA address on the same UTOPIA bus. In this setup, both PHYs' transmitters are enabled, sending out identical data streams. Both PHYs' receivers are enabled, but only one is transferring data to the ATM device. The receiver output is disabled in the backup PHY by writing the UtopRxDis, bit 5, in the UTOP2 register (0x0E) to a logical 1. This disable places five of the backup PHY's signals, URxData, URxPrty, URxSOC, URxClAv, and UTxClAv, in a high-impedance state, preventing data and control signals from being passed to the ATM layer device. The disabled receiver will flush its FIFOs at the same rate as the enabled one, but all data it has received, except the last four cells, will be lost. Should the primary PHY device encounter an unacceptable error rate, software can quickly enable the backup PHY and disable the primary PHY, reducing cell loss in the transition.

NOTE: *To facilitate multi-PHY operation, the RS8228 assigns a different address to each of its eight ports by default.*

2.3.5 UTOPIA Addressing

The UTOPIA address for each port is stored in bits 0–4 of the UTOP2 register (0x0E). The default for this value is the port number. For example, the UTOP2 register for port 4 (0x10E [with the offset]) defaults to 04 hex. However, the value can be changed to any value from 00–1E hex by programming the register to accommodate multiple devices on the same UTOPIA bus. The value 1F hex is reserved for the null address. The UTOPIA address should be changed only when the device or port is in the reset state.

UTOPIA bus conflicts can occur if different RS8228 ports are programmed with the same multi-PHY address. Under these circumstances, a bus conflict may occur if data is being transferred through these ports at the same time. A bus conflict will generate an error in BusCnflct (bit 2) of the TXCELL register (0x2E). During a data collision, data will be transmitted according to port priority; the lowest port number has highest priority.

2.3.6 Handshaking

The RS8228 provides both cell-level and octet-level handshaking on its UTOPIA interface (only cell-level is used in Level 2). Octet-level sends and receives four octets at a time, while cell-level sends and receives a full cell at a time, depending on FIFO size and availability. In octet-level handshaking, UTxClAv is an active low, FIFO full indicator. In cell-level, it is an active high, cell buffer available indicator. These two options are selectable in the Handshake bit, bit 1, of the MODE register (0x0202).

TxCIAv (transmit cell available): The RS8228 implementation of TxCIAv is designed to provide a "look ahead" feature to allow the ATM layer to anticipate when the FIFOs will be full. The UTOPIA layer polls the port to determine if that port has room for a cell. In response, the port will assert (logic1) the TxCIAv line if it has room and will de-assert (0) the line if it does not have room. The threshold is controlled by bits [1:0] in the UTOP1 register. For maximum performance when using a standard ATM layer device, Conexant recommend leaving these set to 0s.

0 0	The TxCIAv line will be asserted if the UTOPIA FIFO can accept at least 1 more complete cell
0 1	The TxCIAv line will be asserted only if the UTOPIA FIFO has room for at least 2 more cell.
0 1	The TxCIAv line will be asserted only if the UTOPIA FIFO has room for at least 3 more cells.
1 1	The TxCIAv line will be asserted only if the UTOPIC FIFO can accept at least 3 more cells.

2.4 Microprocessor Interface

The microprocessor interface transfers control and status information in 8-bit data transfers between the external microprocessor and RS8228 by means of write and/or read access to internal registers. This interface allows the microprocessor to configure the RS8228 by writing various control registers. These control registers can also be read for configuration confirmation. This interface also provides the ability to read the device's current condition via its status registers and counters. Summary status is available for rapid interrupt identification.

The microprocessor interface can operate in either an asynchronous mode or a synchronous mode. The MSyncMode pin (pin B18) determines which mode is active.

For the asynchronous mode, the microprocessor interface pins are defined as follows: MClk, MCs~, MRd~, MWr~, MInt~, MAddr, MData. In this mode, the MRd~ and MWr~ strobes direct the data transfers.

For the synchronous mode, the microprocessor interface pins are defined as follows: MClk, MCs~, MW/R~, MAs~, MInt~, MAddr, MData. In this mode, the timing of these signals is synchronized to MClk, which is intended to be directly driven by the external microprocessor. The synchronous interface is compatible with the Bt8230 and Bt8233 SAR devices, providing no-wait-state operation.

2.4.1 Resets

There are four reset functions, two at the device level and two at the port level. The two levels allow a user to reset either the entire RS8228 with one command or only a port within the device. The two logic resets allow the user to keep the device or port in a reset state while the control registers are being programmed. When the reset bit is deasserted, all changes to the registers take place simultaneously.

At the device level, the software-controlled DevMstRst, bit 7, in the MODE register (0x0202), restarts all device functions and sets the control and status registers to their default values except this bit (DevMstRst). The DevLgcRst, bit 6, in the MODE register (0x0202) restarts all device functions but leaves all control registers unaffected.

At the port level, the PrtMstRst, bit 7, in the PMODE register (0x04), restarts all port functions and sets the registers for the associated port to their default values except this bit (PrtMstRst). The PrtLgcRst, bit 6, in the PMODE register (0x04) restarts all functions but leaves the port control registers unaffected.

2.4.2 Status Pins

Each port has four user-programmable status output signals, LStatOut[0:3]. They are configured by bits 0 and 1 in the IOMODE register (0x05), as listed in Table 2-5. When the OutStat values (the bottom row of the table) are selected, the status pins reflect the value in the OutStat register, which is user programmable. The other values (first four rows in the table) are events that occur in hardware.

The activity on these pins are events that cause microprocessor register status and interrupt indications. However, the pins behave differently than the registers because they are a direct reflection of the event, whereas the register values may be latched or retimed to the microprocessor clock domain.

Table 2-5. LStatOut Configuration

StatSelect		LStatOut[3]	LStatOut[2]	LStatOut[1]	LStatOut[0]
Bit 1	Bit 0				
0	0	RcvrHld	HECCorr	HECDet	LOCD
0	1	NonMatch	IdleRcvd	CellRcvd	CellSent

Table 2-5. LStatOut Configuration

StatSelect		LStatOut[3]	LStatOut[2]	LStatOut[1]	LStatOut[0]
Bit 1	Bit 0				
1	0	RxOvfl	TxOvfl	SOCErr	ParErr
1	1	OutStat[3]	OutStat[2]	OutStat[1]	OutStat[0]

2.4.3 Counters

The RS8228 counters record events within the device. Two types of events are recorded: error events, such as Section BIP errors, and transmission events, such as transmitted ATM cells.

Counters comprised of more than one register must be accessed by reading the least significant byte (LSB) first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the LSB was read, because the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application will receive an accurate recording of all events.

2.4.4 One-second Latching

The RS8228's implementation of one-second latching ensures the integrity of the statistics being gathered by the network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIn pin (pin A18). Therefore, the data read from the statistic counters represents the same one second of real-time data, independent of network management software timing.

The RS8228 implements one-second latching for both status signals and counter values. When the EnStatLat bit (bit 5) in the MODE register (0x0202) is written to a logical 1, a read from any of the status registers returns the state of the device at the time of the previous OneSecIn pin (pin A18) assertion. When the EnCntrLat bit (bit 4) in the MODE register (0x0202) is written to a logical 1, a read from any of the counters returns the state of the device at the time of the previous OneSecIn pin (pin A18) assertion. Every second, the counter is read, moved to the latch, and the counter is cleared. The latch is cleared when read.

The OneSecIn pin is intended to be asserted at one-second intervals. This can be achieved by connecting the OneSecIn pin to the OneSecOut pin (pin C16). The OneSecOut signal is derived from the 8kHzIn pin (pin A18). This signal is asserted for one 8kHzIn period, every 8,000 8kHzIn periods. If 8kHzIn is being driven by an 8 kHz clock, the OneSecOut signal is asserted every second.

NOTE: *When latching is disabled and a counter is wider than one byte, the LSB should be read first to retain the values of the other bytes for a subsequent read.*

2.4.5 External Framer Interrupts and Chip Selects

The RS8228 interfaces directly with a maximum of eight external framers, reducing the amount of external logic and address decode circuitry. Its eight interrupt inputs (LInt~[0:7]) and eight chip select outputs (LCs[0:7]) provide this function. Furthermore, the user can program the LCs pins in CsPol, bit 2, in the IOMODE register (0x05) to be either active high or active low to match the framer's chip select input polarity.

When an external framer generates an interrupt, it asserts the associated LInt~ pin. Each LInt~ pin is mapped to a corresponding ExInt bit in the appropriate Port's SUMINT register and the interrupt is forwarded, as described in Section 2.4.6.

An LCs pin is asserted when an address within its range appears on the microprocessor address bus and the MCs~ pin is asserted. This output selects the external framer being addressed. The framer's address decoding logic further determines which specific address is being accessed. Table 2-6 lists the LCs pins and their address ranges.

Table 2-6. Chip Selects

Address Range (Hex)	Chip Select	Pin Number
1000–11FF	LCs[0]	G20
1200–13FF	LCs[1]	F20
1400–15FF	LCs[2]	F19
1600–17FF	LCs[3]	F18
1800–19FF	LCs[4]	D20
1A00–1BFF	LCs[5]	D19
1C00–1DFF	LCs[6]	D18
1E00–1FFF	LCs[7]	B20

2.4.6 Interrupts

The RS8228's interrupt indications can be classified as either single- or dual-event; a single-event interrupt is triggered by a status assertion; a dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt: When a parity error occurs on the UTOPIA transmit data bus, an interrupt is generated on ParErrInt, bit 7, in the TXCELLINT register (0x2C). This bit is cleared when read.

Dual-event interrupt: When LOCD occurs, bit 7 of the corresponding RXCELLINT register (0x0D) is set to 1. This bit is cleared when the register is read. Once cell delineation is recovered, bit 7 is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

2.0.0.1 Interrupt Routing

The RS8228 uses three levels of interrupt indications. The first level consists of receive or transmit interrupt indications, which correspond to specific events on a specific port. The second level summarizes first level interrupts and indicates framer and one-second interrupts for each port. The third level indicates which port generated an interrupt.

The first level interrupt indications are located in registers TXCELLINT and RXCELLINT for each port. Each interrupt bit in these registers can be disabled in the corresponding ENCELLR or ENCELLT register, respectively. The result is then ORed into the appropriate bit in the port's SUMINT register.

The second level consists of summary interrupt indications, located in the SUMINT register. It also includes the OneSecInt and the ExInt indications. Each interrupt bit in these registers can be disabled in the corresponding ENSUMINT register. The result is then ORed into the appropriate bit in the SUMPORT register.

The third level contains the overall interrupt indications for each port in the SUMPORT register. These bits can be disabled in the ENSUMPORT register. The result is ORed to the MInt~ pin (pin B19). The MInt~ pin can be enabled or disabled by setting the EnIntPin (bit 3) in the MODE register (0x202).

Figure 2-10 illustrates the flow chart of the interrupt generation process.

Figure 2-10. Interrupt Indication Flow Chart

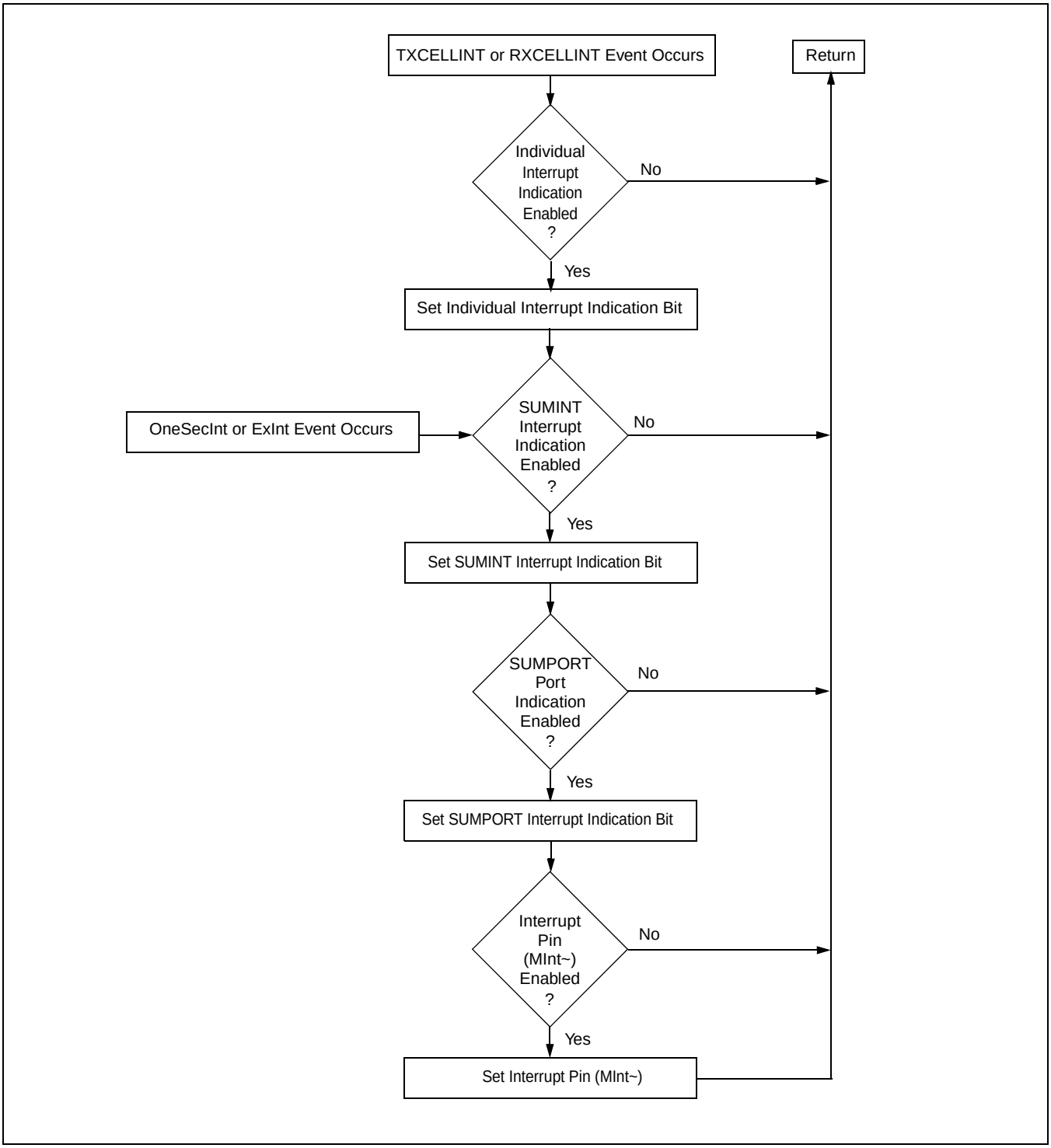
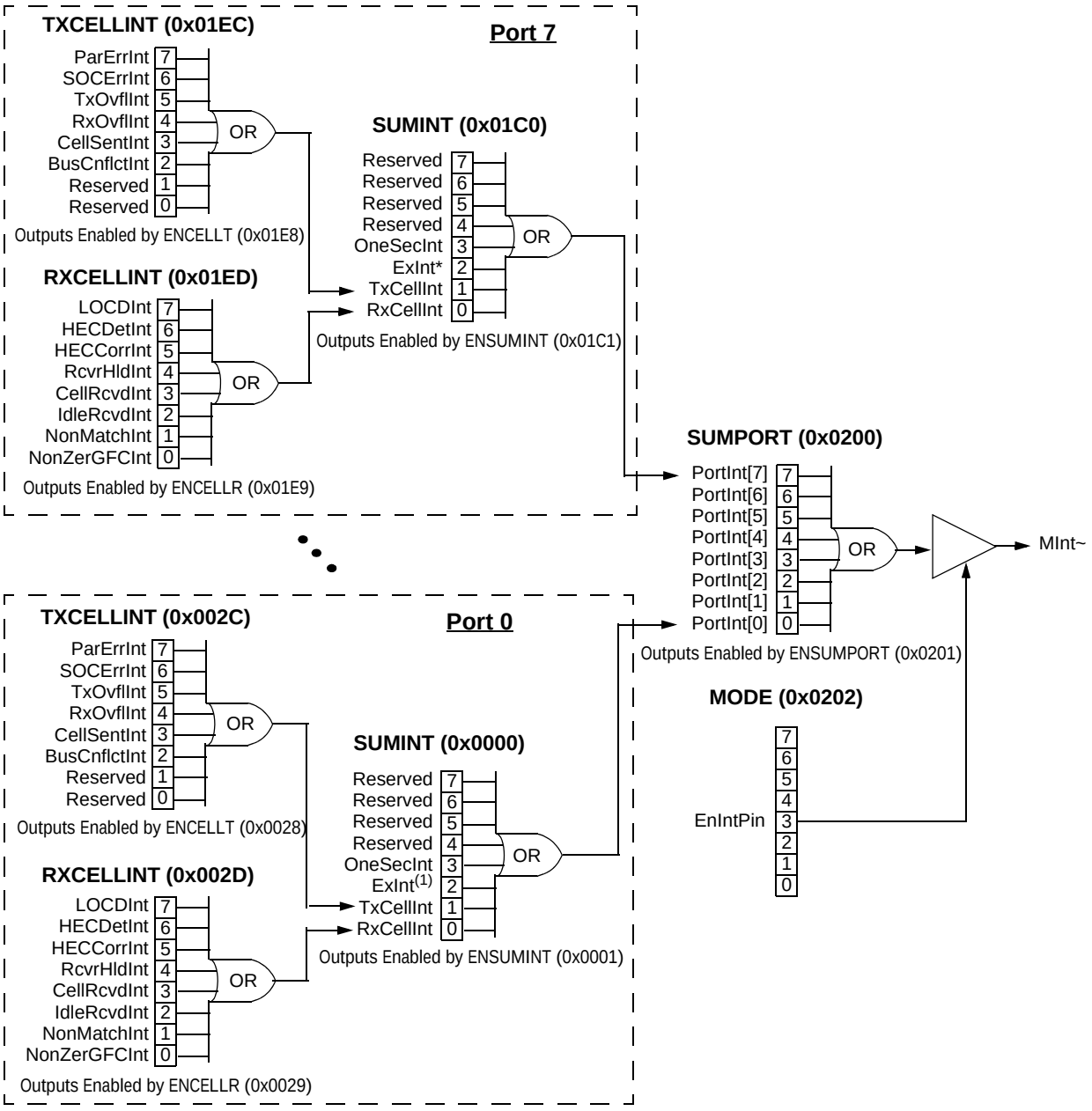


Figure 2-11 illustrates the registers involved in the interrupt generation process.

Figure 2-11. Interrupt Indication Diagram



NOTE(S):

(1) This interrupt is generated by the associated external framer.

2.4.6.1 Interrupt Servicing

When an interrupt occurs on the MInt~ pin (pin B19), it could have been generated by any of 128 events. The RS8228's interrupt indication structure ensures that no more than a maximum of three register reads are needed to determine the source of an interrupt. The interrupt is traced back to its source using the following steps:

1. Read the SUMPORT register to see which port(s) shows an interrupt.
2. Read the appropriate SUMINT register to see which bit(s) shows an interrupt.
   - Bit 0, RxCellInt, reflects activity in the RXCELLINT register.
   - Bit 1, TxCellInt, reflects activity in the TXCELLINT register.
   - Bit 2, ExInt, indicates an interrupt from an external framer.
   - Bit 3, OneSecInt, indicates a one-second interrupt.
   - Bits 4–7 are reserved.
3. If necessary, read the appropriate TXCELLINT or RXCELLINT register.

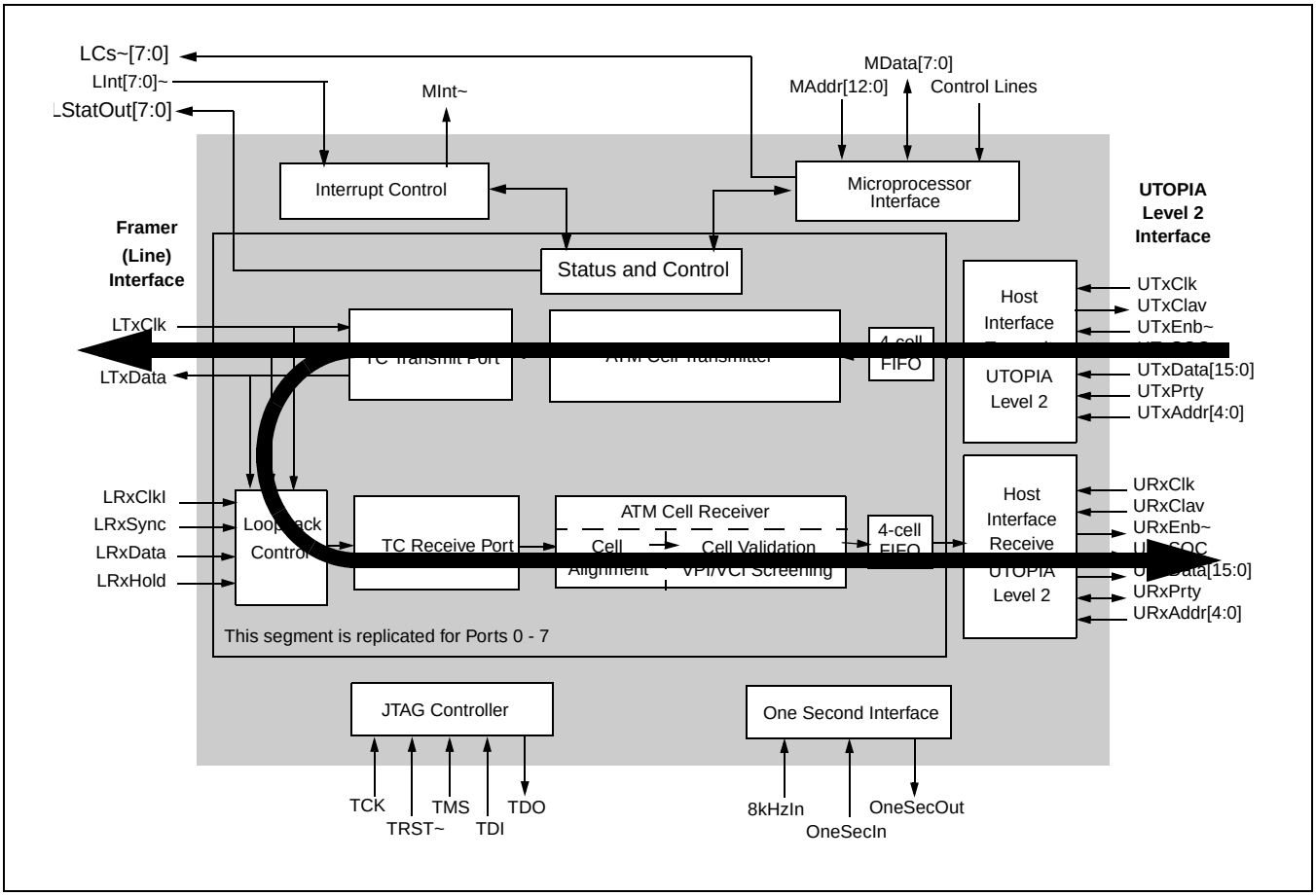
All Level 1 bits are cleared when the register is read. Once the register is read, ALL bits in that register are reset to their default values. Therefore, interrupt service routines must be designed to handle multiple interrupts in the same registers. In Level 2, OneSecInt and ExInt are cleared when the register is read. However, the TxCellInt and RxCellInt bits are cleared only when the corresponding Level 1 register is read and cleared. Level 3 bits are cleared when the entire corresponding Level 2 register has been read and cleared.

2.5 Source Loopback

Source loopback checks that the host (the ATM layer) is communicating with the PHY. It is enabled and disabled in bit 5 of the PMODE register (0x04). When source loopback is enabled for a given port, all data transmitted by the RS8228 on that port is also looped back through the Receive Line Interface. Data from the framer interface is ignored.

NOTE: *LTxClk, LRxClk, LTxSync, and LRxSync must be present for the loopback mode to function properly for a given port.*

Figure 2-12. Source Loopback Diagram



3.0 Registers

The RS8228 registers control and observe the device's operations. Table 3-1 lists the address ranges that represent a device control and status range, along with eight port ranges and eight framer ranges. Three registers make up the device-level range. The registers in each port range are replicated for the other ports. Table 3-2 lists the device-level control and status registers. Table 3-3 lists the port-level control and status registers. All registers are 8 bits wide. All control registers can be read to verify contents. There are 13 primary address pins, MAddr[12:0] (pins P18–P20, N18–N20, M18–M20, L18–L20, and K20), which resolve to 8192 address locations.

NOTE: *Control bits that do not have a documented function are reserved and must be written to a logical 0.*

Table 3-1. Address Ranges

Port Offset Address Range (Hex)	Description	Port Base Address (Hex)
0000–003F	Port 0 Control and Status Registers	0000
0040–007F	Port 1 Control and Status Registers	0040
0080–00BF	Port 2 Control and Status Registers	0080
00C0–00FF	Port 3 Control and Status Registers	00C0
0100–013F	Port 4 Control and Status Registers	0100
0140–017F	Port 5 Control and Status Registers	0140
0180–01BF	Port 6 Control and Status Registers	0180
01C0–01FF	Port 7 Control and Status Registers	01C0
0200–0202	Device Control and Status Registers	—
0203–0FFF	Reserved, set to a logical 0.	—
1000–11FF	Framer 0 Address Range, LCs[0]	—
1200–13FF	Framer 1 Address Range, LCs[1]	—
1400–15FF	Framer 2 Address Range, LCs[2]	—
1600–17FF	Framer 3 Address Range, LCs[3]	—
1800–19FF	Framer 4 Address Range, LCs[4]	—
1A00–1BFF	Framer 5 Address Range, LCs[5]	—
1C00–1DFF	Framer 6 Address Range, LCs[6]	—
1E00–1FFF	Framer 7 Address Range, LCs[7]	—

The device level registers in Table 3-2 provide control for the device's major operating modes, as well as status and control for summary interrupts.

Table 3-2. Device Control and Status Registers

Address	Name	Type	OneSec Latching	Description	Page Number
0x0200	SUMPORT	R	—	Summary Port Interrupt Status Register	page 36
0x0201	ENSUMPORT	R/W	—	Summary Port Interrupt Control Register	page 37
0x0202	MODE	R/W	—	Device Mode Control Register	page 37

The registers listed in Table 3-3 are replicated for each port. Two methods can be used to determine the exact address of a specific register in a specific port. All numbers are in hexadecimal.

1. Add the port offset address to the port base address as shown in Table 3-1. For example:
   For Port 3, IOMODE register
   00C0 (Port 3 base address) + 0x05 (port offset address) = 00C5
2. Use the following formula:
   0x40 (port register map size) × *n* (port number) + port offset address = exact register address

Table 3-3. Port Control and Status Registers *(1 of 3)*

Port Offset Address	Name	Type	One-second Latching	Description	Page Number
0x00	SUMINT	R	—	Summary Interrupt Status Register	page 8
0x01	ENSUMINT	R/W	—	Summary Interrupt Control Register	page 9
0x02	—	—	—	Reserved, set to a logical 0	—
0x03	—	—	—	Reserved, set to a logical 0	—
0x04	PMODE	R/W	—	Port Mode Control Register	page 10
0x05	IOMODE	R/W	—	Input/Output Mode Control Register	page 11
0x06	VERSION	R	—	Part Number/Version Status Register	page 12
0x07	OUTSTAT	R/W	—	Output Pin Control Register	page 12
0x08	CGEN	R/W	—	Cell Generation Control Register	page 13
0x09	HDRFIELD	R/W	—	Header Field Control Register	page 13
0x0A	IDLPAY	R/W	—	Transmit Idle Cell Payload Control Register	page 14
0x0B	ERRPAT	R/W	—	Error Pattern Control Register	page 14
0x0C	CVAL	R/W	—	Cell Validation Control Register	page 15
0x0D	UTOP1	R/W	—	UTOPIA Control Register 1	page 16
0x0E	UTOP2	R/W	—	UTOPIA Control Register 2	page 17
0x0F	—	—	—	Reserved, set to a logical 0	—
0x10	TXHDR1	R/W	—	Transmit Cell Header Control Register 1	page 17
0x11	TXHDR2	R/W	—	Transmit Cell Header Control Register 2	page 18

Table 3-3. Port Control and Status Registers (2 of 3)

Port Offset Address	Name	Type	One-second Latching	Description	Page Number
0x12	TXHDR3	R/W	—	Transmit Cell Header Control Register 3	page 18
0x13	TXHDR4	R/W	—	Transmit Cell Header Control Register 4	page 19
0x14	TXIDL1	R/W	—	Transmit Idle Cell Header Control Register 1	page 19
0x15	TXIDL2	R/W	—	Transmit Idle Cell Header Control Register 2	page 20
0x16	TXIDL3	R/W	—	Transmit Idle Cell Header Control Register 3	page 20
0x17	TXIDL4	R/W	—	Transmit Idle Cell Header Control Register 4	page 21
0x18	RXHDR1	R/W	—	Receive Cell Header Control Register 1	page 21
0x19	RXHDR2	R/W	—	Receive Cell Header Control Register 2	page 22
0x1A	RXHDR3	R/W	—	Receive Cell Header Control Register 3	page 22
0x1B	RXHDR4	R/W	—	Receive Cell Header Control Register 4	page 23
0x1C	RXMSK1	R/W	—	Receive Cell Mask Control Register 1	page 23
0x1D	RXMSK2	R/W	—	Receive Cell Mask Control Register 2	page 24
0x1E	RXMSK3	R/W	—	Receive Cell Mask Control Register 3	page 24
0x1F	RXMSK4	R/W	—	Receive Cell Mask Control Register 4	page 25
0x20	RXIDL1	R/W	—	Receive Idle Cell Header Control Register 1	page 25
0x21	RXIDL2	R/W	—	Receive Idle Cell Header Control Register 2	page 26
0x22	RXIDL3	R/W	—	Receive Idle Cell Header Control Register 3	page 26
0x23	RXIDL4	R/W	—	Receive Idle Cell Header Control Register 4	page 27
0x24	IDLMSK1	R/W	—	Receive Idle Cell Mask Control Register 1	page 27
0x25	IDLMSK2	R/W	—	Receive Idle Cell Mask Control Register 2	page 28
0x26	IDLMSK3	R/W	—	Receive Idle Cell Mask Control Register 3	page 28
0x27	IDLMSK4	R/W	—	Receive Idle Cell Mask Control Register 4	page 29
0x28	ENCELLT	R/W	—	Transmit Cell Interrupt Control Register	page 29
0x29	ENCELLR	R/W	—	Receive Cell Interrupt Control Register	page 30
0x2A	—	—	—	Reserved, set to a logical 0	—
0x2B	—	—	—	Reserved, set to a logical 0	—
0x2C	TXCELLINT	R	—	Transmit Cell Interrupt Indication Control Register	page 30
0x2D	RXCELLINT	R	—	Receive Cell Interrupt Indication Control Register	page 31
0x2E	TXCELL	R	(1)	Transmit Cell Status Control Register	page 31
0x2F	RXCELL	R	(1)	Receive Cell Status Control Register	page 32
0x30	LOCDCNT	R	(2)	LOCD Event Counter	page 32
0x31	CORRCNT	R	(2)	Corrected HEC Error Counter	page 33

***Table 3-3. Port Control and Status Registers** (3 of 3)*

Port Offset Address	Name	Type	One-second Latching	Description	Page Number
0x32	UNCCNT	R	(2)	Uncorrected HEC Error Counter	page 33
0x33	—	—	—	Reserved, set to a logical 0	—
0x34	TXCNTL	R	(2)	Transmitted Cell Counter (low byte)	page 33
0x35	TXCNTM	R	(2)	Transmitted Cell Counter (mid byte)	page 34
0x36	TXCNTH	R	(2)	Transmitted Cell Counter (high byte)	page 34
0x37	—	—	—	Reserved, set to a logical 0	—
0x38	RXCNTL	R	(2)	Received Cell Counter (low byte)	page 34
0x39	RXCNTM	R	(2)	Received Cell Counter (mid byte)	page 35
0x3A	RXCNTH	R	(2)	Received Cell Counter (high byte)	page 35
0x3B	—	—	—	Reserved, set to a logical 0	—
0x3C	NONCNTL	R	(2)	Non-Matching Cell Counter (low byte)	page 35
0x3D	NONCNTH	R	(2)	Non-Matching Cell Counter (high byte)	page 36
0x3E	—	—	—	Reserved, set to a logical 0	—
0x3F	—	—	—	Reserved, set to a logical 0	—

NOTE(S):
(1) One-second latching is enabled by setting EnStatLat (bit 5) in the MODE register (0x0202) to a logical 1.
(2) One-second latching is enabled by setting EnCntrLat (bit 4) in the MODE register (0x0202) to a logical 1.

Table 3-4 lists several registers used for RS8228's basic functions, including device- and port-level operating modes.

Table 3-4. General Use Registers

Port Offset Address	Name	Description	Page Number
0x0202	MODE	Device Mode Control Register	page 37
0x04	PMODE	Port Mode Control Register	page 10
0x05	IOMODE	Input/Output Mode Control Register	page 11
0x06	VERSION	Part Number/Version Status Register	page 12
0x07	OUTSTAT	Output Pin Control Register	page 12

Table 3-5 lists the control registers used for transmission of traffic.

Table 3-5. Cell Transmit Registers

Port Offset Address	Name	Description	Page Number
0x08	CGEN	Cell Generation Control Register	page 13
0x09	HDRFIELD	Header Field Control Register	page 13
0x0A	IDLPAY	Transmit Idle Cell Payload Control Register	page 14
0x0B	ERRPAT	Error Pattern Control Register	page 14
0x10	TXHDR1	Transmit Cell Header Control Register 1	page 17
0x11	TXHDR2	Transmit Cell Header Control Register 2	page 18
0x12	TXHDR3	Transmit Cell Header Control Register 3	page 18
0x13	TXHDR4	Transmit Cell Header Control Register 4	page 19
0x14	TXIDL1	Transmit Idle Cell Header Control Register 1	page 19
0x15	TXIDL2	Transmit Idle Cell Header Control Register 2	page 20
0x16	TXIDL3	Transmit Idle Cell Header Control Register 3	page 20
0x17	TXIDL4	Transmit Idle Cell Header Control Register 4	page 21

Table 3-6 lists the control registers used for reception of traffic.

Table 3-6. Cell Receive Registers

Port Offset Address	Name	Description	Page Number
0x0C	CVAL	Cell Validation Control Register	page 15
0x18	RXHDR1	Receive Cell Header Control Register 1	page 21
0x19	RXHDR2	Receive Cell Header Control Register 2	page 22
0x1A	RXHDR3	Receive Cell Header Control Register 3	page 22
0x1B	RXHDR4	Receive Cell Header Control Register 4	page 23
0x1C	RXMSK1	Receive Cell Mask Control Register 1	page 23
0x1D	RXMSK2	Receive Cell Mask Control Register 2	page 24
0x1E	RXMSK3	Receive Cell Mask Control Register 3	page 24
0x1F	RXMSK4	Receive Cell Mask Control Register 4	page 25
0x20	RXIDL1	Receive Idle Cell Header Control Register 1	page 25
0x21	RXIDL2	Receive Idle Cell Header Control Register 2	page 26
0x22	RXIDL3	Receive Idle Cell Header Control Register 3	page 26
0x23	RXIDL4	Receive Idle Cell Header Control Register 4	page 27
0x24	IDLMSK1	Receive Idle Cell Mask Control Register 1	page 27
0x25	IDLMSK2	Receive Idle Cell Mask Control Register 2	page 28

Table 3-6. Cell Receive Registers

Port Offset Address	Name	Description	Page Number
0x26	IDLMSK3	Receive Idle Cell Mask Control Register 3	page 28
0x27	IDLMSK4	Receive Idle Cell Mask Control Register 4	page 29

Table 3-7 lists the control registers for the UTOPIA operations.

Table 3-7. UTOPIA Registers

Port Offset Address	Name	Description	Page Number
0x0D	UTOP1	UTOPIA Control Register 1	page 16
0x0E	UTOP2	UTOPIA Control Register 2	page 17

Table 3-8 lists interrupt enables, interrupt indications, and status information.

Table 3-8. Status and Interrupt Registers

Port Offset Address	Name	Description	Page Number
0x0200	SUMPORT	Summary Port Interrupt Status Register	page 36
0x0201	ENSUMPORT	Summary Port Interrupt Control Register	page 37
0x00	SUMINT	Summary Interrupt Indication Status Register	page 8
0x01	ENSUMINT	Summary Interrupt Control Register	page 9
0x28	ENCELLT	Transmit Cell Interrupt Control Register	page 29
0x29	ENCELLR	Receive Cell Interrupt Control Register)	page 30
0x2C	TXCELLINT	Transmit Cell Interrupt Indication Status Register	page 30
0x2D	RXCELLINT	Receive Cell Interrupt Indication Status Register	page 31
0x2E	TXCELL	Transmit Cell Status Register	page 31
0x2F	RXCELL	Receive Cell Status Register	page 32

Table 3-9 lists the RS8228's counters. When the counters fill, they saturate and do not roll over. The counts have been sized to ensure against saturation within a one-second interval. Therefore, when one-second latching is enabled, the counters are read and cleared before they can saturate. All counters are cleared when read.

Table 3-9. Counters

Port Offset Address	Name	Description	Page Number
0x30	LOCDCNT	LOCD Event Counter	page 32
0x31	CORRCNT	Corrected HEC Error Counter	page 33
0x32	UNCCNT	Uncorrected HEC Error Counter	page 33
0x34	TXCNTL	Transmitted Cell Counter [Low Byte])	page 33
0x35	TXCNTM	Transmitted Cell Counter [Mid Byte]	page 34
0x36	TXCNTH	Transmitted Cell Counter [High Byte]	page 34
0x38	RXCNTL	Received Cell Counter [Low Byte]	page 34
0x39	RXCNTM	Received Cell Counter [Mid Byte]	page 35
0x3A	RXCNTH	Received Cell Counter [High Byte]	page 35
0x3C	NONCNTL	Non-matching Cell Counter [Low Byte]	page 35
0x3D	NONCNTH	Non-matching Cell Counter [High Byte]	page 36

0x00—SUMINT (Summary Interrupt Indication Status Register)

The SUMINT register indicates the one-second interrupts, external framer interrupts, and port summary interrupts.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	—	OneSecInt(1)	When a logical 1 is read, this bit indicates a One Second Interrupt. This interrupt signifies that a rising edge occurred on the OneSecIn pin (pin A17). This interrupt is generated for each rising edge on the OneSecIn pin.
2	—	ExInt(2)	When a logical 1 is read, this bit indicates an active External Interrupt on the LInt~ pin (pins G19, G18, E18, E19, E20, C18, C19, or C20).
1	—	TxCellInt(3)	When a logical 1 is read, this bit indicates a Transmit Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the TxCellInt register (0x2C).
0	—	RxCellInt(3)	When a logical 1 is read, this bit indicates a Receive Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the RxCellInt register (0x2D).

NOTE(S):

(1) This bit is cleared when this register is read in any of the eight ports.

(2) Single event—A 1 to 0 transition on the corresponding pin causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

(3) This bit is a summary indication of any interrupt events that occurred in the indicated registers. This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bits in the corresponding interrupt indication registers are read and automatically cleared.

0x01—ENSUMINT (Summary Interrupt Control Register)

The ENSUMINT register controls which of the interrupts listed in the SUMINT register (0x00) appear in the SUMPORT register and on the MInt~ (pin B19), provided the corresponding ENSUMPORT bit is enabled and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	1	EnOneSecInt	When written to a logical 1, this bit enables the one-second interrupt generated by the OneSecIn pin (pin A17) to appear on the MInt~ output pin (pin B19).
2	1	EnExtInt	When written to a logical 1, this bit enables the External Interrupt to appear on the MInt~ pin (pin B19), provided that EnPortInt in the ENSUMPORT register (0x0201) is enabled for this port.
1	1	EnTxCellInt	When written to a logical 1, this bit enables the transmit cell interrupts located in the TxCellInt register (0x2C). These interrupts appear can on the MInt~ pin (pin B19), provided that EnPortInt in the ENSUMPORT register (0x0201) is enabled for this port and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.
0	1	EnRxCellInt	When written to a logical 1, this bit enables the receive cell interrupts located in the RxCellInt register (0x2D). These interrupts can appear on the MInt~ pin (pin B19), provided that EnPortInt in the ENSUMPORT register (0x0201) is enabled for this port and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

0x04—PMODE (Port Mode Control Register)

The PMODE register controls the port-level software resets, source loopback, and physical layer interface mode.

Bit	Default	Name	Description
7	0	PrtMstRst	When written to a logical 1, this bit initiates a Port Master Reset. All internal state machines associated with this port are reset and all control registers for this port, except this one, assume their default values. Only bits 0–6 in this register are overwritten with their default values.
6	0	PrtLgcRst	When written to a logical 1, this bit initiates a Port Logic Reset. All internal state machines associated with this port are reset but all registers (0x00–0x3F) listed as “Type: W/R” in Table 3-3 are unaltered.
5	0	SrcLoop[1]	When written to a logical 1, this bit enables a source loopback. The line transmit clock and data outputs are connected to the line receive clock and data inputs.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	0	PhyType[2](1)	These bits determine the Physical Layer Interface Mode: 000 - T1 mode 001 - E1 mode 010 - DS3 mode 011 - E3 mode (G.832) 100 - J2 mode 101 - General Purpose 110 - Reserved, do not use 111 - Power Down
1	0	PhyType[1](1)	
0	0	PhyType[0](1)	

NOTE(S):
(1) These bits should only be changed when the device or port logic reset is asserted.

0x05—IOMODE (Input/Output Mode Control Register)

The IOMODE register controls the line interface signal polarities and status outputs.

Bit	Default	Name	Description
7	0	RxHldPol(1)	This bit programs the polarity of the corresponding LRxHld input. Set this bit to 1 for active high input and to 0 for active low input. Tie the LRxHld pin to 3.3 V for default operation. Most systems can ignore this bit and input pin.
6	0	RxSyncPol(1)	This bit programs the polarity of the corresponding LRxSync input. Set this bit to 1 for active high input and to 0 for active low input. Tie the LRxSync pin to 3.3 V for default operation. Most systems can ignore this bit and input pin.
5	0	RxClkPol	This bit determines the Receiver Clock Input Polarity. Set this bit to 1 to sample the Receive data on the falling edge of the RxClk input and to 0 to sample on the rising edge.
4	0	TxSyncPol(1)	This bit programs the polarity of the corresponding LTxSync input. Set this bit to 1 for active high input and to 0 for active low input. Tie the LTxSync pin to 3.3 V for default operation. Most systems can ignore this bit and input pin.
3	0	TxClkPol(1)	This bit determines the Transmitter Clock Input Polarity. Set this bit to 1 to output the Transmit data on the falling of the TxClk input and to 0 to output data on the rising edge.
2	0	CsPol(1)	This bit programs the polarity of the corresponding LCs input. Set this bit to 1 for active high input and to 0 for active low input. Tie the LCs pin to 3.3 V for default operation. Most systems can ignore this bit and input pin.
1	1	StatSel[1]	These bits indicate the output status select control: 00—RcvrHld, HECCorr, HECDet, and LOCD appear on the LStatOut[3:0] pins. 01—NonMatch, IdleRcvd, CellRcvd, and CellSent appear on the LStatOut[3:0] pins. 10—RxOvfl, TxOvfl, SOCErr, and ParErr appear on the LStatOut[3:0] pins. 11—The value in the OutStat control register (0x07) appears on the LStatOut[3:0] pins.
0	1	StatSel[0]	

NOTE(S):
(1) These bits should only be changed when the device or port logic reset is asserted.

0x06—VERSION (Part Number/Version Status Register)

The VERSION register identifies the Conexant device and its revision level.

Bit	Default	Name	Description
7	1	Part[3] - MSB	The part number that uniquely identifies the RS8228 device.
6	0	Part[2]	
5	0	Part[1]	
4	0	Part[0] - LSB	
3	0	Ver[3] - MSB	The version number that uniquely identifies the specific version of the RS8228 device. Version numbers start at 1 for the first version and are incremented for each revision thereafter. 01 - Original release. 010 - Not used. 011 - Rev B. (8228-12)
2	1	Ver[2]	
1	0	Ver[1]	
0	0	Ver[0] - LSB	

0x07—OUTSTAT (Output Pin Control Register)

The OUTSTAT register contains the values that will be reflected on the LStatOut[3:0] pins when StatSel[1:0] (bits 1 and 0) in the IOMODE register (0x05) is written to a logical 1.

Bit	Default	Name	Description
7	0	—	Reserved, write to a logical 0.
6	0	—	Reserved, write to a logical 0.
5	0	—	Reserved, write to a logical 0.
4	0	—	Reserved, write to a logical 0.
3	0	Outstat[3]	Value to be reflected to LStatOut[3] pin.
2	0	Outstat[2]	Value to be reflected to LStatOut[2] pin.
1	0	Outstat[1]	Value to be reflected to LStatOut[1] pin.
0	0	Outstat[0]	Value to be reflected to LStatOut[0] pin.

0x08—CGEN (Cell Generation Control Register)

The CGEN register controls the device's cell generation functions.

Bit	Default	Name	Description
7	0	DisHEC	When written to a logical 1, this bit disables internal generation of the HEC field. When disabled, the HEC field from the UTOPIA interface remains unchanged in the transmitted cell. When written to a logical 0, HEC is internally calculated and inserted in the transmitted cell.
6	1	EnTxCos	When written to a logical 1, this bit enables the Transmit HEC Coset. When written to a logical 0, the HEC Coset is disabled.
5	1	EnTxCellScr	When written to a logical 1, this bit enables the Transmit Cell Scrambler. When written to a logical 0, the Transmit Cell Scrambler is disabled.
4	0	ErrHEC	When written to a logical 1, this bit causes the ERRPAT register to be XORed with the calculated HEC byte for one transmit cell. These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.
3	0	—	Reserved, write to a logical 0.
2	0	—	Reserved, write to a logical 0.
1	0	EnTxDSSScr	When written to a logical 1, this bit enables the Transmit DSS Scrambler. When written to a logical 0, the Transmit DSS Scrambler is disabled.
0	0	EnRxDSSScr	When written to a logical 1, this bit enables the Receive DSS Scrambler. When written to a logical 0, the Receive DSS Scrambler is disabled.

0x09—HDRFIELD (Header Field Control Register)

The HDRFIELD register controls the header insertion elements.

Bit	Default	Name	Description
7	0	—	Reserved, write to a logical 0.
6	0	—	Reserved, write to a logical 0.
5	0	—	Reserved, write to a logical 0.
4	0	InsGFC	When written to a logical 1, this bit inserts a Generic Flow Control (GFC) field in the outgoing header from the TXHDR registers. When written to a logical 0, the GFC field is not changed prior to transmission.
3	0	InsVPI	When written to a logical 1, this bit inserts a Virtual Path Identifier (VPI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VPI field is not changed prior to transmission.
2	0	InsVCI	When written to a logical 1, this bit inserts a Virtual Channel Identifier (VCI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VCI field is not changed prior to transmission.
1	0	InsPT	When written to a logical 1, this bit inserts a Payload Type (PT) field in the outgoing header from the TXHDR registers. When written to a logical 0, the PT field is not changed prior to transmission.
0	0	InsCLP	When written to a logical 1, this bit inserts a Cell Loss Priority (CLP) bit in the outgoing header from the TXHDR registers. When written to a logical 0, the CLP field is not changed prior to transmission.

0x0A—IDLPAY (Transmit Idle Cell Payload Control Register)

The IDLPAY register contains the transmit idle cell payload.

Bit	Default	Name	Description
7	0	IdlPay[7]	These bits hold the Transmit Idle Cell Payload values for outgoing idle cells.
6	1	IdlPay[6]	
5	1	IdlPay[5]	
4	0	IdlPay[4]	
3	1	IdlPay[3]	
2	0	IdlPay[2]	
1	1	IdlPay[1]	
0	0	IdlPay[0]	

0x0B—ERRPAT (Error Pattern Control Register)

The ERRPAT register provides the error pattern for the HEC error insertion function. ErrHEC (bit 4) in the CGEN register (0x08) enables this function. Each bit in the error pattern register is XORed with the corresponding bit of the calculated HEC byte to be errored.

Bit	Default	Name	Description
7	0	ErrPat[7]	Error pattern bit 7.
6	0	ErrPat[6]	Error pattern bit 6.
5	0	ErrPat[5]	Error pattern bit 5.
4	0	ErrPat[4]	Error pattern bit 4.
3	0	ErrPat[3]	Error pattern bit 3.
2	0	ErrPat[2]	Error pattern bit 2.
1	0	ErrPat[1]	Error pattern bit 1.
0	0	ErrPat[0]	Error pattern bit 0.

0x0C—CVAL (Cell Validation Control Register)

The CVAL register controls the validation of incoming cells.

Bit	Default	Name	Description
7	0	RejHdr	When written to a logical 1, this bit enables the Rejection of certain Header cells. When enabled, cells with headers matching the RXHDRx/RXMSKx definition are rejected and all others are accepted. When written to a logical 0, cells with matching headers are accepted and cells with non-matching headers are rejected.
6	1	DelIdle	When written to a logical 1, this bit enables the Deletion of Idle Cells. When enabled, cells matching the RXIDL/IDLMSK definition are deleted from the received cell stream. When written to a logical 0, idle cells are included in the received stream.
5	1	EnRxCos	When written to a logical 1, this bit enables the Receive HEC Coset. When written to a logical 0, the HEC Coset is disabled.
4	1	EnRxCellScr	When written to a logical 1, this bit enables the Receive Cell Scrambler. When written to a logical 0, the Receive Cell Scrambler is disabled.
3	0	EnHECCorr	When written to a logical 1, this bit enables HEC Correction. When written to a logical 0, HEC Correction is disabled.
2	0	DisHECChk	When written to a logical 1, this bit disables HEC Checking. When written to a logical 0, HEC checking is performed as a cell validation criterion.
1	0	DisCellRcvr	When written to a logical 1, this bit disables the Cell Receiver. When disabled, all cell reception is disabled on the next cell boundary. When written to a logical 0, cell reception begins or resumes on the next cell boundary.
0	0	DisLOCD	When written to a logical 1, this bit disables Loss of Cell Delineation. When disabled, cells are passed even if cell delineation has not been found. When written to a logical 0, cells are passed only while cell alignment has been achieved.

0x0D—UTOP1 (UTOPIA Control Register 1)

The UTOP1 register controls the UTOPIA resets, parity orientation, and the transmit FIFO fill-level threshold.

Bit	Default	Name	Description
7	0	TxReset	When written to a logical 1, this bit resets the transmit FIFO pointers. This reset should only be used as a test function because it can create short cells.
6	0	RxReset	When written to a logical 1, this bit resets the receive FIFO pointers. This reset should only be used as a test function because it can create short cells.
5	0	—	Reserved, write to a logical 0.
4	0	—	Reserved, write to a logical 0.
3	0	—	Reserved, write to a logical 0.
2	0	OddEven(1)	This bit determines Odd/Even Parity. When written to a logical 1, even parity is generated and checked. When set to a logical 0, odd parity is generated and checked.
1	0	TxFill[1](1)	0 0 The TxCIAv line will be asserted if the UTOPIA FIFO can accept at least 1 more complete cell. 0 1 The TxCIAv line will be asserted only if the UTOPIA FIFO has room for at least 2 more cell. 0 1 The TxCIAv line will be asserted only if the UTOPIA FIFO has room for at least 3 more cells. 1 1 The TxCIAv line will be asserted only if the UTOPIC FIFO can accept at least 3 more cells.
0	0	TxFill[0](1)	

NOTE(S):
(1) These bits should only be changed when the device or port logic reset is asserted.

0x0E—UTOP2 (UTOPIA Control Register 2)

The UTOP2 register contains the multi-PHY address value for the device.

Bit	Default	Name	Description
7	0	Test 1	This is a test function, set to a logical 0.
6	0	Test 2	This is a test function, set to a logical 0.
5	0	UtopDis(1)	When written to a logical 1, this bit disables UTOPIA outputs for this port.
4	0	MphyAddr[4] - MSB(1)	These bits are the Multi-PHY Device Address. Each RS8228 port should have a unique address. These bits correspond to the URxAddr and UTxAddr pins. When the pin matches the bit values, the port is accessed. This port ignores any transactions meant for another port or PHY device.
3	0	MphyAddr[3](1)	
2	(2)	MphyAddr[2](1)	
1	(2)	MphyAddr[1](1)	
0	(2)	MphyAddr[0] - LSB(1)	

NOTE(S):
(1) These bits should only be changed when the device or port logic reset is asserted.
(2) The default for these bits is the port number for each port. (000 - Port 0, 001 - Port 1, 010 - Port 2, 011 - Port 3, 100 - Port 4, 101 - Port 5, 110 - Port 6, 111 - Port 7)

0x10—TXHDR1 (Transmit Cell Header Control Register 1)

The TXHDR1 register contains the first byte of the Transmit Cell Header. It controls the header value that is inserted in the transmitted cell. This header consists of 32 bits divided among four registers (TXHDR1–4). Cell generation is described in detail in Section 2.1.1.

Bit	Default	Name	Description
7	0	TxHdr1[7]	These bits hold the Transmit Header values for Octet 1 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). GFC/VPI bits (for UNI they are GFC bits, for NNI they are VPI bits)
6	0	TxHdr1[6]	
5	0	TxHdr1[5]	
4	0	TxHdr1[4]	
3	0	TxHdr1[3]	VPI bits
2	0	TxHdr1[2]	
1	0	TxHdr1[1]	
0	0	TxHdr1[0]	

0x11—TXHDR2 (Transmit Cell Header Control Register 2)

The TXHDR2 register contains the second byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr2[7]	These bits hold the Transmit Header values for Octet 2 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VPI bits
6	0	TxHdr2[6]	
5	0	TxHdr2[5]	
4	0	TxHdr2[4]	
3	0	TxHdr2[3]	VCI bits
2	0	TxHdr2[2]	
1	0	TxHdr2[1]	
0	0	TxHdr2[0]	

0x12—TXHDR3 (Transmit Cell Header Control Register 3)

The TXHDR3 register contains the third byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr3[7]	These bits hold the Transmit Header values for Octet 3 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VCI bits
6	0	TxHdr3[6]	
5	0	TxHdr3[5]	
4	0	TxHdr3[4]	
3	0	TxHdr3[3]	
2	0	TxHdr3[2]	
1	0	TxHdr3[1]	
0	0	TxHdr3[0]	

0x13—TXHDR4 (Transmit Cell Header Control Register 4)

The TXHDR4 register contains the fourth byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr4[7]	These bits hold the Transmit Header values for Octet 4 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VCI bits
6	0	TxHdr4[6]	
5	0	TxHdr4[5]	
4	0	TxHdr4[4]	
3	0	TxHdr4[3]	Payload-type bits
2	0	TxHdr4[2]	
1	0	TxHdr4[1]	
0	0	TxHdr4[0]	Cell Loss Priority bit

0x14—TXIDL1 (Transmit Idle Cell Header Control Register 1)

The TXIDL1 register contains the first byte of the Transmit Idle Cell Header. It controls the header value that is inserted in the transmitted idle cells. This header consists of 32 bits divided among four registers. Section 2.1.1 describes cell generation in detail.

Bit	Default	Name	Description
7	0	TxIdl1[7]	These bits hold the Transmit Idle Cell Header values for Octet 1 of the outgoing cell. GFC/VPI bits (for UNI they are GFC bits, for NNI the are VPI bits)
6	0	TxIdl1[6]	
5	0	TxIdl1[5]	
4	0	TxIdl1[4]	
3	0	TxIdl1[3]	VPI bits
2	0	TxIdl1[2]	
1	0	TxIdl1[1]	
0	0	TxIdl1[0]	

0x15—TXIDL2 (Transmit Idle Cell Header Control Register 2)

The TXIDL2 register contains the second byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl2[7]	These bits hold the Transmit Idle Cell Header values for Octet 2 of the outgoing cell.
6	0	TxIdl2[6]	
5	0	TxIdl2[5]	VPI bits
4	0	TxIdl2[4]	
3	0	TxIdl2[3]	
2	0	TxIdl2[2]	VCI bits
1	0	TxIdl2[1]	
0	0	TxIdl2[0]	

0x16—TXIDL3 (Transmit Idle Cell Header Control Register 3)

The TXIDL3 register contains the third byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl3[7]	These bits hold the Transmit Idle Cell Header values for Octet 3 of the outgoing cell.
6	0	TxIdl3[6]	
5	0	TxIdl3[5]	
4	0	TxIdl3[4]	
3	0	TxIdl3[3]	
2	0	TxIdl3[2]	VCI bits
1	0	TxIdl3[1]	
0	0	TxIdl3[0]	

0x17—TXIDL4 (Transmit Idle Cell Header Control Register 4)

The TXIDL4 register contains the fourth byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl4[7]	These bits hold the Transmit Idle Cell Header values for Octet 4 of the outgoing cell.
6	0	TxIdl4[6]	
5	0	TxIdl4[5]	VCI bits
4	0	TxIdl4[4]	
3	0	TxIdl4[3]	
2	0	TxIdl4[2]	Payload-type bits
1	0	TxIdl4[1]	
0	1	TxIdl4[0]	Cell Loss Priority bit

0x18—RXHDR1 (Receive Cell Header Control Register 1)

The RXHDR1 register contains the first byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port if an incoming ATM cell header matches the value in the header register. Receive Header Mask Registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr1[7]	These bits hold the Receive Header values for Octet 1 of the incoming cell.
6	0	RxHdr1[6]	
5	0	RxHdr1[5]	
4	0	RxHdr1[4]	
3	0	RxHdr1[3]	
2	0	RxHdr1[2]	
1	0	RxHdr1[1]	
0	0	RxHdr1[0]	

0x19—RXHDR2 (Receive Cell Header Control Register 2)

The RXHDR2 register contains the second byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr2[7]	These bits hold the Receive Header values for Octet 2 of the incoming cell.
6	0	RxHdr2[6]	
5	0	RxHdr2[5]	
4	0	RxHdr2[4]	
3	0	RxHdr2[3]	
2	0	RxHdr2[2]	
1	0	RxHdr2[1]	
0	0	RxHdr2[0]	

0x1A—RXHDR3 (Receive Cell Header Control Register 3)

The RXHDR3 register contains the third byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr3[7]	These bits hold the Receive Header values for Octet 3 of the incoming cell.
6	0	RxHdr3[6]	
5	0	RxHdr3[5]	
4	0	RxHdr3[4]	
3	0	RxHdr3[3]	
2	0	RxHdr3[2]	
1	0	RxHdr3[1]	
0	0	RxHdr3[0]	

0x1B—RXHDR4 (Receive Cell Header Control Register 4)

The RXHDR4 register contains the fourth byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr4[7]	These bits hold the Receive Header values for Octet 4 of the incoming cell.
6	0	RxHdr4[6]	
5	0	RxHdr4[5]	
4	0	RxHdr4[4]	
3	0	RxHdr4[3]	
2	0	RxHdr4[2]	
1	0	RxHdr4[1]	
0	0	RxHdr4[0]	

0x1C—RXMSK1 (Receive Cell Mask Control Register 1)

The RXMSK1 register contains the first byte of the Receive Cell Mask. It modifies ATM cell screening, which compares the Receive Cell Header Registers to the incoming cells (see Section 2.0.0.2). Setting a bit in the Mask Register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1 bit 0 to 1 causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk1[7]	These bits hold the Receive Header Mask for Octet 1 of the incoming cell.
6	1	RxMsk1[6]	
5	1	RxMsk1[5]	
4	1	RxMsk1[4]	
3	1	RxMsk1[3]	
2	1	RxMsk1[2]	
1	1	RxMsk1[1]	
0	1	RxMsk1[0]	

0x1D—RXMSK2 (Receive Cell Mask Control Register 2)

The RXMSK2 register contains the second byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk2[7]	These bits hold the Receive Header Mask for Octet 2 of the incoming cell.
6	1	RxMsk2[6]	
5	1	RxMsk2[5]	
4	1	RxMsk2[4]	
3	1	RxMsk2[3]	
2	1	RxMsk2[2]	
1	1	RxMsk2[1]	
0	1	RxMsk2[0]	

0x1E—RXMSK3 (Receive Cell Mask Control Register 3)

The RXMSK3 register contains the third byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk3[7]	These bits hold the Receive Header Mask for Octet 3 of the incoming cell.
6	1	RxMsk3[6]	
5	1	RxMsk3[5]	
4	1	RxMsk3[4]	
3	1	RxMsk3[3]	
2	1	RxMsk3[2]	
1	1	RxMsk3[1]	
0	1	RxMsk3[0]	

0x1F—RXMSK4 (Receive Cell Mask Control Register 4)

The RXMSK4 register contains the fourth byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk4[7]	These bits hold the Receive Header Mask for Octet 4 of the incoming cell.
6	1	RxMsk4[6]	
5	1	RxMsk4[5]	
4	1	RxMsk4[4]	
3	1	RxMsk4[3]	
2	1	RxMsk4[2]	
1	1	RxMsk4[1]	
0	1	RxMsk4[0]	

0x20—RXIDL1 (Receive Idle Cell Header Control Register 1)

The RXIDL1 register contains the first byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are discarded from the received stream if register CVAL (0x0C) bit 6 is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl1[7]	These bits hold the Receive Idle cell header for Octet 1 of the incoming cell.
6	0	RxIdl1[6]	
5	0	RxIdl1[5]	
4	0	RxIdl1[4]	
3	0	RxIdl1[3]	
2	0	RxIdl1[2]	
1	0	RxIdl1[1]	
0	0	RxIdl1[0]	

0x21—RXIDL2 (Receive Idle Cell Header Control Register 2)

The RXIDL2 register contains the second byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl2[7]	These bits hold the Receive Idle cell header for Octet 2 of the incoming cell.
6	0	RxIdl2[6]	
5	0	RxIdl2[5]	
4	0	RxIdl2[4]	
3	0	RxIdl2[3]	
2	0	RxIdl2[2]	
1	0	RxIdl2[1]	
0	0	RxIdl2[0]	

0x22—RXIDL3 (Receive Idle Cell Header Control Register 3)

The RXIDL3 register contains the third byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl3[7]	These bits hold the Receive Idle cell header for Octet 3 of the incoming cell.
6	0	RxIdl3[6]	
5	0	RxIdl3[5]	
4	0	RxIdl3[4]	
3	0	RxIdl3[3]	
2	0	RxIdl3[2]	
1	0	RxIdl3[1]	
0	0	RxIdl3[0]	

0x23—RXIDL4 (Receive Idle Cell Header Control Register 4)

The RXIDL4 register contains the fourth byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl4[7]	These bits hold the Receive Idle cell header for Octet 4 of the incoming cell.
6	0	RxIdl4[6]	
5	0	RxIdl4[5]	
4	0	RxIdl4[4]	
3	0	RxIdl4[3]	
2	0	RxIdl4[2]	
1	0	RxIdl4[1]	
0	1	RxIdl4[0]	

0x24—IDLMSK1 (Receive Idle Cell Mask Control Register 1)

The IDLMSK1 register contains the first byte of the Receive Idle Cell Mask. It modifies ATM cell screening, which compares the Receive Idle Cell Header Registers to the incoming cells (see Section 2.0.0.2). Setting a bit in the Mask Register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1 bit 0 to 1 causes cells to be accepted as ATM idle cells with either 1 or 0 in the octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk1[7]	These bits hold the Receive Idle cell header mask for Octet 1 of the incoming cell.
6	0	IdlMsk1[6]	
5	0	IdlMsk1[5]	
4	0	IdlMsk1[4]	
3	0	IdlMsk1[3]	
2	0	IdlMsk1[2]	
1	0	IdlMsk1[1]	
0	0	IdlMsk1[0]	

0x25—IDLMSK2 (Receive Idle Cell Mask Control Register 2)

The IDLMSK2 register contains the second byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk2[7]	These bits hold the Receive Idle cell header mask for Octet 2 of the incoming cell.
6	0	IdlMsk2[6]	
5	0	IdlMsk2[5]	
4	0	IdlMsk2[4]	
3	0	IdlMsk2[3]	
2	0	IdlMsk2[2]	
1	0	IdlMsk2[1]	
0	0	IdlMsk2[0]	

0x26—IDLMSK3 (Receive Idle Cell Mask Control Register 3)

The IDLMSK3 register contains the third byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk3[7]	These bits hold the Receive Idle cell header mask for Octet 3 of the incoming cell.
6	0	IdlMsk3[6]	
5	0	IdlMsk3[5]	
4	0	IdlMsk3[4]	
3	0	IdlMsk3[3]	
2	0	IdlMsk3[2]	
1	0	IdlMsk3[1]	
0	0	IdlMsk3[0]	

0x27—IDLMSK4 (Receive Idle Cell Mask Control Register 4)

The IDLMSK4 register contains the fourth byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk4[7]	These bits hold the Receive Idle cell header mask for Octet 4 of the incoming cell.
6	0	IdlMsk4[6]	
5	0	IdlMsk4[5]	
4	0	IdlMsk4[4]	
3	0	IdlMsk4[3]	
2	0	IdlMsk4[2]	
1	0	IdlMsk4[1]	
0	0	IdlMsk4[0]	

0x28—ENCELLT (Transmit Cell Interrupt Control Register)

The ENCELLT register controls which of the interrupts listed in the TxCellInt register (0x2C) appear on the MInt~ pin (pin B19), provided that both EnTxCellInt (bit 1) in the ENSUMINT register (0x01) and EnPortInt in the ENSUMPORT register (0x0201) for this port are enabled, and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	1	EnParErrInt	When written to a logical 1, this bit enables the Parity Error Interrupt.
6	1	EnSOCErrInt	When written to a logical 1, this bit enables the Start of Cell Error Interrupt.
5	1	EnTxOvflInt	When written to a logical 1, this bit enables the Transmit FIFO Overflow Interrupt.
4	1	EnRxOvflInt	When written to a logical 1, this bit enables the Receive FIFO Overflow Interrupt.
3	1	EnCellSentInt	When written to a logical 1, this bit enables the Cell Sent Interrupt.
2	1	EnBusCnflctInt	When written to a logical 1, this bit enables the Bus Conflict Interrupt.
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, set to a logical 0.

0x29—ENCELLR (Receive Cell Interrupt Control Register)

The ENCELLR register controls which of the interrupts listed in the RxCellInt register (0x2D) appear on the MInt~ pin (pin B19), provided that both EnRxCellInt (bit 0) in the ENSUMINT register (0x01) and EnPortInt in the ENSUMPORT register (0x0201) for this port are enabled, and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	1	EnLOCDInt	When written to a logical 1, this bit enables a Loss of Cell Delineation Interrupt.
6	1	EnHECDetInt	When written to a logical 1, this bit enables a HEC Error Detected Interrupt.
5	1	EnHECCorrInt	When written to a logical 1, this bit enables a HEC Error Corrected Interrupt.
4	1	EnRcvrHldInt	When written to a logical 1, this bit enables a Receiver Hold Interrupt.
3	1	EnCellRcvdInt	When written to a logical 1, this bit enables a Cell Received Interrupt.
2	1	EnIdleRcvdInt	When written to a logical 1, this bit enables an Idle Cell Received Interrupt.
1	1	EnNonMatchInt	When written to a logical 1, this bit enables a Non-matching Cell Received Interrupt.
0	1	EnNonZerGFCInt	When written to a logical 1, this bit enables a Non-zero GFC Received Interrupt.

0x2C—TXCELLINT (Transmit Cell Interrupt Indication Status Register)

The TXCELLINT register indicates that a change of status has occurred within the transmit status signals.

Bit	Default	Name	Description
7	—	ParErrInt(1)	When a logical 1 is read, this bit indicates that a Parity Error occurred.
6	—	SOCErrInt(1)	When a logical 1 is read, this bit indicates that a Start of Cell Error occurred.
5	—	TxOvflInt(1)	When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow occurred.
4	—	RxOvflInt(1)	When a logical 1 is read, this bit indicates that a Receive FIFO Overflow occurred.
3	—	CellSentInt(1)	When a logical 1 is read, this bit indicates that a cell has been sent.
2	—	BusCnflctInt(1)	When a logical 1 is read, this bit indicates that a Bus Conflict occurred.
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, set to a logical 0.

NOTE(S):

(1) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2D—RXCELLINT (Receive Cell Interrupt Indication Status Register)

The RXCELLINT register indicates that a change of status has occurred within the receive status signals.

Bit	Default	Name	Description
7	—	LOCDInt(1)	When a logical 1 is read, this bit indicates that a Loss of Cell Delineation has occurred.
6	—	HECDetInt(2)	When a logical 1 is read, this bit indicates that a HEC Error was detected.
5	—	HECCorrInt(2)	When a logical 1 is read, this bit indicates that a HEC Error was corrected.
4	—	RcvrHldInt(1)	When a logical 1 is read, this bit indicates that a Receiver Hold has occurred.
3	—	CellRcvdInt(2)	When a logical 1 is read, this bit indicates that a cell has been received.
2	—	IdleRcvdInt(2)	When a logical 1 is read, this bit indicates that an Idle Cell has been received.
1	—	NonMatchInt(2)	When a logical 1 is read, this bit indicates that a Non-matching Cell has been received.
0	—	NonZerGFCInt(2)	When a logic 1 is read, this bit indicates that a Non-zero GFC has been received.

NOTE(S):
(1) Dual event—Either a 0 to 1 or a 1 to 0 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.
(2) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2E—TXCELL (Transmit Cell Status Register)

The TXCELL register contains status for the cell transmitter.

Bit	Default	Name	Description
7	—	ParErr(1)	When a logical 1 is read, this bit indicates that a parity error was received on the transmit UTOPIA input data octet.
6	—	SOCErr(1)	When a logical 1 is read, this bit indicates that a Start of Cell Error was received on the UTxSOC pin (pin W12).
5	—	TxOvfl(1)	When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow condition occurred in the transmit UTOPIA FIFO.
4	—	RxOvfl(1)	When a logical 1 is read, this bit indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO.
3	—	CellSent(1)	When a logical 1 is read, this bit indicates that a non-idle cell was formatted and transmitted.
2	—	BusCnflct(1)	When a logical 1 is read, this bit indicates that a UTOPIA bus conflict has occurred, which means that a duplicate multi-PHY address has been programmed for this port. Check the contents of the UTOP2 register (0x0E).
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, set to a logical 0.

NOTE(S):
(1) This status indicates an event that occurred since the register was last read.

0x2F—RXCELL (Receive Cell Status Register)

The RXCELL register contains status for the cell receiver.

Bit	Default	Name	Description
7	—	LOCD(1)	When a logical 1 is read, this bit indicates a Loss of Cell Delineation.
6	—	HECDet(2)	When a logical 1 is read, this bit indicates that an uncorrected HEC Error was detected.
5	—	HECCorr(2)	When a logical 1 is read, this bit indicates that a HEC Error was corrected.
4	—	RcvrHld(1)	When a logical 1 is read, this bit indicates that an active level was detected on the LRxHld pin (pin V1, P1, K3, F1, C2, C6, B9, or D12).
3	—	CellRcvd(2)	When a logical 1 is read, this bit indicates that a cell with a header matching the receive header value and mask criteria was received.
2	—	IdleRcvd(2)	When a logical 1 is read, this bit indicates that a cell with a header matching the receive idle cell header value and mask criteria was received.
1	—	NonMatch(2)	When a logical 1 is read, this bit indicates that a cell with a header not matching either the receive cell or idle cell criteria was received.
0	—	NonZerGFC(2)	When a logical 1 is read, this bit indicates that a cell with a Non-zero GFC field in the header was received.

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status indicates an event that occurred since the register was last read.

0x30—LOCDCNT (LOCD Event Counter)

The LOCDCNT counter tracks the number of LOCD events.

Bit	Default	Name	Description
7	—	LOCDCnt[7]	LOCD Event counter bit 7 (MSB).
6	—	LOCDCnt[6]	LOCD Event counter bit 6.
5	—	LOCDCnt[5]	LOCD Event counter bit 5.
4	—	LOCDCnt[4]	LOCD Event counter bit 4.
3	—	LOCDCnt[3]	LOCD Event counter bit 3.
2	—	LOCDCnt[2]	LOCD Event counter bit 2.
1	—	LOCDCnt[1]	LOCD Event counter bit 1.
0	—	LOCDCnt[0]	LOCD Event counter bit 0 (LSB).

0x31—CORRCNT (Corrected HEC Error Counter)

The CORRCNT counter tracks the number of corrected HEC errors.

Bit	Default	Name	Description
7	—	CorrCnt[7]	Corrected HEC Error counter bit 7 (MSB).
6	—	CorrCnt[6]	Corrected HEC Error counter bit 6.
5	—	CorrCnt[5]	Corrected HEC Error counter bit 5.
4	—	CorrCnt[4]	Corrected HEC Error counter bit 4.
3	—	CorrCnt[3]	Corrected HEC Error counter bit 3.
2	—	CorrCnt[2]	Corrected HEC Error counter bit 2.
1	—	CorrCnt[1]	Corrected HEC Error counter bit 1.
0	—	CorrCnt[0]	Corrected HEC Error counter bit 0 (LSB).

0x32—UNCCNT (Uncorrected HEC Error Counter)

The UNCCNT counter tracks the number of uncorrected HEC errors.

Bit	Default	Name	Description
7	—	UncCnt[7]	Uncorrected HEC Error counter bit 7 (MSB).
6	—	UncCnt[6]	Uncorrected HEC Error counter bit 6.
5	—	UncCnt[5]	Uncorrected HEC Error counter bit 5.
4	—	UncCnt[4]	Uncorrected HEC Error counter bit 4.
3	—	UncCnt[3]	Uncorrected HEC Error counter bit 3.
2	—	UncCnt[2]	Uncorrected HEC Error counter bit 2.
1	—	UncCnt[1]	Uncorrected HEC Error counter bit 1.
0	—	UncCnt[0]	Uncorrected HEC Error counter bit 0 (LSB).

0x34—TXCNTL (Transmitted Cell Counter [Low Byte])

The TXCNTL counter tracks the number of transmitted cells. This byte of the counter should be read first.

Bit	Default	Name	Description
7	—	TxCnt[7]	Transmitted cell counter bit 7.
6	—	TxCnt[6]	Transmitted cell counter bit 6.
5	—	TxCnt[5]	Transmitted cell counter bit 5.
4	—	TxCnt[4]	Transmitted cell counter bit 4.
3	—	TxCnt[3]	Transmitted cell counter bit 3.
2	—	TxCnt[2]	Transmitted cell counter bit 2.
1	—	TxCnt[1]	Transmitted cell counter bit 1.
0	—	TxCnt[0]	Transmitted cell counter bit 0 (LSB).

0x35—TXCNTM (Transmitted Cell Counter [Mid Byte])

The TXCNTM counter tracks the number of transmitted cells.

Bit	Default	Name	Description
7	—	TxCnt[15]	Transmitted cell counter bit 15.
6	—	TxCnt[14]	Transmitted cell counter bit 14.
5	—	TxCnt[13]	Transmitted cell counter bit 13.
4	—	TxCnt[12]	Transmitted cell counter bit 12.
3	—	TxCnt[11]	Transmitted cell counter bit 11.
2	—	TxCnt[10]	Transmitted cell counter bit 10.
1	—	TxCnt[9]	Transmitted cell counter bit 9.
0	—	TxCnt[8]	Transmitted cell counter bit 8.

0x36—TXCNTH (Transmitted Cell Counter [High Byte])

The TXCNTH counter tracks the number of transmitted cells.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	—	TxCnt[18]	Transmitted cell counter bit 18 (MSB).
1	—	TxCnt[17]	Transmitted cell counter bit 17.
0	—	TxCnt[16]	Transmitted cell counter bit 16.

0x38—RXCNTL (Received Cell Counter [Low Byte])

The RXCNTL counter tracks the number of received cells. This byte of the counter should be read first.

Bit	Default	Name	Description
7	—	RxCnt[7]	Received cell counter bit 7.
6	—	RxCnt[6]	Received cell counter bit 6.
5	—	RxCnt[5]	Received cell counter bit 5.
4	—	RxCnt[4]	Received cell counter bit 4.
3	—	RxCnt[3]	Received cell counter bit 3.
2	—	RxCnt[2]	Received cell counter bit 2.
1	—	RxCnt[1]	Received cell counter bit 1.
0	—	RxCnt[0]	Received cell counter bit 0 (LSB).

0x39—RXCNTM (Received Cell Counter [Mid Byte])

The RXCNTM register tracks the number of received cells.

Bit	Default	Name	Description
7	—	RxCnt[15]	Received cell counter bit 15.
6	—	RxCnt[14]	Received cell counter bit 14.
5	—	RxCnt[13]	Received cell counter bit 13.
4	—	RxCnt[12]	Received cell counter bit 12.
3	—	RxCnt[11]	Received cell counter bit 11.
2	—	RxCnt[10]	Received cell counter bit 10.
1	—	RxCnt[9]	Received cell counter bit 9.
0	—	RxCnt[8]	Received cell counter bit 8.

0x3A—RXCNTH (Received Cell Counter [High Byte])

The RXCNTH counter tracks the number of received cells.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	—	RxCnt[18]	Received cell counter bit 18 (MSB).
1	—	RxCnt[17]	Received cell counter bit 17.
0	—	RxCnt[16]	Received cell counter bit 16.

0x3C—NONCNTL (Non-matching Cell Counter [Low Byte])

The NONCNTL counter tracks the number of non-matching cells. This byte of the counter should be read first.

Bit	Default	Name	Description
7	—	NonCnt[7]	Non-matching cell counter bit 7.
6	—	NonCnt[6]	Non-matching cell counter bit 6.
5	—	NonCnt[5]	Non-matching cell counter bit 5.
4	—	NonCnt[4]	Non-matching cell counter bit 4.
3	—	NonCnt[3]	Non-matching cell counter bit 3.
2	—	NonCnt[2]	Non-matching cell counter bit 2.
1	—	NonCnt[1]	Non-matching cell counter bit 1.
0	—	NonCnt[0]	Non-matching cell counter bit 0 (LSB).

0x3D—NONCNTH (Non-matching Cell Counter [High Byte])

The NONCNTH counter tracks the number of non-matching cells.

Bit	Default	Name	Description
7	—	NonCnt[15]	Non-matching cell counter bit 15 (MSB).
6	—	NonCnt[14]	Non-matching cell counter bit 14.
5	—	NonCnt[13]	Non-matching cell counter bit 13.
4	—	NonCnt[12]	Non-matching cell counter bit 12.
3	—	NonCnt[11]	Non-matching cell counter bit 11.
2	—	NonCnt[10]	Non-matching cell counter bit 10.
1	—	NonCnt[9]	Non-matching cell counter bit 9.
0	—	NonCnt[8]	Non-matching cell counter bit 8.

0x0200—SUMPORT (Summary Port Interrupt Status Register)

The SUMPORT register indicates the port summary interrupts.

Bit	Default	Name	Description
7	0	PortInt[7](1)	This bit is a summary indicator of the interrupts from the Port 7 SUMINT register (01C0).
6	0	PortInt[6](1)	This bit is a summary indicator of the interrupts from the Port 6 SUMINT register (0180).
5	0	PortInt[5](1)	This bit is a summary indicator of the interrupts from the Port 5 SUMINT register (0140).
4	0	PortInt[4](1)	This bit is a summary indicator of the interrupts from the Port 4 SUMINT register (0100).
3	0	PortInt[3](1)	This bit is a summary indicator of the interrupts from the Port 3 SUMINT register (00C0).
2	0	PortInt[2](1)	This bit is a summary indicator of the interrupts from the Port 2 SUMINT register (0080).
1	0	PortInt[1](1)	This bit is a summary indicator of the interrupts from the Port 1 SUMINT register (0040).
0	0	PortInt[0](1)	This bit is a summary indicator of the interrupts from the Port 0 SUMINT register (0000).

NOTE(S):

(1) This bit is a pointer to the next interrupt indication register to be read. This bit is cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

0x0201—ENSUMPORT (Summary Port Interrupt Control Register)

The ENSUMPORT register controls which of the interrupts listed in the SUMPORT register (0x0200) are observed on the MInt~ (pin B19) if MInt~ is also enabled. See Section 2.4.6.

Bit	Default	Name	Description
7	1	EnPortInt[7]	This bit enables PortInt[7] to appear on the MInt~ pin (pin B19).
6	1	EnPortInt[6]	This bit enables PortInt[6] to appear on the MInt~ pin (pin B19).
5	1	EnPortInt[5]	This bit enables PortInt[5] to appear on the MInt~ pin (pin B19).
4	1	EnPortInt[4]	This bit enables PortInt[4] to appear on the MInt~ pin (pin B19).
3	1	EnPortInt[3]	This bit enables PortInt[3] to appear on the MInt~ pin (pin B19).
2	1	EnPortInt[2]	This bit enables PortInt[2] to appear on the MInt~ pin (pin B19).
1	1	EnPortInt[1]	This bit enables PortInt[1] to appear on the MInt~ pin (pin B19).
0	1	EnPortInt[0]	This bit enables PortInt[0] to appear on the MInt~ pin (pin B19).

0x0202—MODE (Device Mode Control Register)

The MODE register controls the device-level software resets, one-second latch enables, and UTOPIA interface modes.

Bit	Default	Name	Description
7	0	DevMstRst	When written to a logical 1, this bit initiates a Device Master Reset. When the device resets, internal state machines are reset and all registers (0000–1FFF), except this one, assume their default values. Only bits 0–6 in this register are overwritten with their default values. ***NOTE(S):*** The reset process starts when this bit transitions from a 1 back to a 0. Software must not attempt to change any other bit in this register on the same write cycle as clearing DevMstRst.
6	0	DevLgcRst	When written to a logical 1, this bit initiates a Device Logic Reset. When the device resets, all internal state machines are reset, but all registers (0000–1FFF) listed as “Type: W/R” in Table 3-2 and Table 3-3 are unaltered.
5	0	EnStatLat	When written to a logical 1, this bit enables one-second status latching. When one-second status latching is enabled, the registers indicated in Table 3-3, footnote 1, are updated with new status information after a rising edge on the OneSecIn pin (pin A17). Status information in these registers is updated continuously if one-second status latching is disabled.
4	0	EnCntrLat	When written to a logical 1, this bit enables one-second counter latching. When one-second counter latching is enabled, the registers indicated in Table 3-3, footnote 2, are updated with new count information after a rising edge of the OneSecIn pin (pin A17). Count information in these registers is updated continuously if one-second counter latching is disabled.
3	0	EnIntPin	When written to a logical 1, this bit enables the MInt~ pin (pin B19).
2	1	UtopMode	When written to a logical 1, this bit enables UTOPIA Level 2 Mode. When written to a logical 0, UTOPIA Level 1 operation is enabled. This bit must be set to 1 for multi-PHY operation.
1	1	Handshake	When written to a logical 1, this bit enables UTOPIA cell handshaking. When written to a logical 0, UTOPIA octet handshaking is enabled.
0	0	BusWidth	When written to a logical 1, this bit enables the 8-bit UTOPIA bus. When written to a logical 0, the 16-bit UTOPIA bus is enabled.

4.0 Electrical and Mechanical Specifications

This chapter describes the electrical and mechanical aspects of the RS8228. It includes timing diagrams, absolute maximum ratings, DC characteristics, and mechanical drawings.

4.1 Timing Specifications

This section provides timing diagrams and descriptions for the various interfaces of the RS8228. Table 4-1 lists the different types of timing relationships that appear in the timing diagrams. The timing relationship labels are numbered when they occur more than once in a diagram, so each label is unique. This numbering aids in identifying the appropriate label in the timing table. Signals are measured at the 50% point of the changing edge, except for those involving high impedance transitions, which are measured at 10% and 90%.

Table 4-1. Timing Diagram Nomenclature *(1 of 3)*

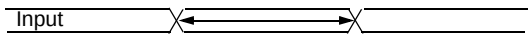
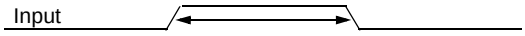
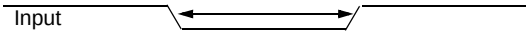
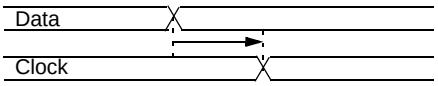
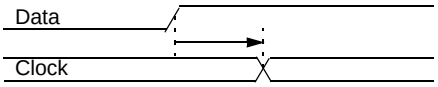
Symbol	Timing Relationship	Waveform
t_{pw}	Pulse Width	
t_{pwh}	Pulse Width High	
t_{pwl}	Pulse Width Low	
t_s	Setup Time	
t_{sh}	Setup High Time	

Table 4-1. Timing Diagram Nomenclature *(2 of 3)*

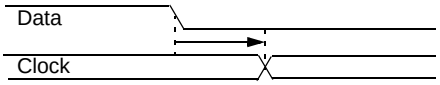
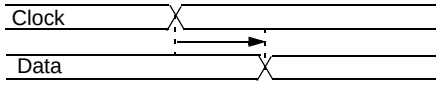
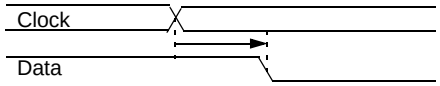
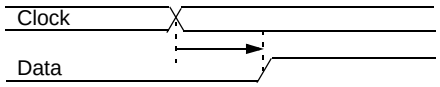
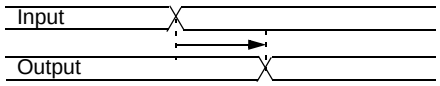
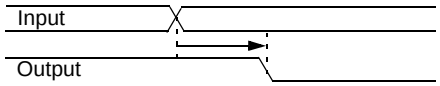
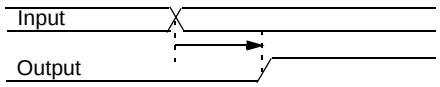
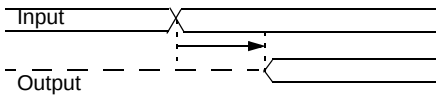
Symbol	Timing Relationship	Waveform
t_{sl}	Setup Low Time	
t_{h}	Hold Time	
t_{hh}	Hold High Time	
t_{hl}	Hold Low Time	
t_{pd}	Propagation Delay	
t_{pdhl}	Propagation Delay—High-to-Low	
t_{pdlh}	Propagation Delay—Low-to-High	
t_{en}	Enable Time	

***Table 4-1. Timing Diagram Nomenclature** (3 of 3)*

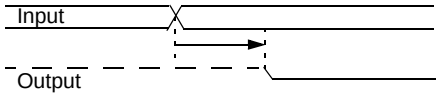
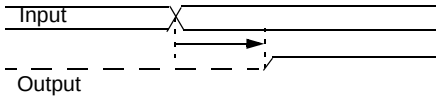
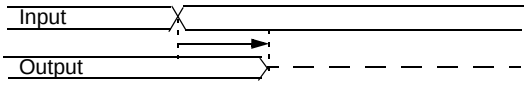
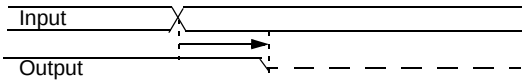
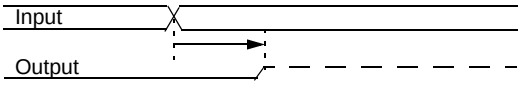
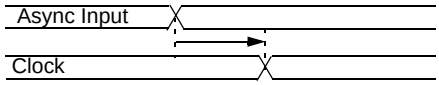
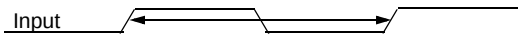
Symbol	Timing Relationship	Waveform
t_{enzl}	Enable Time—High-impedance to Low Enable	
t_{enzh}	Enable Time—High-impedance to High Enable	
t_{dis}	Disable Time	
t_{dishz}	Disable Time—High Disable	
t_{dislz}	Disable Time—Low Disable	
t_{rec}	Recovery Time	
t_{per}	Period	
t_{cyc}	Cycle Time	
f_{max}	Maximum Frequency	
f_{min}	Minimum Frequency	

Figure 4-1 and Figure 4-2 illustrate how input and output waveforms are defined.

Figure 4-1. Input Waveform

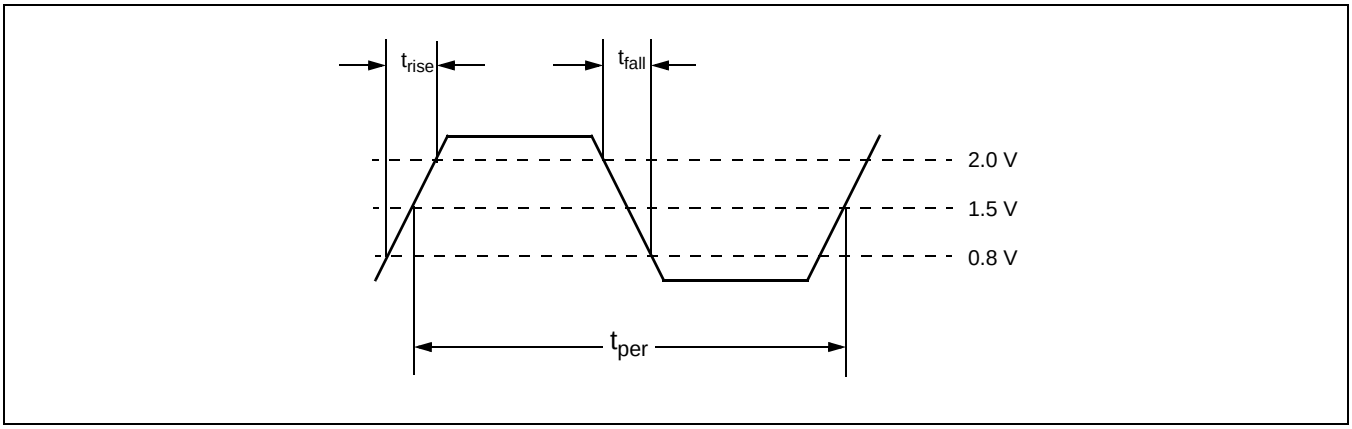
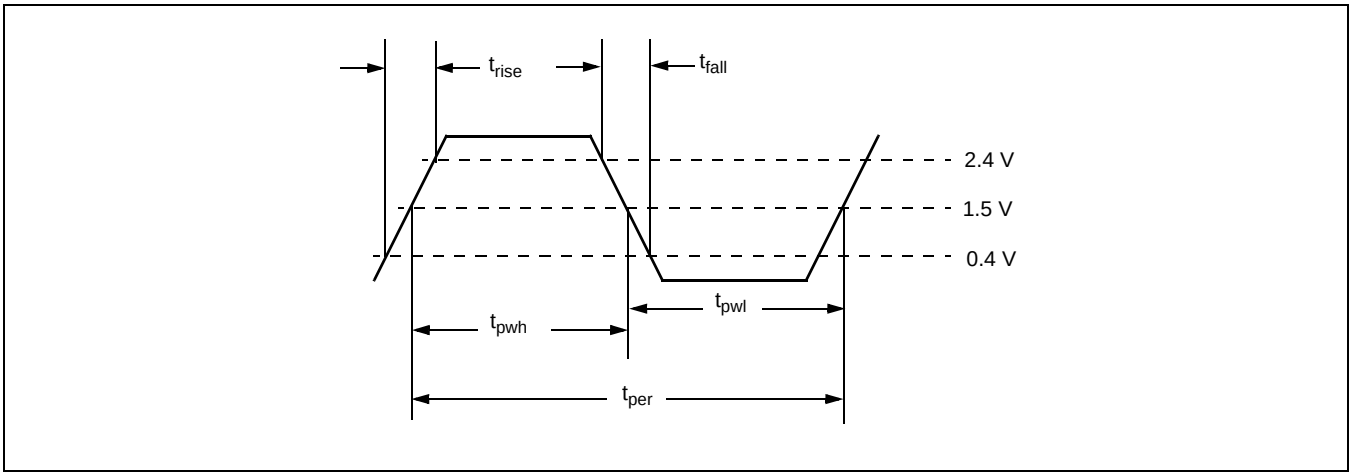


Figure 4-2. Output Waveform



4.1.1 Microprocessor Timing

Figures 4-3 through 4-6 and Tables 4-2 through 4-5 show the timing requirements and characteristics of the microprocessor interface.

Figure 4-3. Microprocessor Timing Diagram—Asynchronous Read

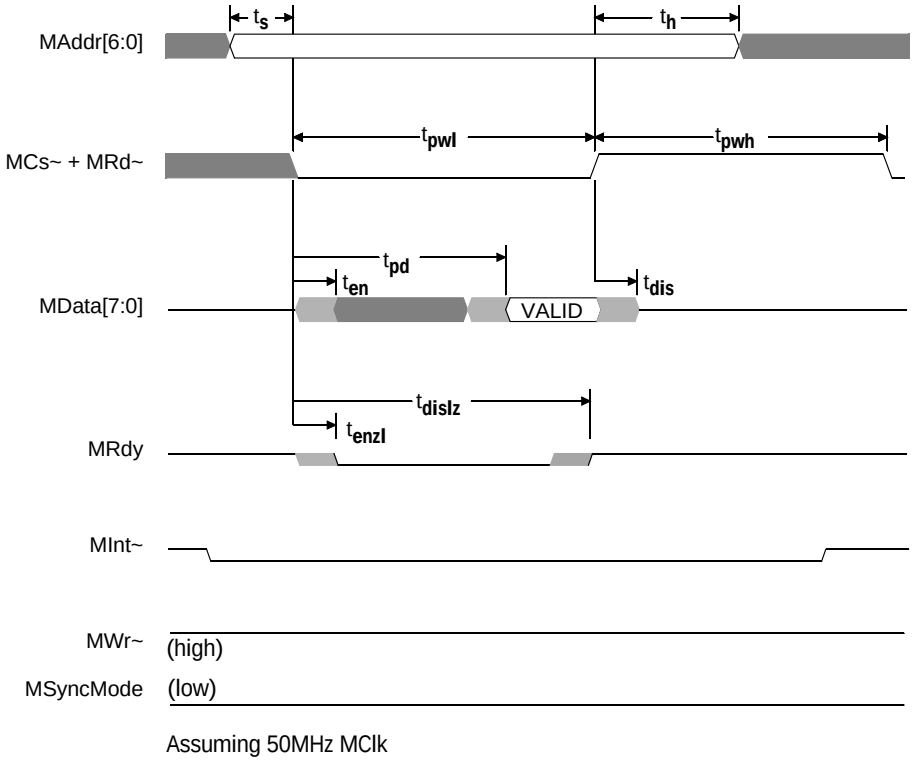


Table 4-2. Microprocessor Timing Table—Asynchronous Read

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low (MCs~ + MRd~)	3 * Mclk + 20	—	ns
t_{pwh}	Pulse Width High (MCs~ + MRd~)	80	—	ns
t_{s}	Setup, MAddr[6:0] to the falling edge of (MCs~ + MRd~)	2	—	ns
t_{h}	Hold, MAddr[6:0] from the rising edge of (MCs~ + MRd~)	7	—	ns
t_{en}	Enable, MData[7:0] from the falling edge of (MCs~ + MRd~)	2	13	ns
t_{pd}	Propagation Delay, MData[7:0] from the falling edge of (MCs~ + MRd~)	—	50	ns
t_{dis}	Disable, MData[7:0] from the rising edge of (MCs~ + MRd~)	2	13	ns
t_{enzl}	Enable, MRdy from the falling edge of (MCs~ + MRd~)	1	10	ns
t_{dislz}	Disable, MRdy from the rising edge of (MCs~ + MRd~)	2 mclk+1	3 mclk+10	ns

Figure 4-4. MIcroprocessor Timing Diagram—Asynchronous Write

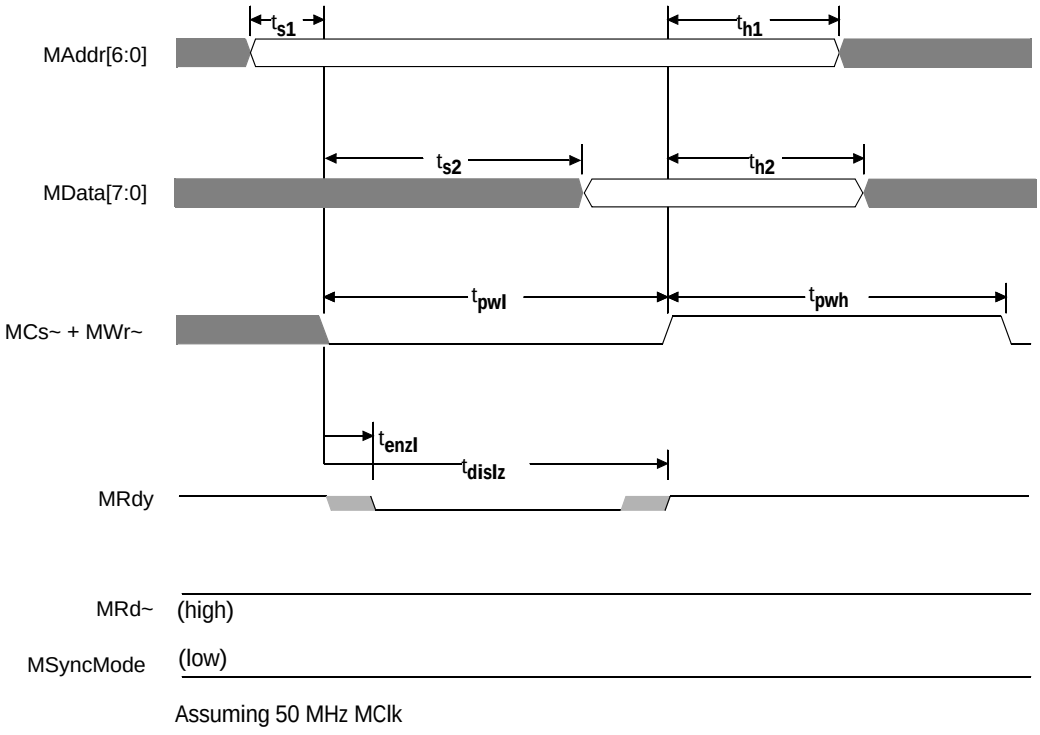


Table 4-3. Microprocessor Timing Table—Asynchronous Write

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low (MCs~ + MWr~)	80	—	ns
t_{pwh}	Pulse Width High (MCs~ + MWr~)	80	—	ns
t_{s1}	Setup, MAddr[6:0] to the falling edge of (MCs~ + MWr~)	2	—	ns
t_{h1}	Hold, MAddr[6:0] from the rising edge of (MCs~ + MWr~)	7	—	ns
t_{s2}	Setup, MData[7:0] from the falling edge of (MCs~ + MWr~)	—	Mclk – 8	ns
t_{h2}	Hold, MData[6:0] from the rising edge of (MCs~ + MWr~)	7	—	ns
t_{enzl}	Enable, MRdy from the falling edge of (MCs~ + MRd~)	1	10	ns
t_{dislz}	Disable, MRdy from the rising edge of (MCs~ + MRd~)	41	70	ns

Figure 4-5. Microprocessor Timing Diagram—Synchronous Read

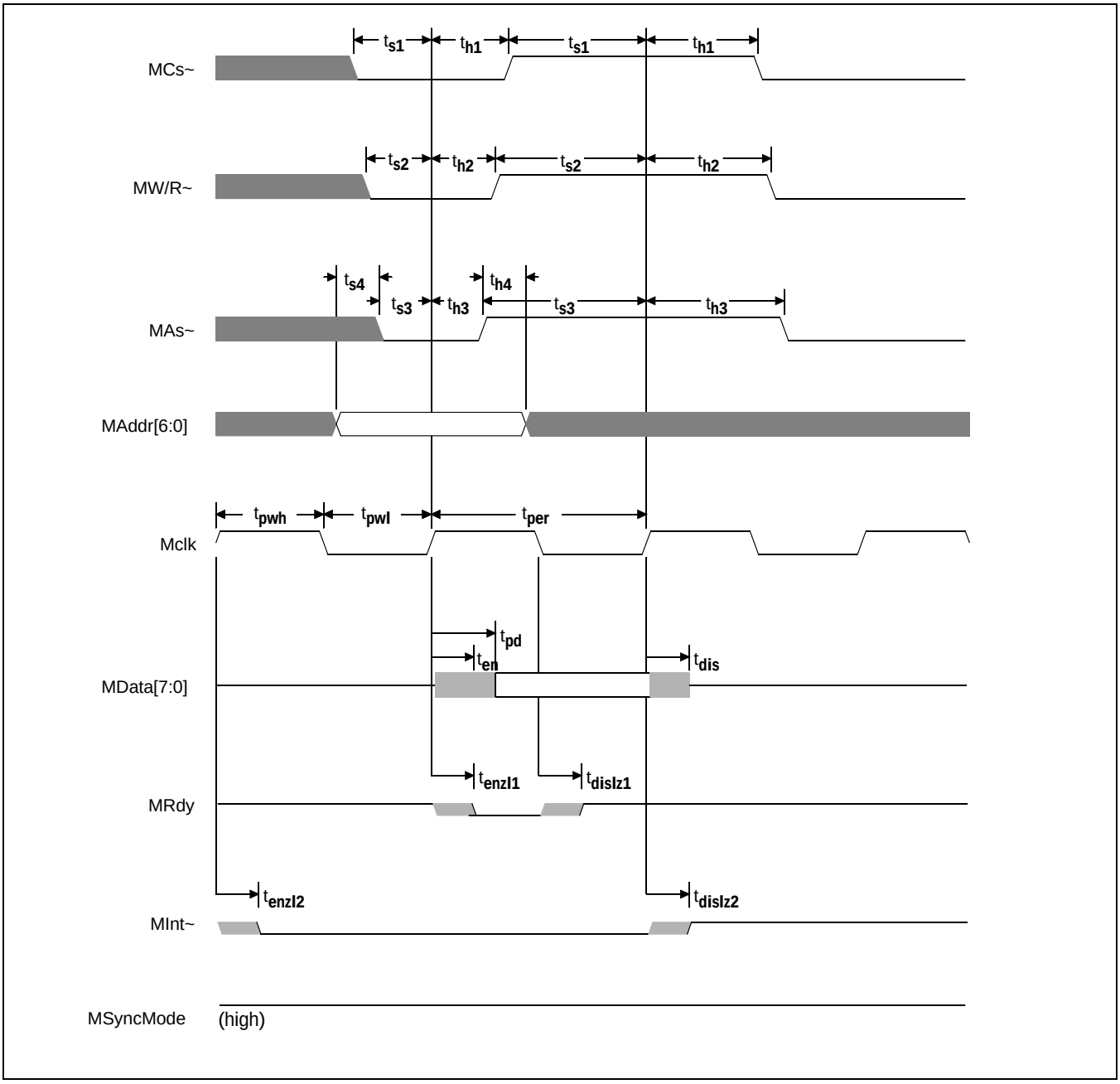


Table 4-4. Microprocessor Timing Table—Synchronous Read

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, MClk	10	50	ns
t_{pwh}	Pulse Width High, MClk	10	50	ns
t_{per}	Period, MClk (Min at 50 MHz, Max at 8 MHz)	20	125	ns
t_{s1}	Setup, MCs~ to the rising edge of MClk	1	—	ns
t_{h1}	Hold, MCs~ from the rising edge of MClk	2.5	—	ns
t_{s2}	Setup, MW/R~ to the falling edge of MClk	1	—	ns
t_{h2}	Hold, MW/R~ from the rising edge of MClk	2.5	—	ns
t_{s3}	Setup, MAs~ to the falling edge of MClk	1	—	ns
t_{h3}	Hold, MAs~ from the rising edge of MClk	2.5	—	ns
t_{s4}	Setup, MAddr[6:0] to the falling edge of MAs~	1	—	ns
t_{h4}	Hold, MAddr[6:0] from the rising edge of MAs~	2.5	—	ns
t_{en}	Enable, MData[7:0] from the rising edge of MClk	2	13	ns
t_{pd}	Propagation Delay, MData[7:0] from the rising edge of MClk	2	13	ns
t_{dis}	Disable, MData[7:0] from the rising edge of MClk	2	13	ns
t_{enzl1}	Enable, MRdy from the rising edge of MClk	2	10	ns
t_{dislz1}	Disable, MRdy from the falling edge of MClk	2	10	ns
t_{enzl2}	Enable, MInt~ from the rising edge of MClk	2	10	ns
t_{dislz2}	Disable, MInt~ from the rising edge of MClk	2	10	ns

Figure 4-6. Microprocessor Timing Diagram—Synchronous Write

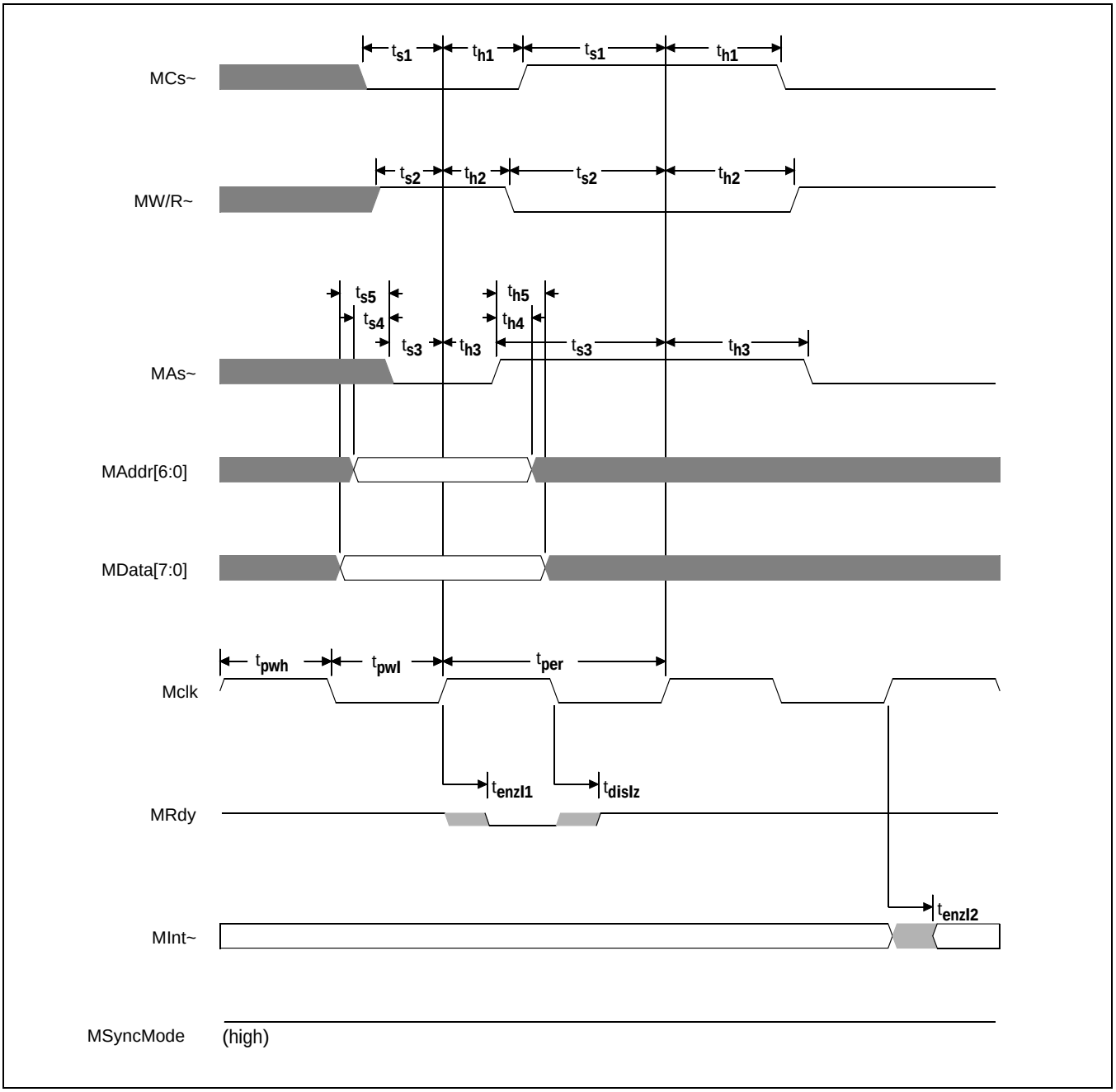


Table 4-5. Microprocessor Timing Table—Synchronous Write

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, MClk	10	50	ns
t_{pwh}	Pulse Width High, MClk	10	50	ns
t_{per}	Period, MClk (Min at 50 MHz, Max at 8 MHz)	20	125	ns
t_{s1}	Setup, MCs~ to the rising edge of MClk	1	—	ns
t_{h1}	Hold, MCs~ from the rising edge of MClk	2.5	—	ns
t_{s2}	Setup, MW/R~ to the falling edge of MClk	1	—	ns
t_{h2}	Hold, MW/R~ from the rising edge of MClk	2.5	—	ns
t_{s3}	Setup, MAs~ to the rising edge of MClk	1	—	ns
t_{h3}	Hold, MAs~ from the rising edge of MClk	2.5	—	ns
t_{s4}	Setup, MAddr[6:0] to the falling edge of MAs~	1	—	ns
t_{h4}	Hold, MAddr[6:0] from the rising edge of MAs~	2.5	—	ns
t_{s5}	Setup, MData[7:0] to the falling edge of MAs~	1	—	ns
t_{h5}	Hold, MData[7:0] from the rising edge of MAs~	2.5	—	ns
t_{enzl1}	Enable, MRdy from the rising edge of MClk	2	10	ns
t_{dislz}	Disable, MRdy from the falling edge of MClk	2	10	ns
t_{enzl2}	Enable, MInt~ from the rising edge of MClk	2	10	ns

4.1.2 Framer (Line) Interface Timing

Figures 4-7 through 4-9 and Tables 4-6 through 4-8 show the timing requirements and characteristics of the Framer (Line) interface.

NOTE: *The LCS uses combinational logic and is functional even when the RS825X is in reset.*

Figure 4-7. Framer (Line) Control Timing Diagram

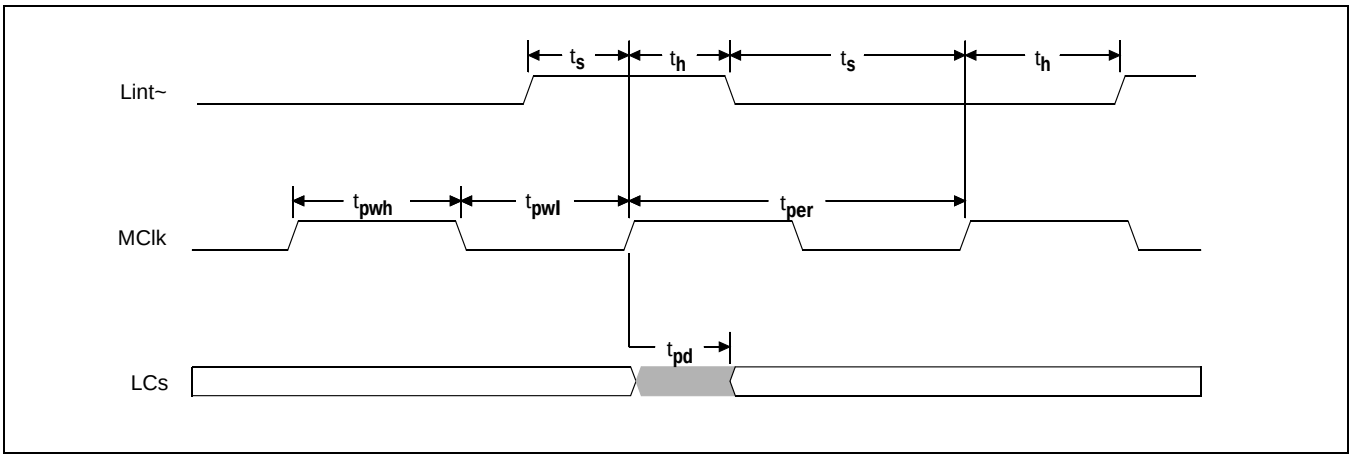


Table 4-6. Framer (Line) Control Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, MClk	10	62.5	ns
t_{pwh}	Pulse Width High, MClk	10	62.5	ns
t_{per}	Period, MClk (Minimum at 50 MHz, Maximum at 8 MHz)	20	125	ns
t_s	Setup, LInt~ to the rising edge of MClk	5	—	ns
t_h	Hold, LInt~ from the rising edge of MClk	5	—	ns
t_{pd}	Propagation Delay, LCs from the rising edge of MClk	1	15	ns

Figure 4-8. Framer (Line) Transmit Timing Diagram

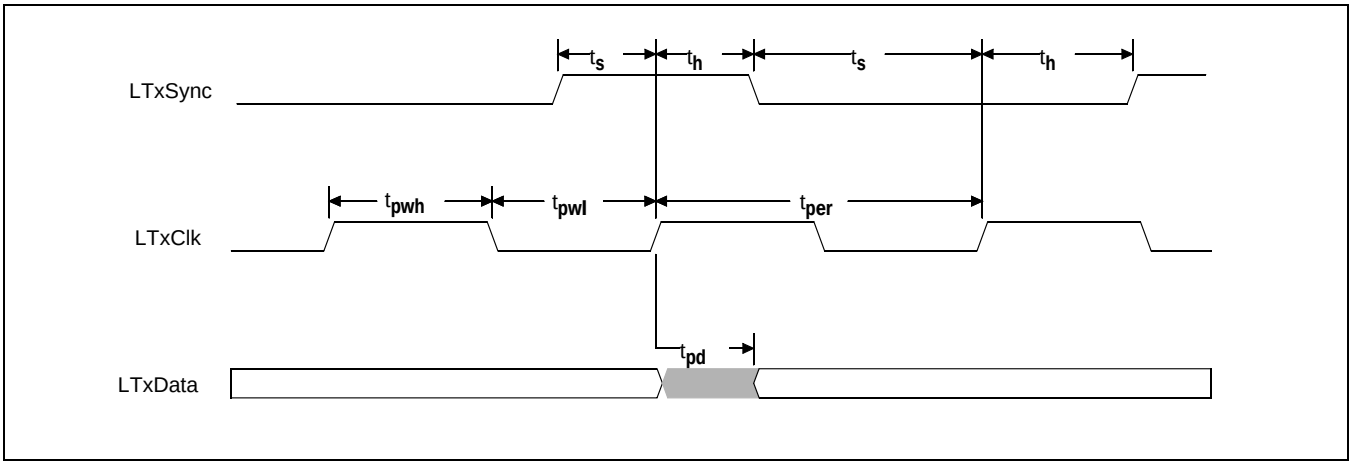


Table 4-7. Framer (Line) Transmit Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, LTxClk	10	325	ns
t_{pwh}	Pulse Width High, LTxClk	10	325	ns
t_{per}	Period, LTxClk (Min. at 50 MHz, Max. at 1.54 MHz)	20	650	ns
t_s	Setup, LTxSync to the rising edge of LTxClk	6	—	ns
t_h	Hold, LTxSync from the rising edge of LTxClk	6	—	ns
t_{pd}	Propagation Delay, LTxData from the rising edge of LTxClk	9.5	13	ns

Figure 4-9. Framer (Line) Receive Timing Diagram

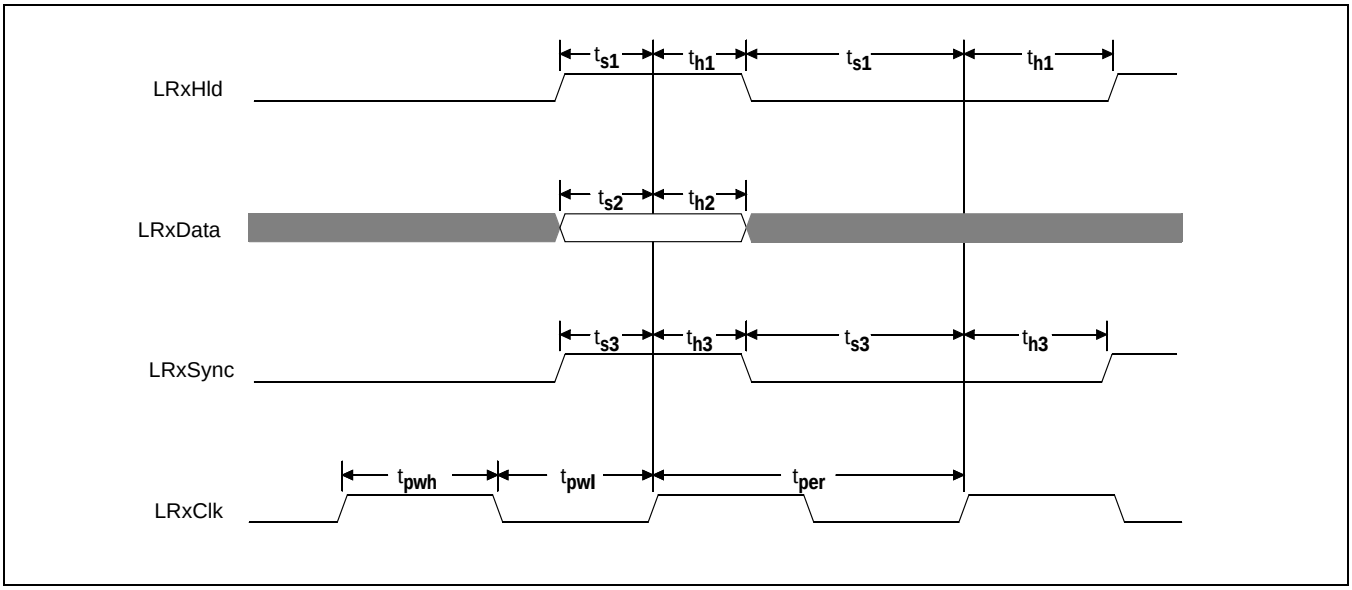


Table 4-8. Framer (Line) Receive Timing Table

Label	Description	Min Mclk = 50 MHz	Max Mclk = 1.5 MHz	Unit
t_{pwl}	Pulse Width Low, LRxClk	10	325	ns
t_{pwh}	Pulse Width High, LRxClk	10	325	ns
t_{per}	Period, LRxClk (Min. at 50 MHz, Max. at 1.54 MHz)	20	650	ns
t_{s1}	Setup, LRxHld to the rising edge of LRxClk	6	—	ns
t_{h1}	Hold, LRxHld from the rising edge of LRxClk	6	—	ns
t_{s2}	Setup, LRxData to the rising edge of LRxClk	4	—	ns
t_{h2}	Hold, LRxData from the rising edge of LRxClk	2	—	ns
t_{s3}	Setup, LRxSync to the rising edge of LRxClk	6	—	ns
t_{h3}	Hold, LRxSync from the rising edge of LRxClk	6	—	ns

4.1.3 UTOPIA Interface Timing

Figures 4-10 through 4-11 and Tables 4-9 through 4-10 show the timing requirements and characteristics of the UTOPIA interface.

Figure 4-10. UTOPIA Transmit Timing Diagram

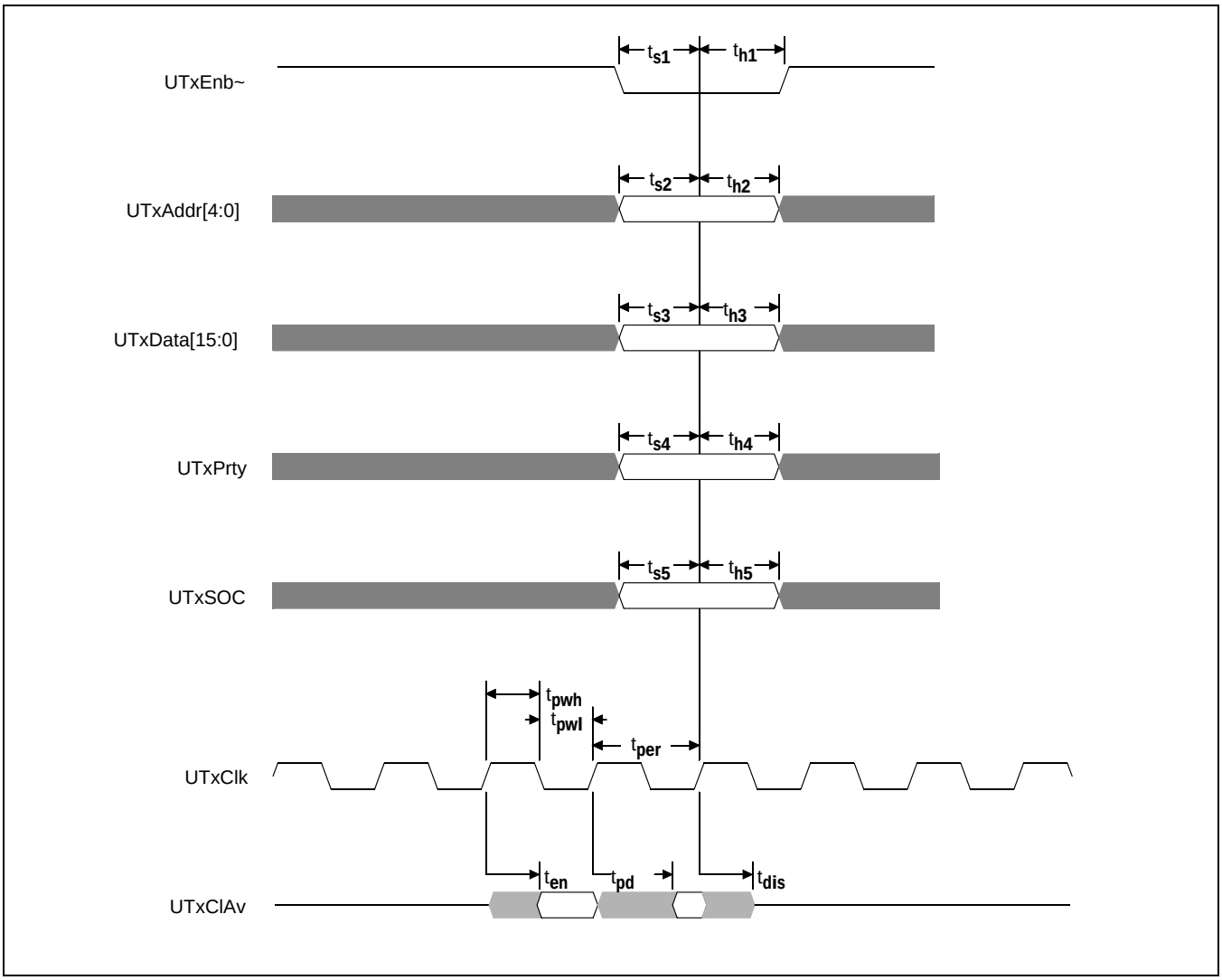


Table 4-9. UTOPIA Transmit Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, UTxClk	8	—	ns
t_{pwh}	Pulse Width High, UTxClk	8	—	ns
t_{per}	Period, UTxClk	20	—	ns
t_{s1}	Setup, UTxEnb~ to the rising edge of UTxClk	4	—	ns
t_{h1}	Hold, UTxEnb~ from the rising edge of UTxClk	1	—	ns
t_{s2}	Setup, UTxAddr to the rising edge of UTxClk	4	—	ns
t_{h2}	Hold, UTxAddr from the rising edge of UTxClk	1	—	ns
t_{s3}	Setup, UTxData to the rising edge of UTxClk	4	—	ns
t_{h3}	Hold, UTxData from the rising edge of UTxClk	1	—	ns
t_{s4}	Setup, UTxPrty to the rising edge of UTxClk	4	—	ns
t_{h4}	Hold, UTxPrty from the rising edge of UTxClk	1	—	ns
t_{s5}	Setup, UTxSOC to the rising edge of UTxClk	4	—	ns
t_{h5}	Hold, UTxSOC from the rising edge of UTxClk	1	—	ns
t_{en}	Enable, UTxClAv from the rising edge of UTxClk	1	4	ns
t_{pd}	Propagation Delay, UTxClAv from the rising edge of UTxClk	1	9	ns
t_{dis}	Disable, UTxClAv from the rising edge of UTxClk	1	4	ns

Figure 4-11. UTOPIA Receive Timing Diagram

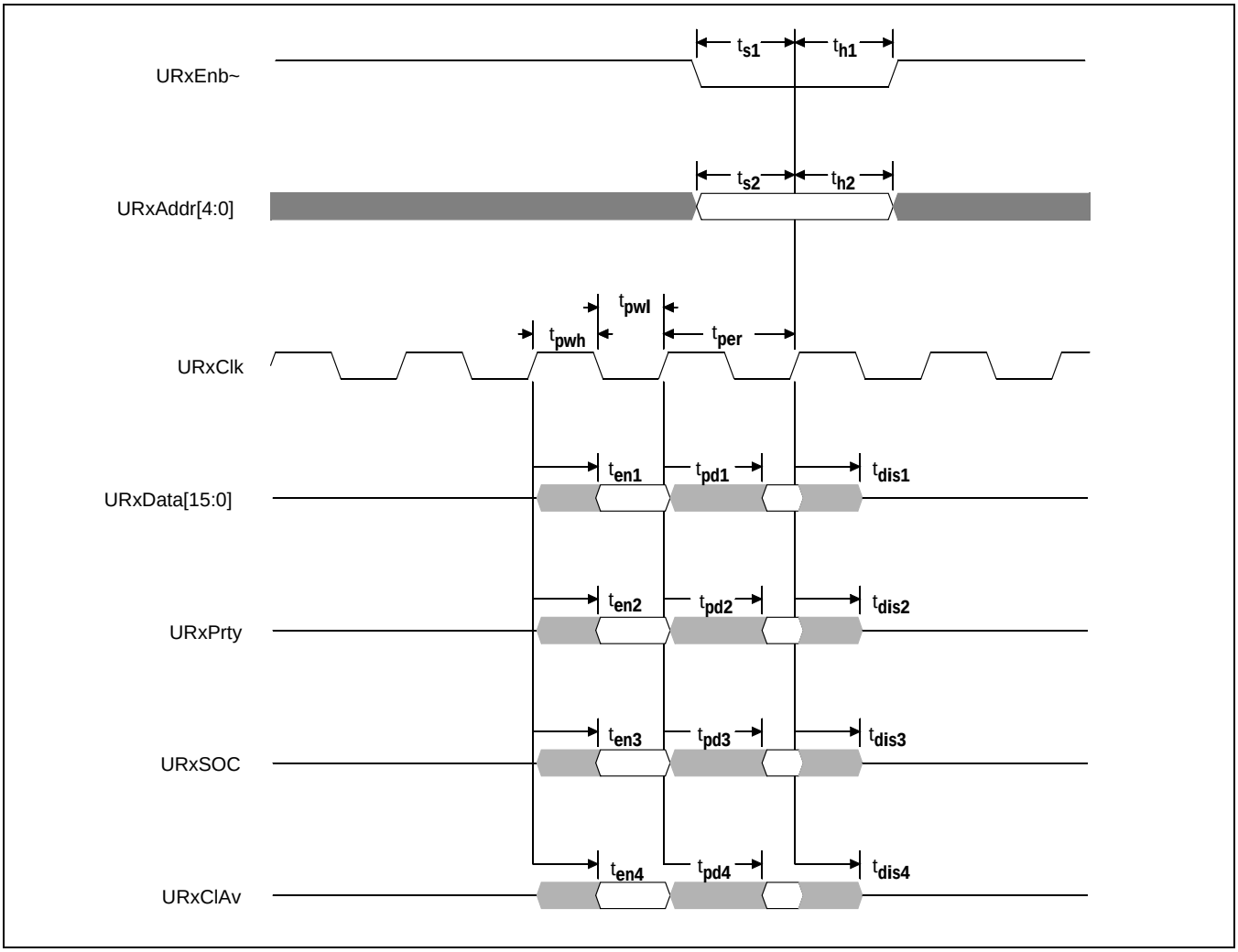


Table 4-10. UTOPIA Receive Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, URxClk	8	—	ns
t_{pwh}	Pulse Width High, URxClk	8	—	ns
t_{per}	Period, URxClk	20	—	ns
t_{s1}	Setup, URxEnb~ to the rising edge of URxClk	4	—	ns
t_{h1}	Hold, URxEnb~ from the rising edge of URxClk	1	—	ns
t_{s2}	Setup, URxAddr to the rising edge of URxClk	4	—	ns
t_{h2}	Hold, URxAddr from the rising edge of URxClk	1	—	ns
t_{en1}	Enable, URxData[15:0] from the rising edge of URxClk	2	10	ns

Table 4-10. UTOPIA Receive Timing Table

Label	Description	Min	Max	Unit
t_{pd1}	Propagation Delay, URxData[15:0] from the rising edge of URxClk	1	14	ns
t_{dis1}	Disable, URxData[15:0] from the rising edge of URxClk	2	10	ns
t_{en2}	Enable, URxPrty from the rising edge of URxClk	2	10	ns
t_{pd2}	Propagation Delay, URxPrty from the rising edge of URxClk	1	14	ns
t_{dis2}	Disable, URxPrty from the rising edge of URxClk	2	10	ns
t_{en3}	Enable, URxSOC from the rising edge of URxClk	2	10	ns
t_{pd3}	Propagation Delay, URxSOC from the rising edge of URxClk	1	14	ns
t_{dis3}	Disable, URxSOC from the rising edge of URxClk	2	10	ns
t_{en4}	Enable, URxClAv from the rising edge of URxClk	1	8	ns
t_{pd4}	Propagation Delay, URxClAv from the rising edge of URxClk	1	8	ns
t_{dis4}	Disable, URxClAv from the rising edge of URxClk	1	8	ns

4.1.4 JTAG Interface Timing

Figure 4-12 and Table 4-11 show the timing requirements and characteristics of the JTAG interface.

Figure 4-12. JTAG Timing Diagram

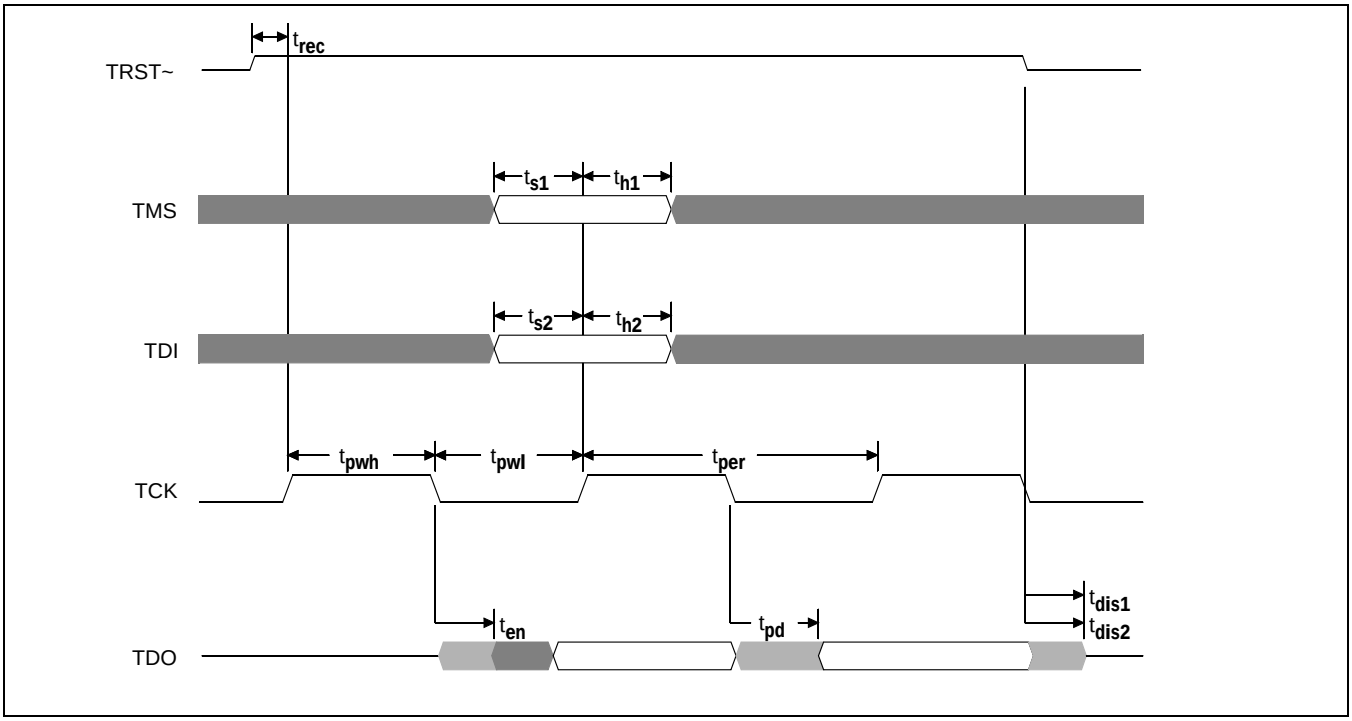


Table 4-11. JTAG Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, TCK	16	—	ns
t_{pwh}	Pulse Width High, TCK	16	—	ns
t_{per}	Period, TCK	40	—	ns
t_{rec}	Recovery, the rising edge of TCK from the rising edge of TRST~	2.5	—	ns
t_{s1}	Setup, TMS to the rising edge of TCK	2	—	ns
t_{h1}	Hold, TMS from the rising edge of TCK	—	1	ns
t_{s2}	Setup, TDI to the rising edge of TCK	2	—	ns
t_{h2}	Hold, TDI from the rising edge of TCK	—	1	ns
t_{en}	Enable, TDO from the falling edge of TCK	0.8	5	ns
t_{pd}	Propagation Delay, TDO from the falling edge of TCK	0.8	5	ns
t_{dis1}	Disable, TDO from the falling edge of TCK	0.8	5	ns
t_{dis2}	Disable, TDO from the falling edge of TRST~	0.8	5	ns

4.1.5 One-second Interface Timing

Figure 4-13 and Table 4-12 show the timing requirements and characteristics of the one-second interface.

Figure 4-13. One-second Timing Diagram

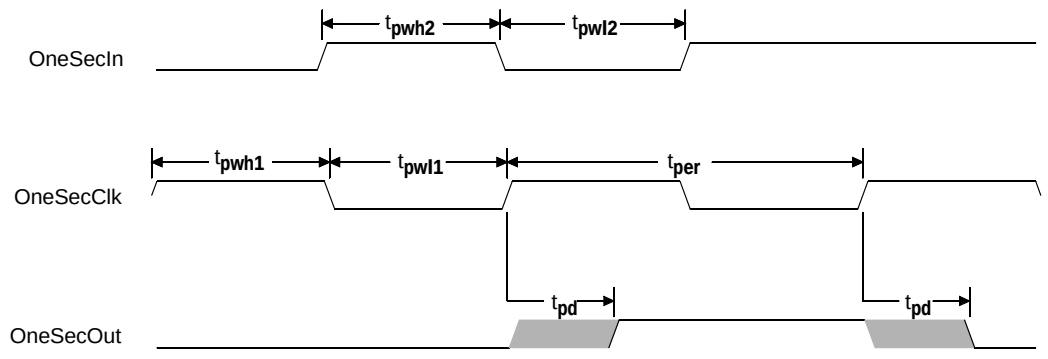


Table 4-12. One-second Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, OneSecIn	125	—	ns
t_{pwh}	Pulse Width High, OneSecIn	125	—	ns
t_{pwl}	Pulse Width Low, OneSecClk	62500	—	ns
t_{pwh}	Pulse Width High, OneSecClk	62500	—	ns
t_{per}	Period, OneSecClk (at 8 kHz)	12500	—	ns
t_{pd}	Propagation Delay, OneSecOut from the rising edge of OneSecClk	1	15	ns

4.2 Absolute Maximum Ratings

The absolute maximum ratings in Table 4-13 indicate the maximum stresses that the RS8228 can tolerate without risking permanent damage. These ratings are not typical of normal operation of the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 4-13. Absolute Maximum Ratings

Parameter	Value
Supply Voltage	–0.5 to +3.3 V
Input Voltage	–0.5 to Vdd + 0.5 V
Output Voltage	–0.5 to Vdd + 0.5 V
Storage Temperature	–40 °C to 125 °C
Operating Temperature Range	–40 °C to 85 °C
Lead Temperature	+240 °C for 10 seconds
Junction Temperature	+150 °C
Maximum Current at Maximum Clock Frequencies (not including LStatOut outputs)	145 mA
Static Discharge Voltage	±1000 V
Latch-up Current	±100 mA
DC Input Current	±20 mA
θ_{JC}	3.5 °C/W
θ_{JA}	30 °C/W

4.3 DC Characteristics

Table 4-14 lists the DC characteristics of the RS8228.

Table 4-14. DC Characteristics

Parameter	Min	Typical	Max	Comments
Power Supply (PWR)	3.0	3.3	3.6	VDC
Input Low Voltage (VIL) - 5 V-Tolerant HYS	0	—	0.3 * VDD	VDC
Input High Voltage (VIH) - 5 V-Tolerant HYS	0.7*VDD	—	5.25	VDC
Input Hysteresis - 5 V-Tolerant HYS	0.3	—		VDC
Output Voltage Low (TTL)	—	—	0.4	Volts; I_{OH} = 4.0 mA
Output Voltage High (TTL)	2.4	—	—	Volts; I_{OH} = 1500 µA
Input Leakage Current	–10	—	10	µA; Vin = PWR or GND
Three-state Output Leakage Current	–10	—	10	µA; Vout = PWR or GND
Input Capacitance	—	—	7	pF
Output Capacitance	—	—	7	pF
Bidirectional Capacitance	—	—	7	pF
Power consumed when processing cells on all 8 ports simultaneously:				
E1 or T1 data rate	—	200	—	mW; not including LStatOut pins
DS3 data rate	—	480	—	mW; not including LStatOut pins

4.4 27 mm Mechanical Drawing

The RS8228 is a 272-ball BGA package. A mechanical drawing of the device is provided in Figure 4-14 and Figure 4-15.

Figure 4-14. RS8228 27 mm Mechanical Drawing (Bottom View)

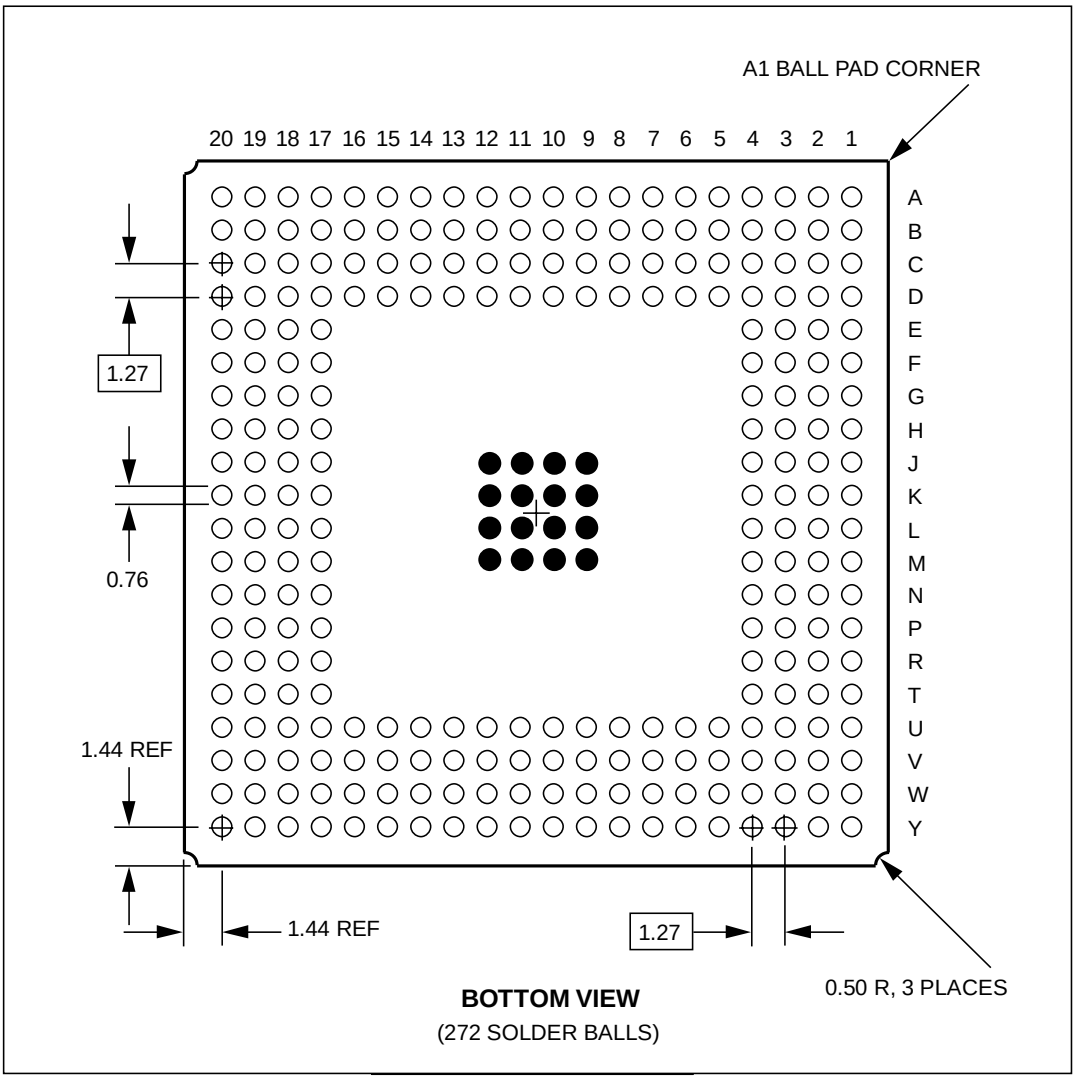
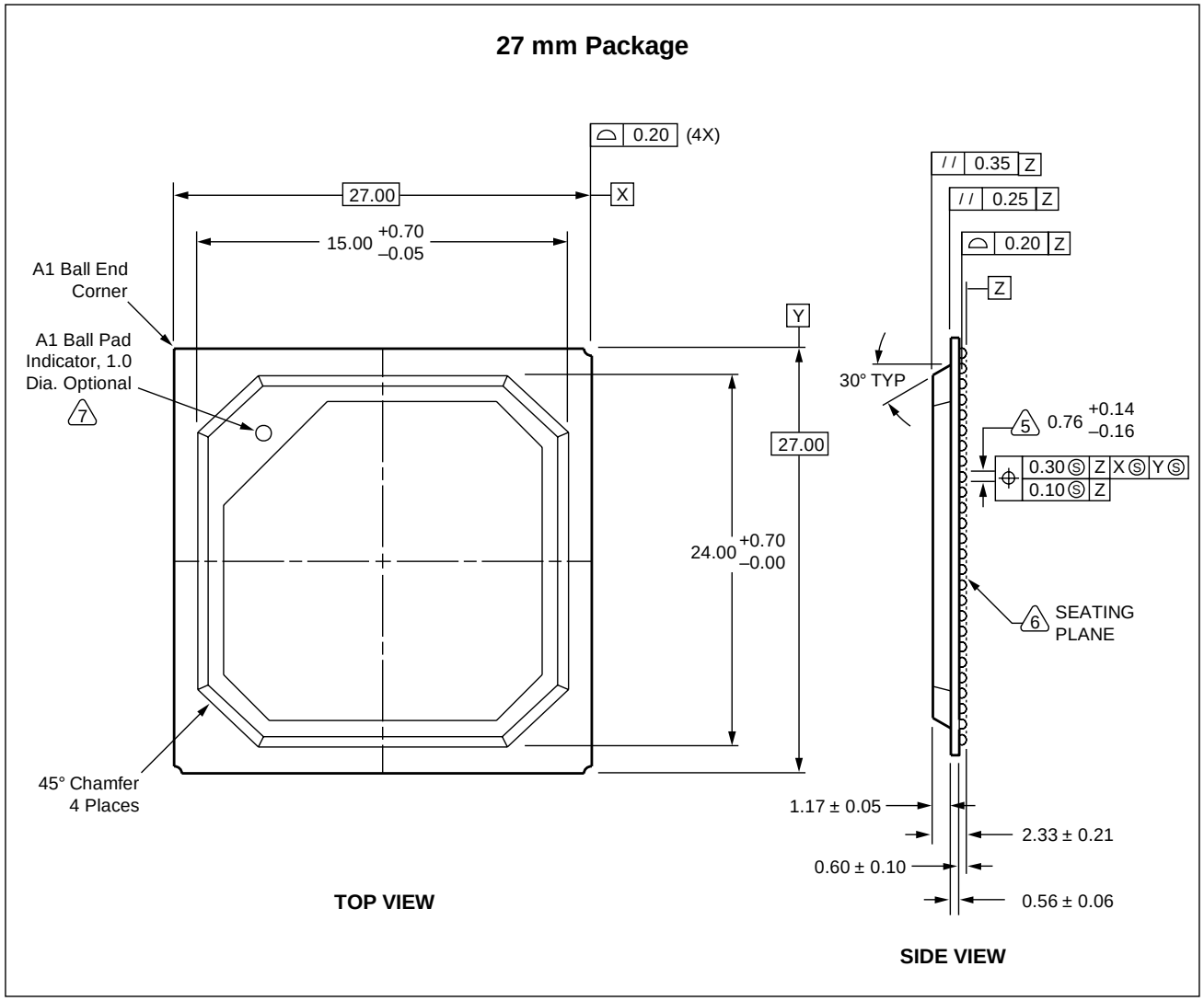


Figure 4-15. RS8228 27 mm Mechanical Drawing (Top and Side Views)



4.5 17 mm Mechanical Drawing

The M28228 is a 256-ball BGA package. A mechanical drawing of the device is provided in Figure 4-16 and Figure 4-17.

Figure 4-16. M28228 17 mm Mechanical Drawing (Bottom View)

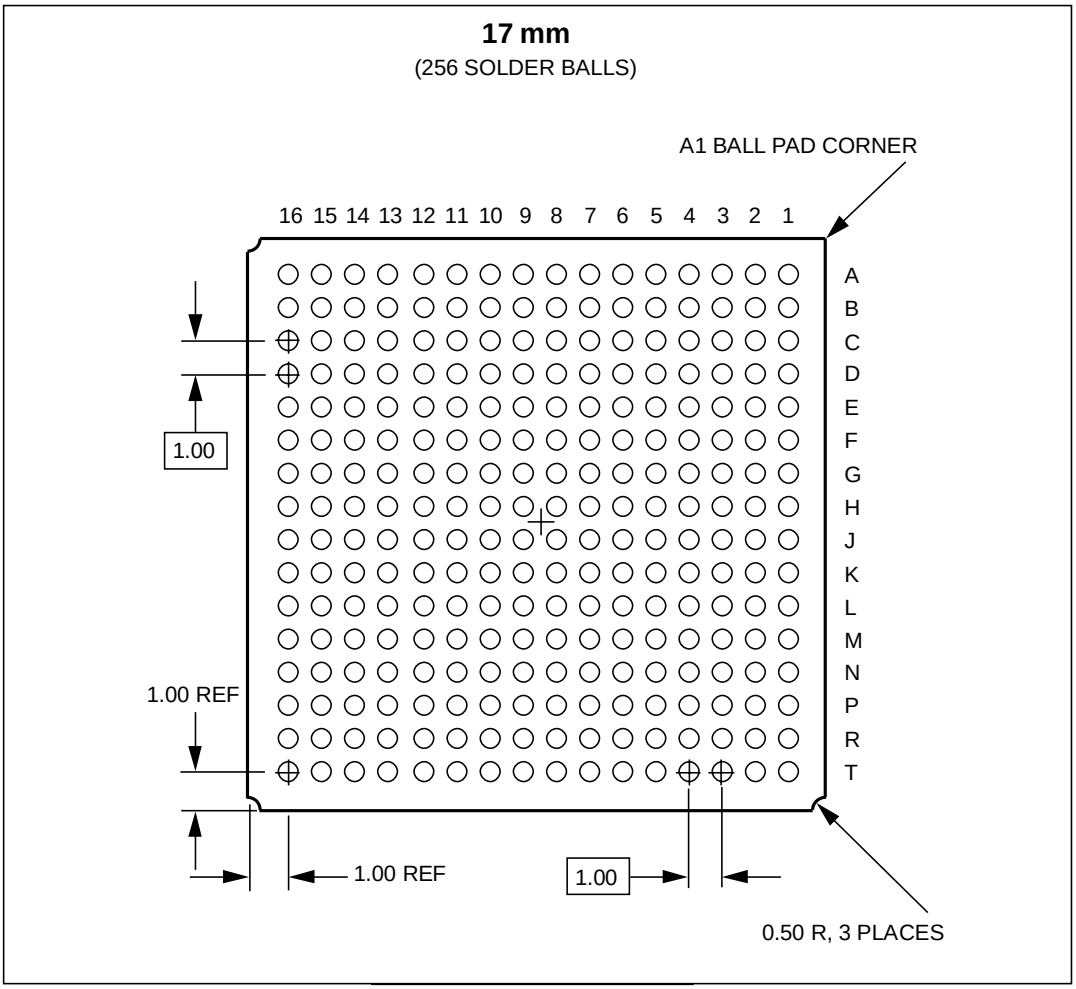
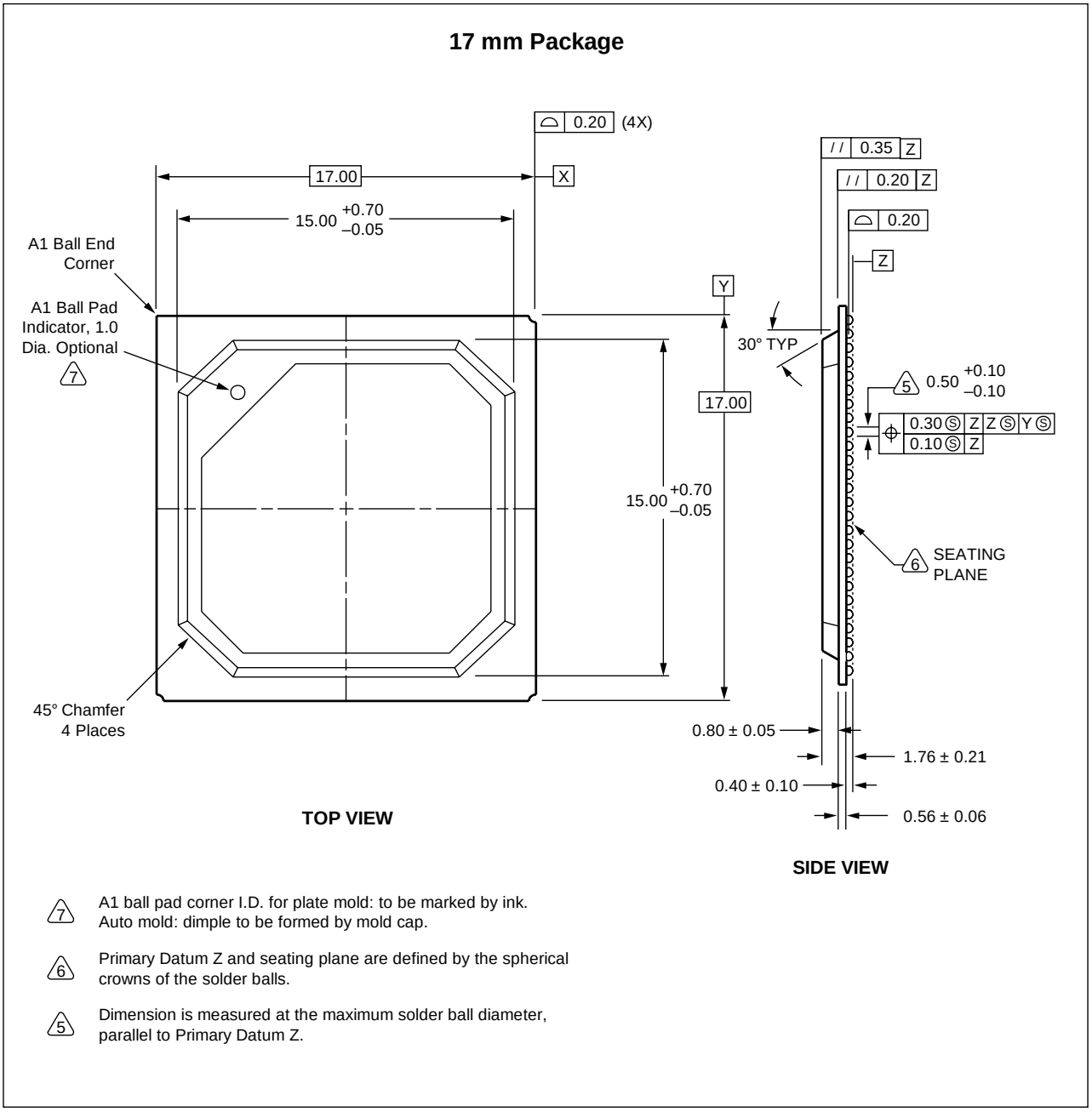


Figure 4-17. M28228 17 mm Mechanical Drawing (Top and Side Views)



Appendix A: Related Standards

The following is a list of standards relevant to the RS8228:

- ATM Forum UNI Specification 94/0317
- ATM Forum–ATM User Network Interface Specification V3.1, September 1994
- ATM Forum Utopia Level 1 Specification, Ver. 2.01, af-phy-0017.000
- ATM Forum Utopia Level 2 Specification, Ver. 1.0, af-phy-0039.000
- ATM Forum—ATM-PHY/95-0766R2: WIRE Specification
- Bellcore Specification T1S1/92-185
- ITU Recommendation I.432, “B-ISDN User Network Interface - Physical Interface Specification,” June 1990
- ITU Recommendation G.709, “Synchronous Multiplexing Structure,” 1990
- ITU-T Recommendation G.804, “ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)”
- ITU Recommendation Q.921: ISDN User-Network Interface Data Link Layer Specification, 03/93
- ANSI T1.627-1993: Broadband ISDN—ATM Layer Functionality and Specification
- I.610: B-ISDN Operation and maintenance Principles and Functions
- GR-1248: Generic Requirements for Operation of ATM Network Elements

The documents listed above can be obtained from the following companies:

Bellcore
Customer Service
8 Corporate Place - Room 3C-183
Piscataway, NJ 08854-4156
1-800-521-CORE

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
1-800-433-5177
1-503-797-4207

ATM FORUM
The ATM Forum
303 Vintage Park Drive
Foster City, CA 94404-1138

ANSI
11 West 42nd Street
New York, NY 10036
1-212-642-4900

For ITU documents contact:

Omnicom
Phillips Business Information
1201 Seven Locks Road, Suite 300
Potomac, MD 20854
1-800 OMNICOM (666-4266)

Appendix B: Boundary Scan

The RS8228 supports boundary scan testing conforming to IEEE standard 1149.1a-1993 and Supplement 1149.1b, 1994. This appendix is intended to assist the customer in developing boundary scan tests for printed circuit boards and systems that use the RS8228. It is assumed that the reader is familiar with boundary scan terminology. For the latest version of the Boundary Scan Description Language (BSDL) file, contact Conexant.

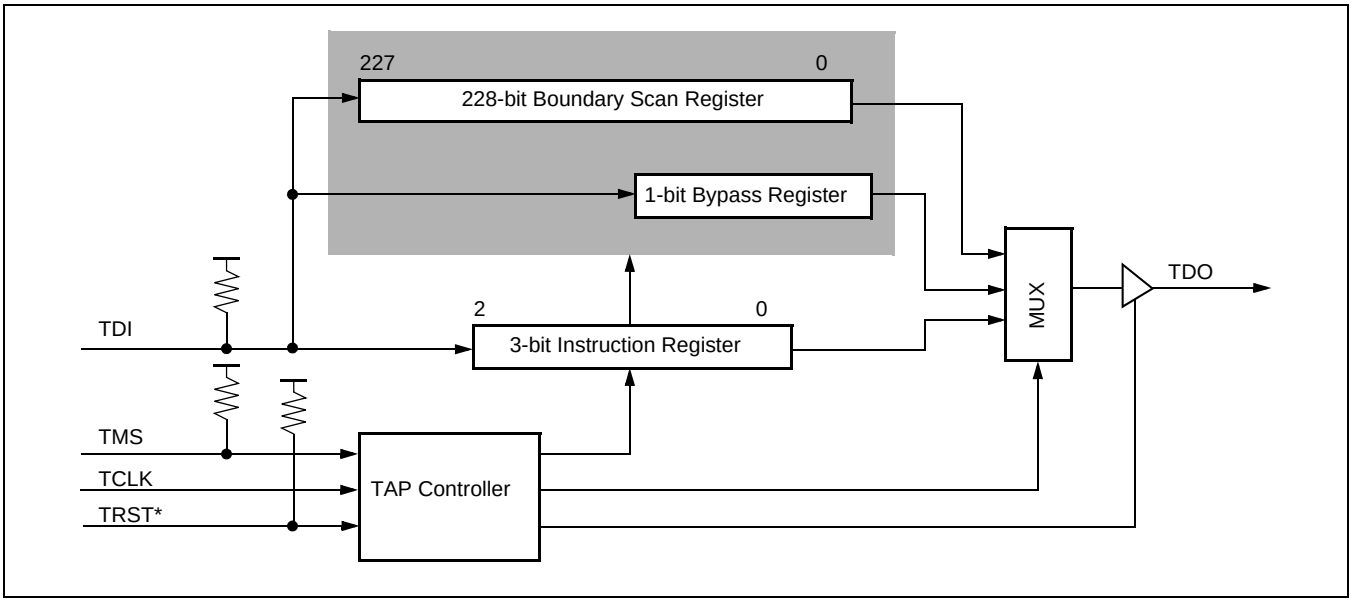
The Boundary Scan section of the RS8228 provides access to all external I/O signals of the device for board and system-level testing. The boundary scan test logic is accessed through five dedicated pins on the RS8228 (see Table B-1).

Table B-1. Boundary Scan Signals

Pin Name	Signal Name	I/O	Definition
TRST*	Test Logic Reset	I	When at a logic low, this signal asynchronously resets the boundary scan test circuitry and puts the test controller into the reset state. This state allows normal system operation.
TCLK	Test Clock	I	Test clocking is generated externally by the system board or by the tester. TCLK can be stopped in either the high state or the low state.
TMS	Test Mode Select	I	Decoded to control test operations.
TDO	Serial Test Data Output	O	Outputs serial test data.
TDI	Serial Test Data Input	I	Input for serial test data.

The test circuitry includes the Boundary Scan Register, a BYPASS Register, an Instruction Register, and the Test Access Port (TAP) controller (see Figure B-2).

Figure B-2. Test Circuitry Block Diagram



B.1 Instruction Register

The Instruction Register (IR) is a 3-bit register. When the boundary scan circuitry is reset, the IR is loaded with the BYPASS Instruction. The Capture-IR binary value is 001.

The eight instructions include three IEEE 1149.1 mandatory public instructions (BYPASS, EXTEST, and SAMPLE/PRELOAD) and five private instructions for manufacturing use only. Bit-0 (LSB) is shifted into the instruction register first.

Table 2-3. IEEE Std. 1149.1 Instructions

Bit 2	Bit 1	Bit 0	Instruction	Register Accessed
0	0	0	EXTEST	Boundary Scan
0	0	1	SAMPLE/PRELOAD	Boundary Scan
0	1	0	Private	—
0	1	1	Private	—
1	0	0	Private	—
1	0	1	Private	—
1	1	0	Private	—
1	1	1	BYPASS	Bypass

B.2 BYPASS Register

The BYPASS Register is a 1-bit shift register used to pass TDI data to TDO, to facilitate testing other devices in the scan path without having to shift the data patterns through the complete Boundary Scan Register of the RS8228.

B.1 Boundary Scan Register

The Boundary Scan Register is a 116-bit shift register that passes TDI data to the TDO to facilitate testing RS8228 pin connections. Table 2-4 defines the Boundary Scan Register cells. Cell 0 is closest to TDO in the chain. All controlling cells put their respective output cell into the inactive state with a value of 1.

Table 2-4. Boundary Scan Register Cells *(1 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
0	(1)	controlr	—
1	OneSecOut	output3	—
2	OneSecIn	input	—
3	8kHzIn	input	—
4	Reset~	input	—
5	MClk	input	—
6	MSyncMode	input	—
7	(1)	controlr	—
8	Mint~	output3	7
9	LInt~[7]	input	—
10	(1)	controlr	—
11	LCs[7]	output3	10
12	LInt~[6]	input	—
13	(1)	controlr	—
14	LCs[6]	output3	13
15	LInt~[5]	input	—
16	(1)	controlr	—
17	LCs[5]	output3	16
18	LInt~[4]	input	—
19	(1)	controlr	—
20	LCs[4]	output3	19
21	LInt~[3]	input	—
22	(1)	controlr	—
23	LCs[3]	output3	22
24	LInt~[2]	input	—

Table 2-4. Boundary Scan Register Cells *(2 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
25	(1)	controlr	—
26	LCs[2]	output3	25
27	LInt~[1]	input	—
28	(1)	controlr	—
29	LCs[1]	output3	28
30	LInt~[0]	input	—
31	(1)	controlr	—
32	LCs[0]	output3	31
33	(1)	controlr	—
34	MData[7]	bidir	33
35	MData[6]	bidir	33
36	MData[5]	bidir	33
37	MData[4]	bidir	33
38	MData[3]	bidir	41
39	MData[2]	bidir	41
40	MData[1]	bidir	41
41	(1)	controlr	—
42	MData[0]	bidir	41
43	MAddr[12]	input	—
44	MAddr[11]	input	—
45	MAddr[10]	input	—
46	MAddr[9]	input	—
47	MAddr[8]	input	—
48	MAddr[7]	input	—
49	MAddr[6]	input	—
50	MAddr[5]	input	—
51	MAddr[4]	input	—
52	MAddr[3]	input	—
53	MAddr[2]	input	—
54	MAddr[1]	input	—
55	MAddr[0]	input	—
56	MAs~,MWr~	input	—
57	MCs~	input	—

***Table 2-4. Boundary Scan Register Cells** (3 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
58	MW/R~,MRd~	input	—
59	(1)	controlr	—
60	MRdy	output3	59
61	URxAddr[4]	input	—
62	URxAddr[3]	input	—
63	URxAddr[2]	input	—
64	URxAddr[1]	input	—
65	URxAddr[0]	input	—
66	URxData[15]	output3	69
67	URxData[14]	output3	69
68	URxData[13]	output3	69
69	(1)	controlr	—
70	URxData[12]	output3	69
71	URxData[11]	output3	74
72	URxData[10]	output3	74
73	URxData[9]	output3	74
74	(1)	controlr	—
75	URxData[8]	output3	74
76	URxData[7]	output3	79
77	URxData[6]	output3	79
78	URxData[5]	output3	79
79	(1)	controlr	—
80	URxData[4]	output3	79
81	URxData[3]	output3	84
82	URxData[2]	output3	84
83	URxData[1]	output3	84
84	(1)	controlr	—
85	URxData[0]	output3	84
86	(1)	controlr	—
87	URxPrty	output3	86
88	(1)	controlr	—
89	URxSOC	output3	88
90	(1)	controlr	—

Table 2-4. Boundary Scan Register Cells *(4 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
91	URxClAv	output3	90
92	URxEnb~	input	—
93	URxClk	input	—
94	UTxClk	input	—
95	UTxEnb~	input	—
96	UTxSOC	input	—
97	(1)	controlr	—
98	UTxClAv	output3	97
99	UTxPrty	input	—
100	UTxData[15]	input	—
101	UTxData[14]	input	—
102	UTxData[13]	input	—
103	UTxData[12]	input	—
104	UTxData[11]	input	—
105	UTxData[10]	input	—
106	UTxData[9]	input	—
107	UTxData[8]	input	—
108	UTxData[7]	input	—
109	UTxData[6]	input	—
110	UTxData[5]	input	—
111	UTxData[4]	input	—
112	UTxData[3]	input	—
113	UTxData[2]	input	—
114	UTxData[1]	input	—
115	UTxData[0]	input	—
116	UTxAddr[4]	input	—
117	UTxAddr[3]	input	—
118	UTxAddr[2]	input	—
119	UTxAddr[1]	input	—
120	UTxAddr[0]	input	—
121	LTxClk[0]	input	—
122	LTxSync[0]	input	—
123	(1)	controlr	—

Table 2-4. Boundary Scan Register Cells (5 of 8)

Cell	Related Pin Name	Cell Type	Controlling Cell
124	LTxData[0]	output3	123
125	LRxClk[0]	input	—
126	LRxData[0]	input	—
127	LRxSync[0]	input	—
128	LRxHld[0]	input	—
129	LStatOut[3][0]	output3	132
130	LStatOut[2][0]	output3	132
131	LStatOut[1][0]	output3	132
132	(1)	controlr	—
133	LStatOut[0][0]	output3	132
134	LTxClk[1]	input	—
135	LTxSync[1]	input	—
136	(1)	controlr	—
137	LTxData[1]	output3	136
138	LRxClk[1]	input	—
139	LRxData[1]	input	—
140	LRxSync[1]	input	—
141	LRxHld[1]	input	—
142	LStatOut[3][1]	output3	—
143	LStatOut[2][1]	output3	—
144	LStatOut[1][1]	output3	145
145	(1)	controlr	—
146	LStatOut[0][1]	output3	145
147	LTxClk[2]	input	—
148	LTxSync[2]	input	—
149	(1)	controlr	—
150	LTxData[2]	output3	149
151	LRxClk[2]	input	—
152	LRxData[2]	input	—
153	LRxSync[2]	input	—
154	LRxHld[2]	input	—
155	LStatOut[3][2]	output3	158
156	LStatOut[2][2]	output3	158

Table 2-4. Boundary Scan Register Cells *(6 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
157	LStatOut[1][2]	output3	158
158	(1)	controlr	—
159	LStatOut[0][2]	output3	158
160	LTxClk[3]	input	—
161	LTxSync[3]	input	—
162	(1)	controlr	—
163	LTxData[3]	output3	162
164	LRxClk[3]	input	—
165	LRxData[3]	input	—
166	LRxSync[3]	input	—
167	LRxHld[3]	input	—
168	LStatOut[3][3]	output3	171
169	LStatOut[2][3]	output3	171
170	LStatOut[1][3]	output3	171
171	(1)	controlr	—
172	LStatOut[0][3]	output3	171
173	LTxClk[4]	input	—
174	LTxSync[4]	input	—
175	(1)	controlr	—
176	LTxData[4]	output3	175
177	LRxClk[4]	input	—
178	LRxData[4]	input	—
179	LRxSync[4]	input	—
180	LRxHld[4]	input	—
181	LStatOut[3][4]	output3	184
182	LStatOut[2][4]	output3	184
183	LStatOut[1][4]	output3	184
184	(1)	controlr	—
185	LStatOut[0][4]	output3	184
186	LTxClk[5]	input	—
187	LTxSync[5]	input	—
188	(1)	controlr	—
189	LTxData[5]	output3	188

Table 2-4. Boundary Scan Register Cells (7 of 8)

Cell	Related Pin Name	Cell Type	Controlling Cell
190	LRxClk[5]	input	—
191	LRxData[5]	input	—
192	LRxSync[5]	input	—
193	LRxHld[5]	input	—
194	LStatOut[3][5]	output3	197
195	LStatOut[2][5]	output3	197
196	LStatOut[1][5]	output3	197
197	(1)	controlr	—
198	LStatOut[0][5]	output3	—
199	LTxClk[6]	input	—
200	LTxSync[6]	input	—
201	(1)	controlr	—
202	LTxData[6]	output3	201
203	LRxClk[6]	input	—
204	LRxData[6]	input	—
205	LRxSync[6]	input	—
206	LRxHld[6]	input	—
207	LStatOut[3][6]	output3	210
208	LStatOut[2][6]	output3	210
209	LStatOut[1][6]	output3	210
210	(1)	input	—
211	LStatOut[0][6]	output3	210
212	LTxClk[7]	input	—
213	LTxSync[7]	input	—
214	(1)	controlr	—
215	LTxData[7]	output3	214
216	LRxClk[7]	input	—
217	LRxData[7]	input	—
218	LRxSync[7]	input	—
219	LRxHld[7]	input	—
220	LStatOut[3][7]	output3	223
221	LStatOut[2][7]	output3	223
222	LStatOut[1][7]	output3	223

Table 2-4. Boundary Scan Register Cells *(8 of 8)*

Cell	Related Pin Name	Cell Type	Controlling Cell
223	(1)	controlr	—
224	LStatOut[0][7]	output3	223
225	Test[1]	input	—
226	Test[2]	input	—
227	Test[3]	input	—

NOTE(S):
(1) See IEEE Std. 1149.1b-1994, Table B.4, for more information on cell types.

Appendix C: Register Summary

Figure C-1 is a quick reference to the RS8228's registers. It lists all of the registers and the bits in each one.

Figure C-1. Register Summary *(1 of 8)*

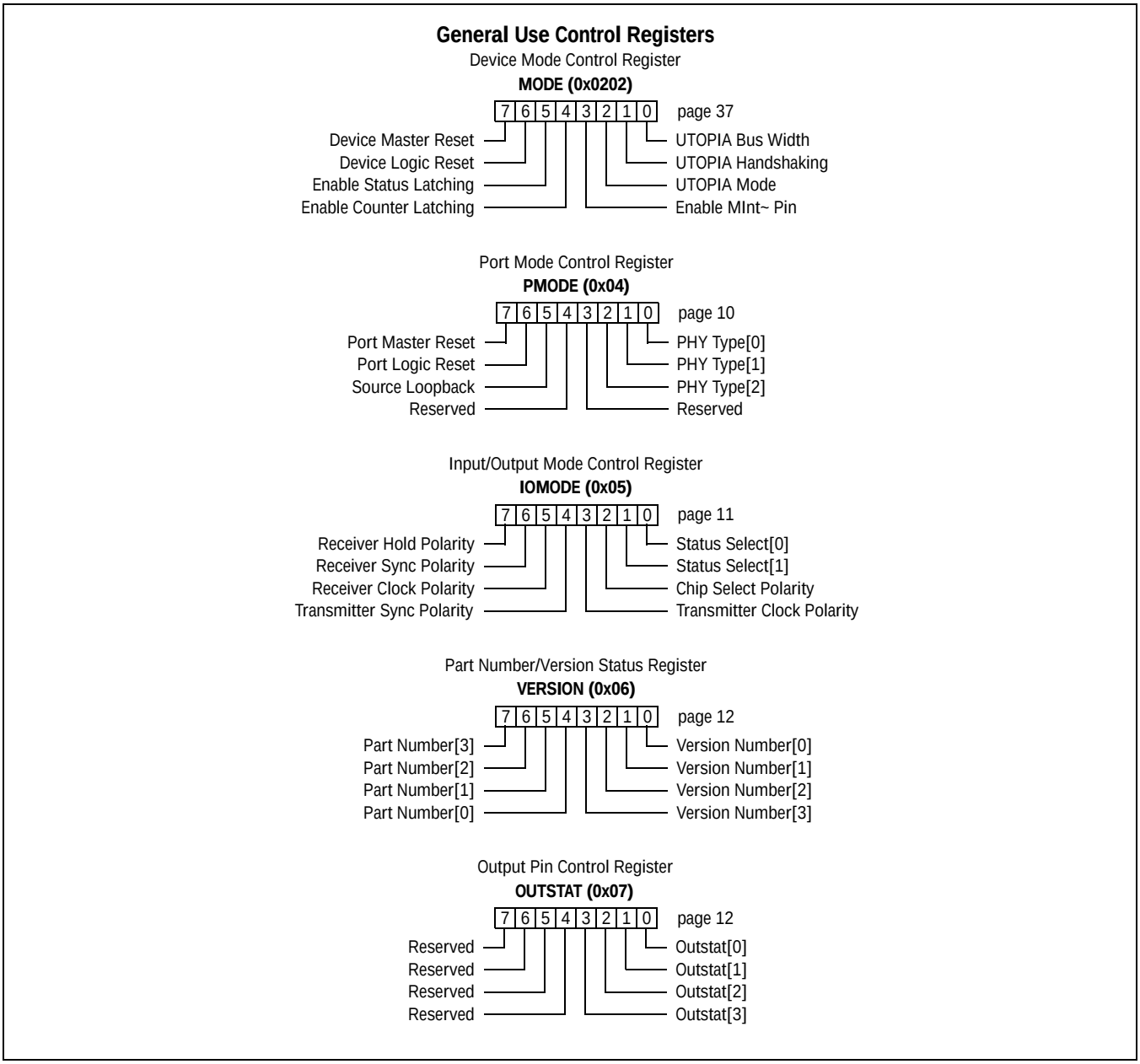


Figure C-1. Register Summary *(2 of 8)*

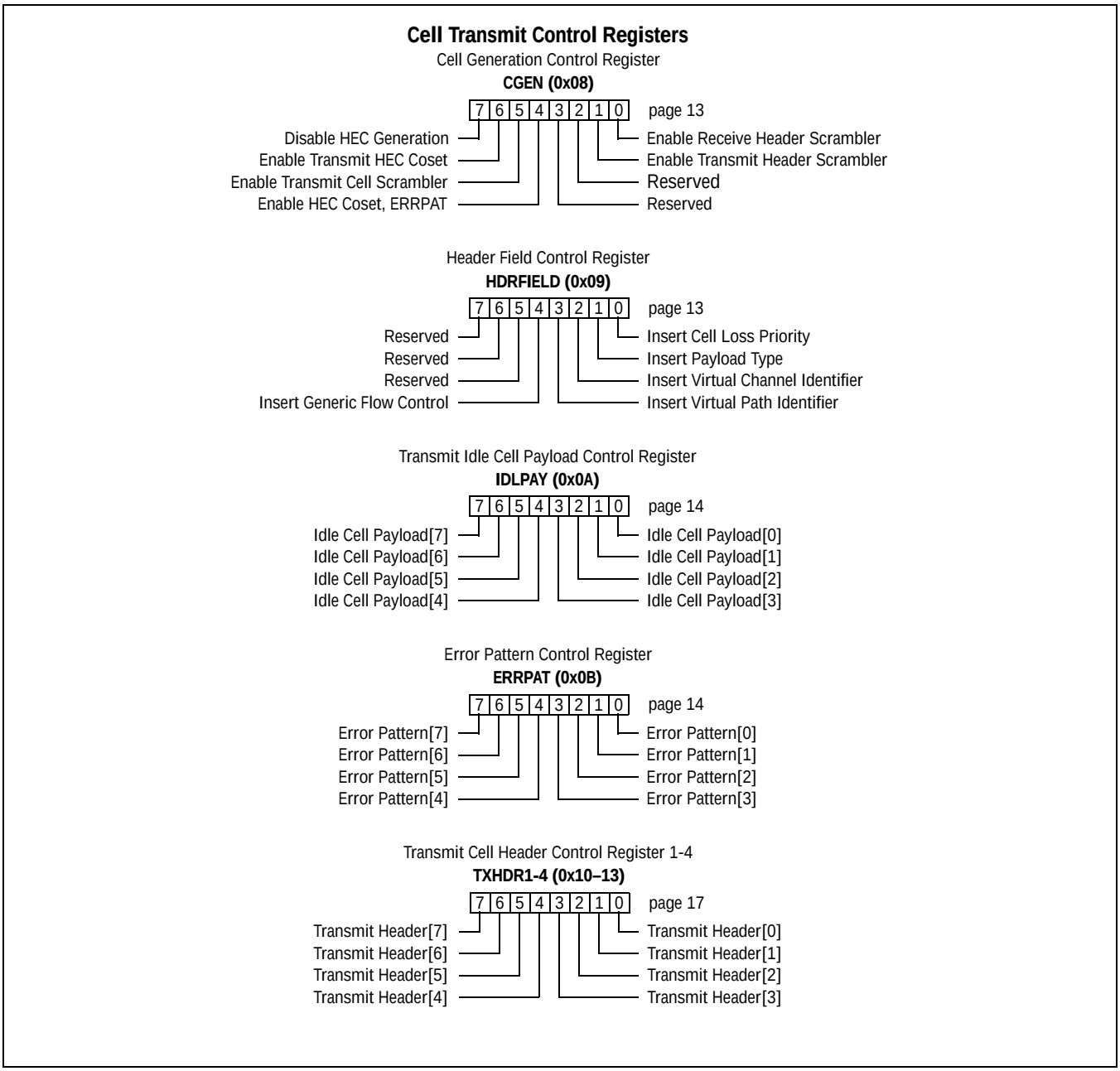


Figure C-1. Register Summary *(3 of 8)*

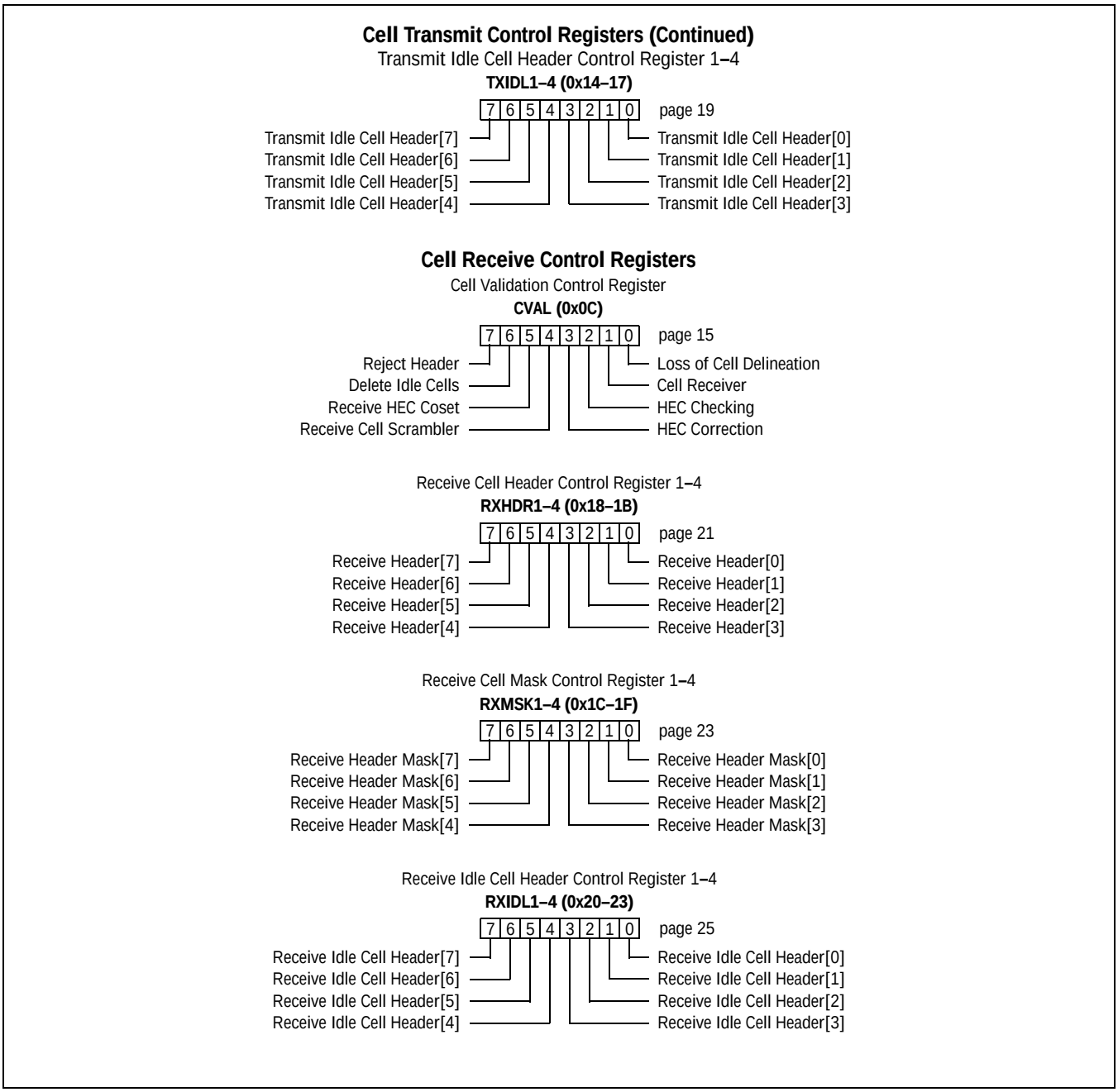


Figure C-1. Register Summary *(4 of 8)*

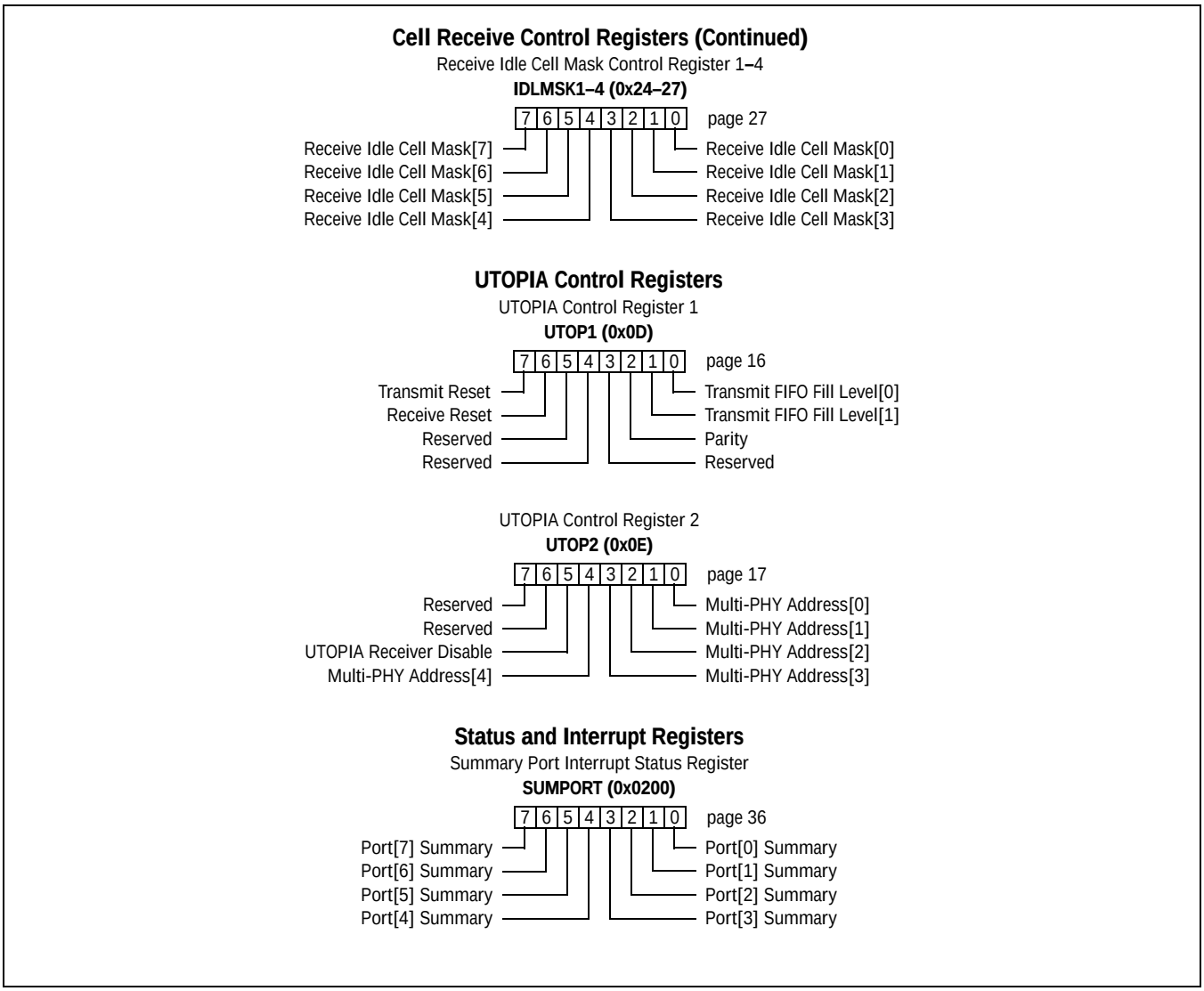


Figure C-1. Register Summary *(5 of 8)*

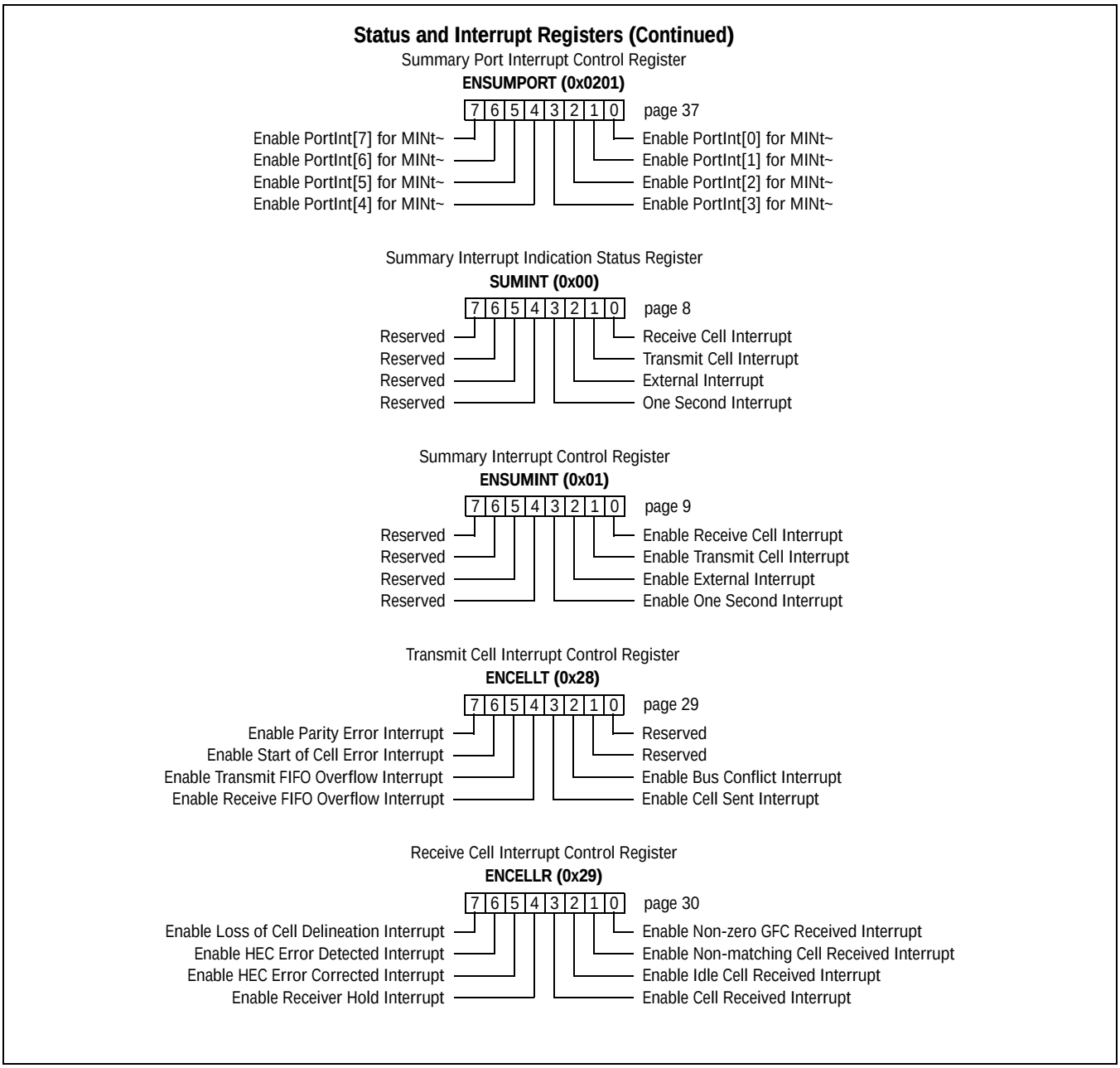


Figure C-1. Register Summary *(6 of 8)*

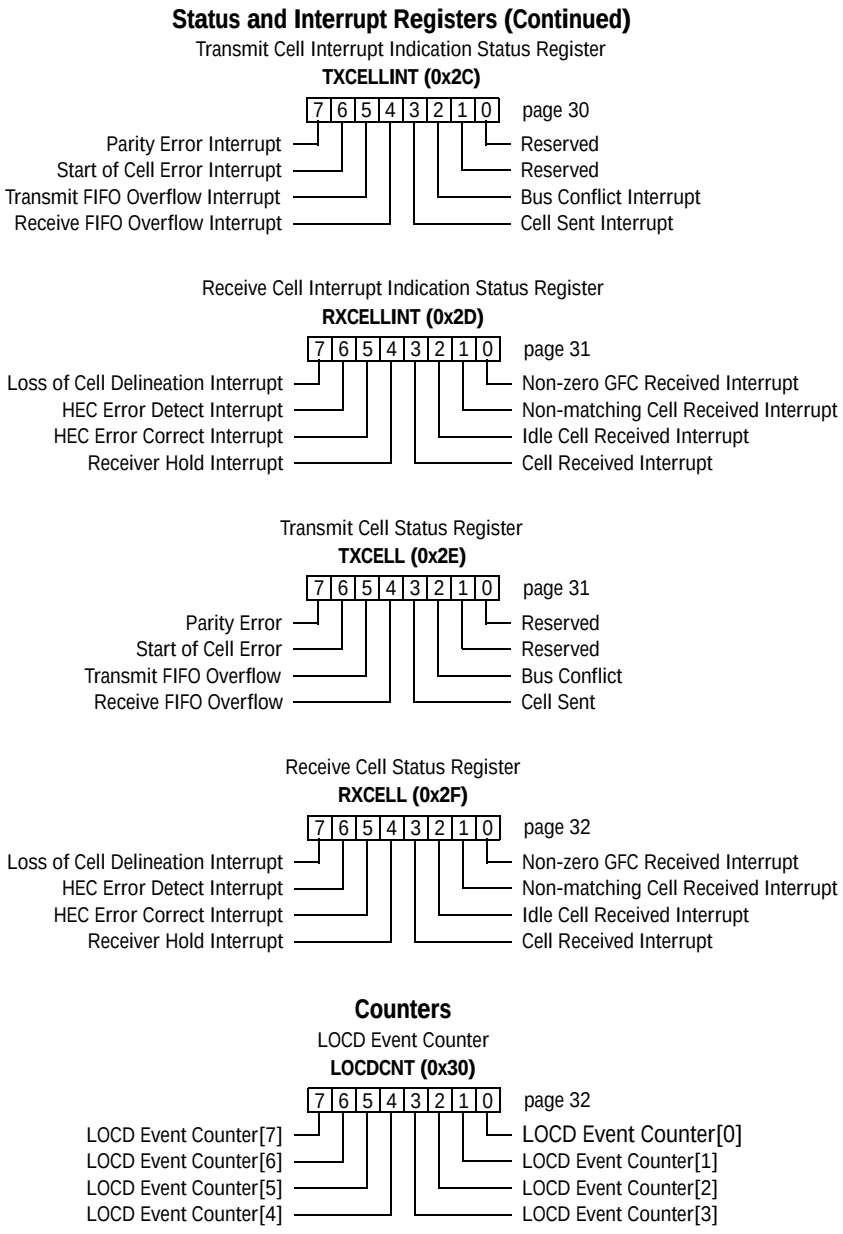


Figure C-1. Register Summary *(7 of 8)*

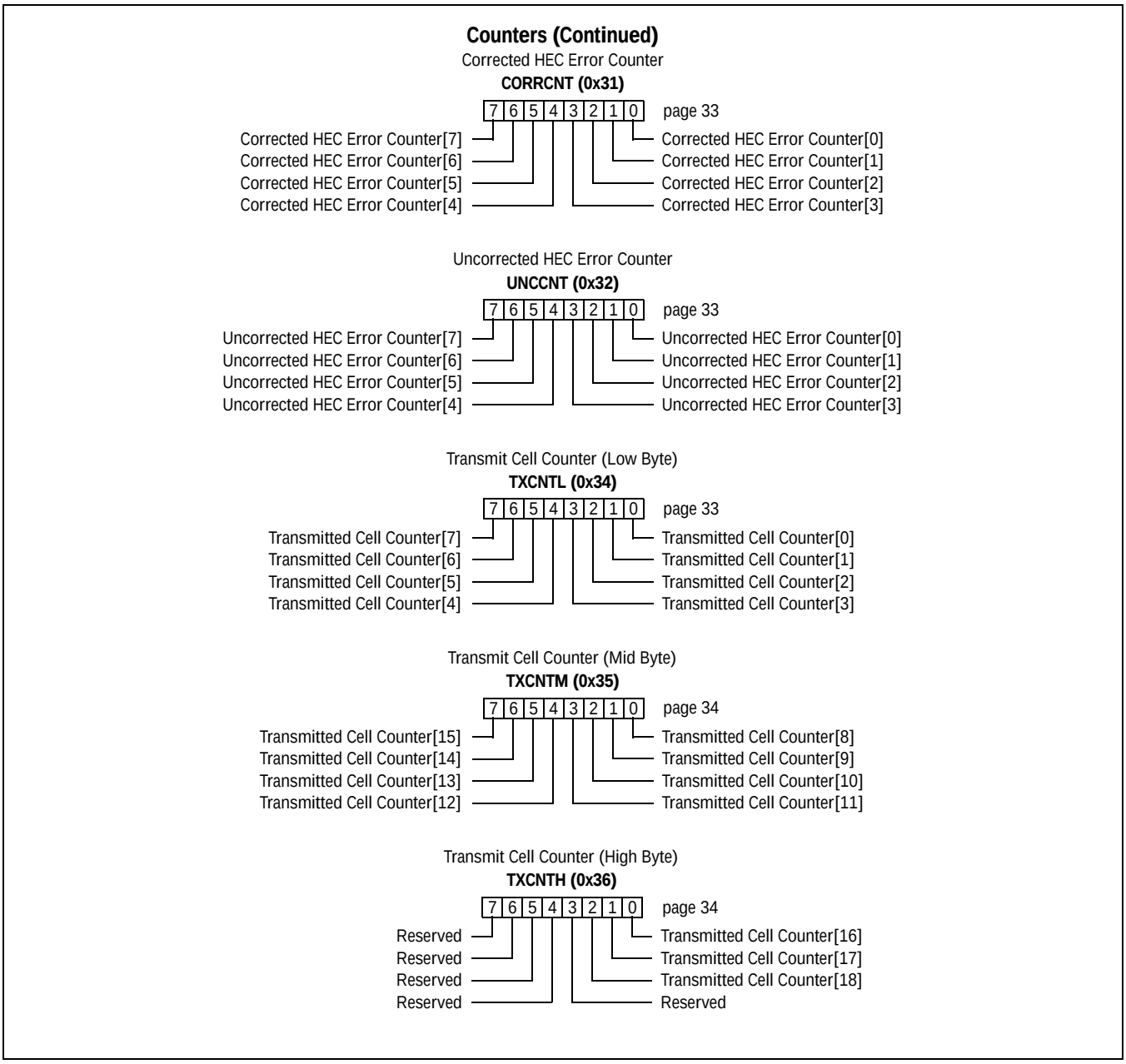
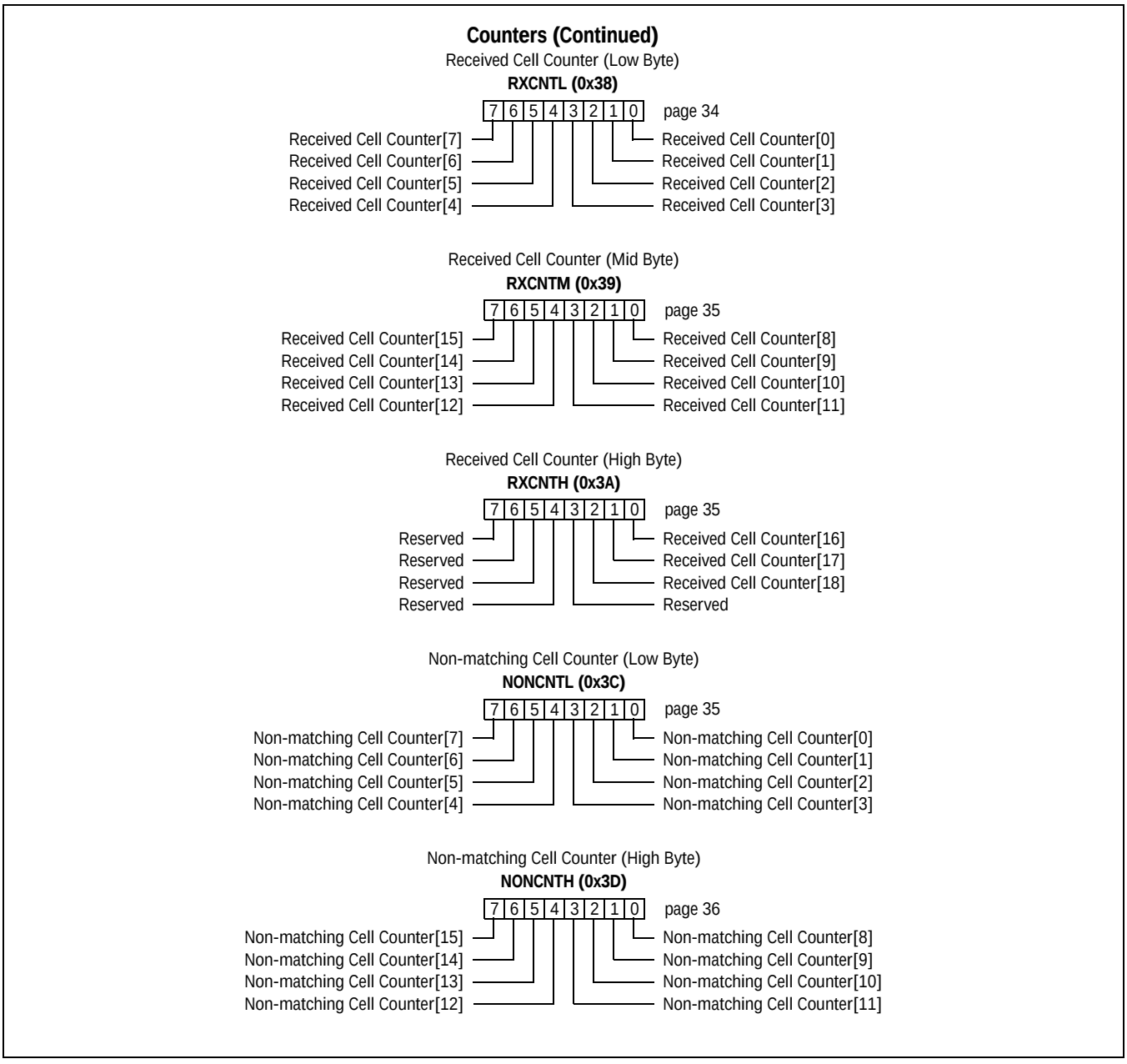


Figure C-1. Register Summary *(8 of 8)*



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