NEC®

4:1 MULTIPLEXER

UPG704 SERIES

FEATURES

- **ECL COMPATIBLE**
- **ULTRA HIGH SPEED**
  UPG704B-10 $f\phi_{MAX}$ = 1 GHz MIN Clock Speed
  UPG704B-15 $f\phi_{MAX}$ = 1.5 GHz MIN Clock Speed
  UPG704B-20 $f\phi_{MAX}$ = 2 GHz MIN Clock Speed
  UPG704B-25 $f\phi_{MAX}$ = 2.5 GHz MIN Clock Speed
- **HERMETIC CERAMIC PACKAGE ASSURES HIGH RELIABILITY**

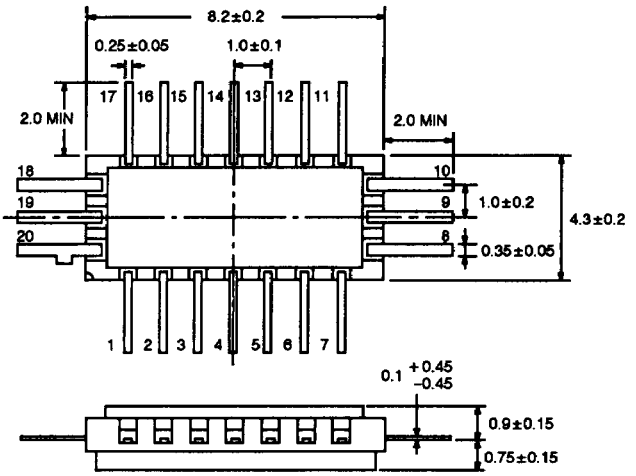
DESCRIPTION AND APPLICATIONS

UPG704B is a GaAs 4 to 1 multiplexer that operates at 1, 1.5, 2 and 2.5 GHz (min.) clock rates. It can interface directly with ECL logic and power supply levels.

It is designed as a multiplexer for high speed digital data transmission systems, digital instrumentation and digital RF memories. The UPG704B is housed in a hermetic 20-pin ceramic package for high reliability.

OUTLINE DIMENSIONS (Units in mm)

OUTLINE H20



PIN CONNECTIONS

1. D_{IN4}	8. V_{SS2}	15. $\overline{Out}$
2. D_{IN3}	9. V_{SS1}	16. Out
3. D_{IN2}	10. SEL	17. V_{DD2}
4. D_{IN1}	11. CK_{OUT}	18. V_{DD1}
5. CK2	12. V_{DD2}	19. V_{SS1}
6. CK1	13. 1/4 CK_{OUT}	20. V_{SS2}
7. 1/4 CK_{IN}	14. V_{DD1}	

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER				UPG704B-10, 704B-15, 704B-20, 704B-25		
SYMBOLS	PARAMETERS	TEST CONDITIONS	UNITS	MIN.	TYP.	MAX.
I_{SS2}	Supply Current	V_{DD1} = V_{DD2} = 0 V V_{SS1} = −2 V V_{SS2} = −5.2 V	mA		160	
V_{OH}	High Level Output Voltage[1]		V	−1	−0.8	−0.6
V_{OL}	Low Level Output Voltage[1]		V	−2	−1.8	−1.6
I_{DD1}[4]	Supply Current		mA		196	
V_{TH}	Threshold Voltage		V		−1.3	
$f\phi_{MAX}$	Maximum Clock Frequency UPG704B-10 UPG704B-15 UPG704B-20 UPG704B-25		 GHz GHz GHz GHz	 1 1.5 2 2.5		
ϕ	Phase Margin[3]		deg.		200	
t_{PD}	Propagation Delay		ps		800	
t_R	Output Rise Time[2]		ps		150	
t_F	Output Fall Time[2]		ps		150	

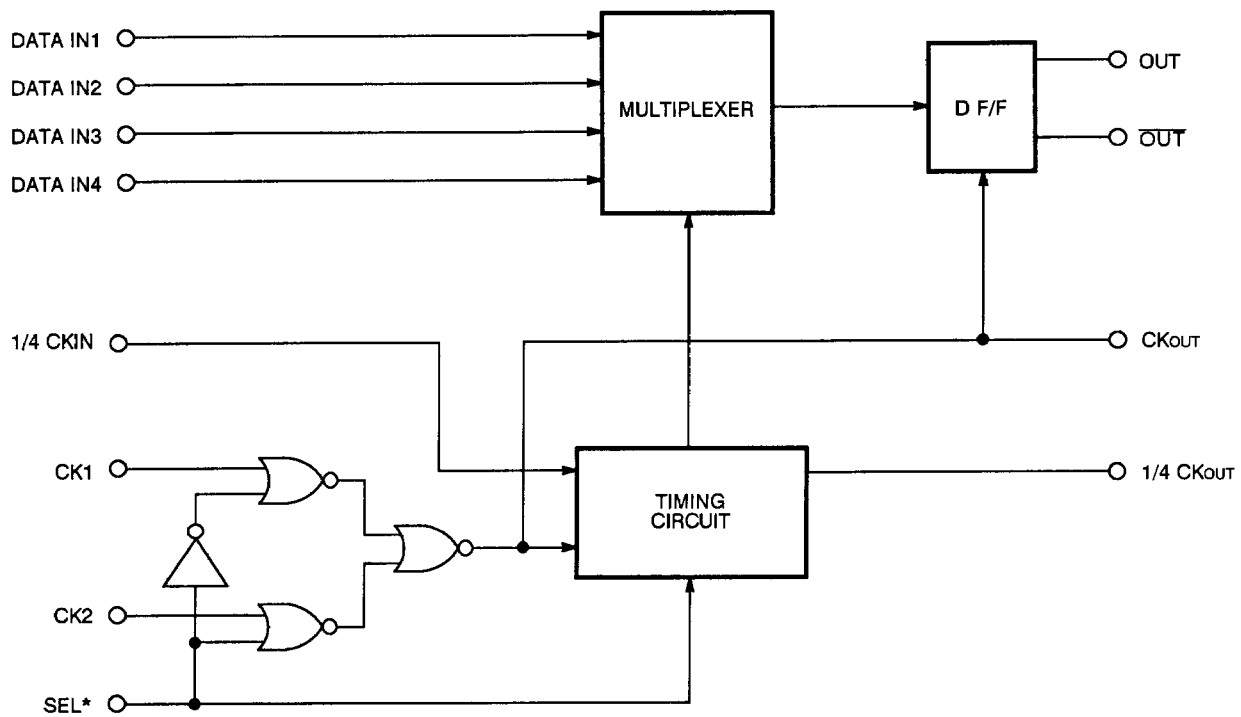
Notes:

1. The value in case 50 Ω load resistance is connected between output and V_{TT} (−2 V) terminal. V_{TT} is the terminating voltage of the external 50 Ω load resistance.
2. The time from 20% to 80% of output voltage amplitude.
3. The phase difference between data and clock at 2 GHz.
4. Test condition: V_{DD1} = V_{DD2} = +2 V; V_{SS1} = Ground; V_{SS2} = −3.2 V.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD1}, V_{DD2}	Supply Voltage	V	+4
V_{SS1}	Terminating Voltage	V	V_{DD1}, V_{DD2} −4
V_{SS2}	Supply Voltage	V	−8
V_{IN}	Input Voltage	V	V_{DD1}, V_{DD2} − V_{SS2}
T_{STG}	Storage Temperature	°C	−65 to +175
$T_{C(OPT)}$	Operating Case Temperature	°C	−65 to +125
P_T	Total Power Dissipation	W	1.7

LOGIC DIAGRAM



* SEL, the input terminal for CK1 or CK2 selecting signal.

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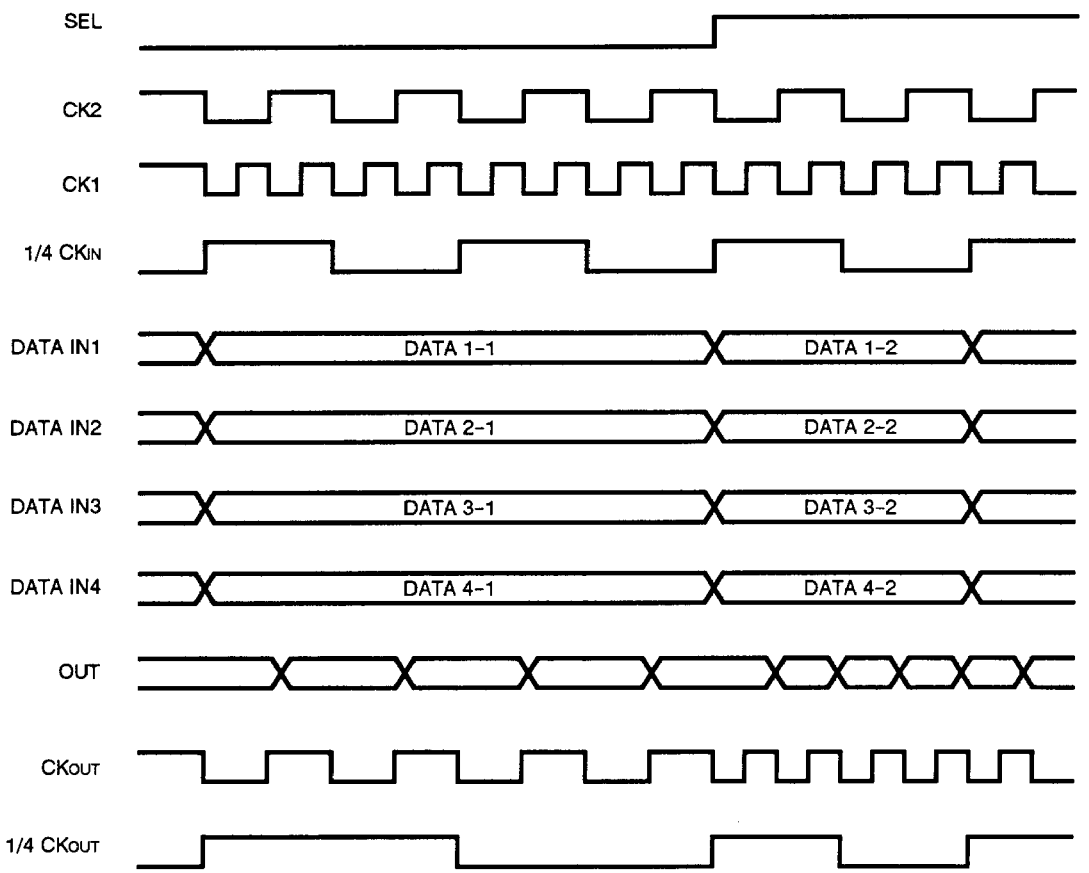
FUNCTIONAL WAVEFORMS



Notes:

1. When a high level voltage (-0.8 V) is applied to SEL terminal the CK1 is selected and it will also be synchronized with the 1/4 CK signal. It is necessary to apply an input to the 1/4 CK_{IN} terminal.
2. When the low level voltage is applied to SEL terminal, CK2 is selected and 1/4 CK signal is generated internally.
3. When SEL terminal is kept open, the low level voltage is generated internally.

Testing and Handling Procedure:

1. Test condition: $V_{DD1} = V_{DD2} = +2$ V; V_{SS1} = Ground: $V_{SS2} = -3.2$ V.
2. The metallized section on the back surface of the package is used as a heat sink, and is electrically connected with the V_{SS2} terminal ($V_{SS2} = -5.2$ normally). Do not ground the metallized section to GND (0 V). This is to prevent a short circuit between V_{DD} ($V_{DD} = 0$ V normally) and V_{SS2} or some other terminals.
3. When handling the device a ground strap should be used to prevent Electric Static Discharge (ESD) that can damage the GaAs MES FETs in the IC.